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De-Embedding Method Using EM Simulator for Characterization of FETs and Its Applicability to Lossy Substrates

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1. Introduction

Accurate characterization of field effect transistors (FETs) is necessary for accurate design of monolithic-microwave integrated-circuit (MMIC). Extraction of FET parameters is difficult because the FET is embedded in the parasitic circuit, which is referred to as test element group (TEG), as shown in Fig.1 to connect probe and biases. De-embedding method using open/short-TEG [1] had been widely used in the characterization of FET. But this method has difficulties, especially in high frequencies, mainly in two reasons; (1) incompleteness of open and short pattern, and (2) approximation of a parasitic circuit by an equivalent circuit topology. In order to overcome these problems, the de-embedding method using EM simulator was proposed [2][3]. And it is shown by the authors that the de-embedding method using EM simulator has higher accuracy than the conventional de-embedding method using open/short-TEG [4].

In this paper, applicability of the de-embedding method using EM simulator for a coplanar-type TEG with lossy substrates is investigated because the FET characterization on Si CMOS is very serious problem in the millimeter-wave band.

2. De-Embedding Method Using EM Simulator

Figure 2 shows flow chart of conventional and proposed de-embedding method. In the conventional de-embedding method using open/short-TEG [1], the parasitic circuit was approximated by equivalent circuit model, which causes error in the estimation of the embedded FET [4]. On the other hand, the parasitic circuit is characterized by the EM simulator in the proposed de-embedding method, which has no approximation in the modeling. The accuracy of the EM simulator is the essential factor in the algorithm, and it must be verified. For example, it can be done by comparing the measured and analyzed S-parameters using open/short-TEG. Z-parameters of the FET are extracted by using S-parameters of the parasitic circuit and measured S-parameters of the FET-TEG [3].

3. TEG Structure

Figure 3 shows the TEG structure considered in the paper. Port1 and Port2 in Fig.3 (a) are the coplanar waveguide (CPW) with characteristic impedance of 55Ω. Two FETs with the same characteristics are embedded in the TEG. Because of the symmetry of the structure and excitation, the analysis model for Fig.3 (a) can be reduced to a half of the whole structure as shown in Fig.3 (b). A magnetic wall, or perfect magnetic conductor (PMC), is assumed at the symmetry center. The analysis model for FEM-based EM simulator Ansoft HFSS is also shown in Fig.3 (b). Terminals of the transmission line are modeled as wave ports, and terminals for a lumped device are modeled as lumped ports.

4. Numerical Results

The proposed de-embedding method using EM simulator is demonstrated fully-numerically, and compared with the conventional de-embedding method using open/short-TEG. The commercial software Ansoft HFSS is used in the paper. A TEG with given lumped impedances at the surface of lumped ports 3 and 4 will be used to simulate measured S-parameters of the FET-TEG. $R_3 = 50\,\Omega$ and $C_3 = 0.1$pF are connected in parallel at the position of Port3 in Fig.3 (b), while $R_4 = 75\,\Omega$ and $L_4 = 1$nH are connected in parallel at the position of Port4. Open/short-TEG are modeled, and simulated S-parameters are used in the simulation of conventional de-embedding method using open/short-TEG [1].

Figure 4 shows the result of numerical simulation of de-embedding when the conductivity of the substrate is $\sigma = 10$ S/m, which is the typical value for Si-CMOS substrate. Parameters of lumped devices at Port 3 and Port 4 can be calculated by the extracted Y-parameters $Y^{(\mathrm{DEV})} = Z^{(\mathrm{DEV})^{-1}}$; $R_3 = 1/\mathrm{Re}[Y_{11}^{(\mathrm{DEV})}]$, $C_3 = \mathrm{Im}[Y_{11}^{(\mathrm{DEV})}]/\omega$, $R_4 = 1/\mathrm{Re}[Y_{22}^{(\mathrm{DEV})}]$, $L_4 = -1/\left(\omega \mathrm{Im}[Y_{22}^{(\mathrm{DEV})}]\right)$. It is observed that the result of the proposed de-embedding method using EM analysis (solid curve) has higher accuracy than that of the conventional one using open/short-TEG (dotted curve).

Figure 5 shows conductivity of substrate vs. average error of extracted lumped values. Average error is defined by

$$E_{av} = \underset{f=10GHz-110GHz}{ave} \left\{ \underset{i=3,4}{ave} \left| \frac{Y_{0i} - Y_i}{Y_{0i}} \right| \right\}$$

where Y_{0i} is the specified admittance at Port i; $Y_{03} = 1/R_3 + j\omega C_3$ and $Y_{04} = 1/R_4 + 1/(j\omega L_4)$. Y_i is the extracted admittance for Port i. $\underset{x=x_1-x_2}{ave}$ means to take average over the parameter x from x_1 to x_2. It is clearly seen that the proposed de-embedding method has higher accuracy below 4% from $\sigma = 0$ to $\sigma = 100$ S/m. The accuracy of the conventional de-embedding method is about 27% even when the conductivity is small. Moreover, the accuracy degrades when the conductivity becomes larger than 1S/m in the conventional method.

5. Conclusion

The accuracy of the proposed de-embedding method using EM simulator is investigated for lossy substrates. It was found that the proposed de-embedding method using EM simulator has higher accuracy than the conventional one using open/short-TEG, even when the conductivity of substrate is as large as 100S/m. The accuracy of conventional method degrades when the conductivity becomes larger than 1S/m. The proposed de-embedding method will be used for the FET characterization, which is necessary for Si-CMOS RF circuit design in 60GHz band.

Acknowledgments

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References

[1] M.C.A.M. Koolen, J.A.M. Geelen, and M.P.J.G. Versleijen, “An improved de-embedding technique for on-wafer high-frequency characterization,” Proc. IEEE, Bipolar/BiCMOS Circuits and Tech. Meeting, pp.188-191, Sept. 1991.

[2] S. Bousnina, C. Falt, P. Mandeville, A.B. Kouki, and F.M. Ghannouchi, “An accurate on-wafer deembedding technique with application to HBT devices characterization,” IEEE Trans. MTT, Vol.50, No.2, pp.420-424, Feb. 2002.

[3] T. Hirano, J. Hirokawa, M. Ando, H. Nakano, and Y. Hirachi, "De-embedding of lumped-element characteristics with the aid of EM analysis," Digest of IEEE AP-S International Symposium and USNC/URSI National Radio Science Meeting, Session: 436.3, July 5-12, 2008.
[4] T. Hirano, H. Nakano, Y. Hirachi, J. Hirokawa, and M. Ando, "De-embedding method using EM simulator for device characterization and error estimation of conventional method using open/short-TEG," Proc. of International Symposium on Antennas and Propagation (ISAP), Session: TP-D07, Paper No.: 1645248, October 27-30, 2008.

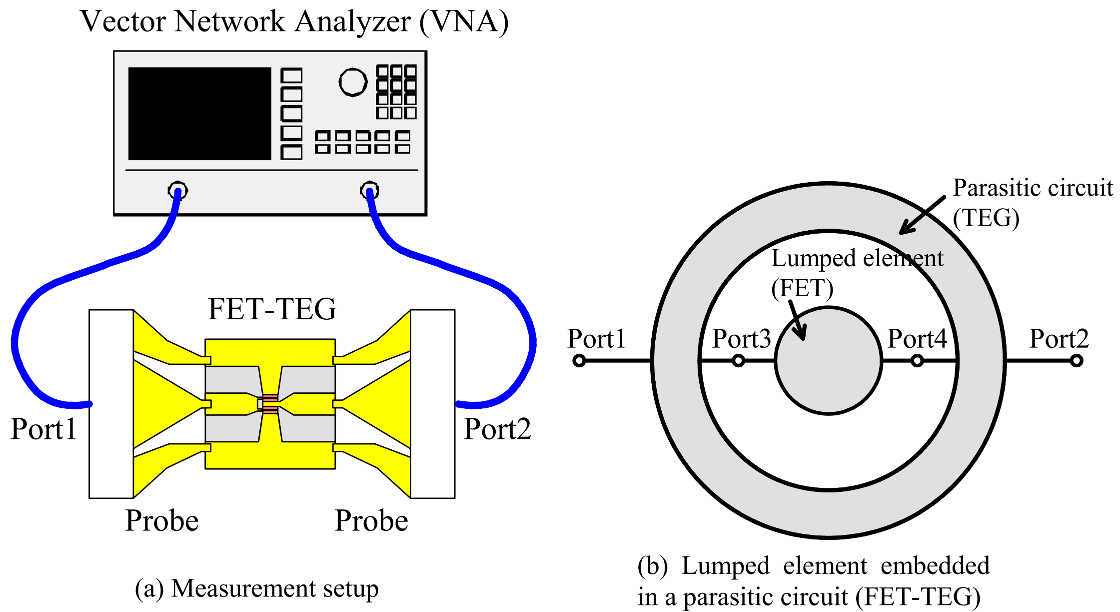


Figure 1: Measurement Setup of the FET-TEG

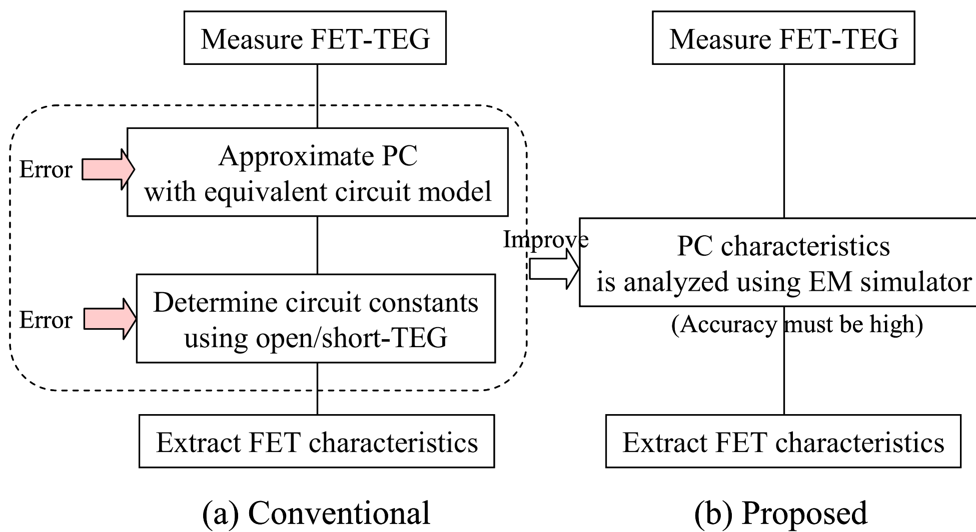
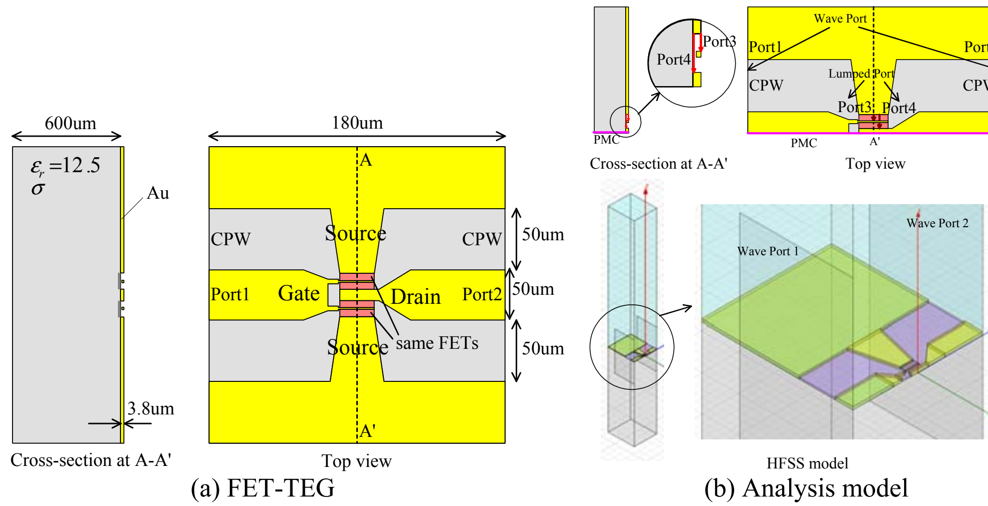


Figure 2: Flow chart of De-embedding Method



(a) FET-TEG (b) Analysis model

Figure 3: TEG Structure

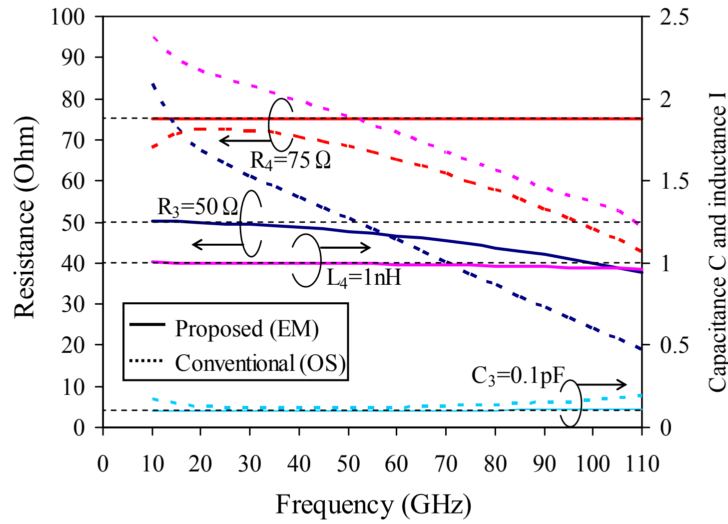


Figure 4: Simulation of Extraction for Lossy Substrate ($\sigma = 10$ S/m)

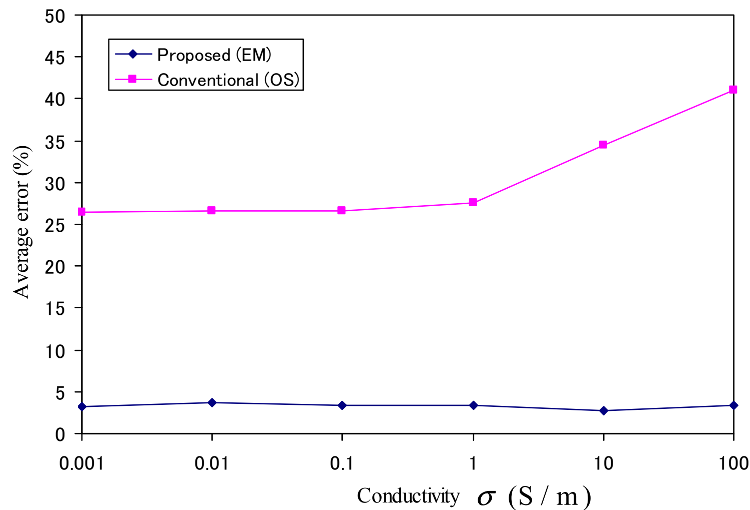


Figure 5: Conductivity of Substrate vs. Average Error of Extracted Lumped Values