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Large detector array and real-time processing and elemental image projection of X-ray and proton microprobe fluorescence data

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Abstract

A detector concept is described that integrates a large solid-angle detector array developed at Brookhaven National Laboratory and a high speed pipelined parallel processing engine developed at CSIRO for machine vision, with an embedded implementation of the *Dynamic Analysis* method for fluorescence spectra deconvolution and image projection, to yield a detection system capable of energy-dispersive detection, spectral deconvolution and real-time elemental imaging at $\sim 10^8$ events per second for PIXE elemental imaging using the nuclear microprobe and SXRF elemental imaging using the synchrotron X-ray microprobe.

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1. Introduction

Detectors place a limit on the performance of proton microprobe and synchrotron X-ray microprobe beamlines. All things being equal, an increase of two orders of magnitude in detector solid-angle would enable an order of magnitude improvement in detection limits, or dramatically shortened analysis times. Sample damage induced in sensitive samples (e.g. biological samples under proton bombardment, redox sensitive samples in a focussed X-ray beam) places an upper limit on integrated beam flux. Increased detector solid-angle can be used to improve detection limits at constant flux. However, increasing solid-angle also increases count-rates, so the benefits of increased solid-angle can only be realized if the count-rate capacity of the detection system is also increased.

An additional problem prevalent in many synchrotron microprobe detection systems is slow pixel rate (beam advance across a sample) caused by spectra read-out delays. Hence, this increased count-rate must be achieved using approaches that solve the read-out problem, such as doing event-by-event processing of detector signals, which also permits the application of techniques for real-time spectral deconvolution and quantitative image projection.

The approach reported here is our next step towards a more holistic approach to spectroscopy detectors that combines a monolithic detector array, application specific integrated circuits (ASICs) and dedicated parallel processors for real-time signal processing into one integrated package.

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This approach offers the potential of building a real-time true elemental microscope, built on a massive increase in data-rates, with interactive quantitative images available continuously to users. This paper describes the detector concept and summarises progress towards this goal and the results of recent tests of major components.

2. Detector components

The detector concept comprises: (i) a monolithic solid-state detector array, with a large number of detector elements, that subtends a large solid-angle; (ii) dedicated 32-channel ASICs for pre-amplification and pulse-shaping; (iii) fast ADCs and pile-up rejection; (iv) real-time pulse-processing of all detector events, with sampling of stage *XY*; (v) real-time spectral deconvolution using the *Dynamic Analysis* (DA) method [1] to project true elemental images and (vi) an interactive graphical user interface that enables direct, real-time interrogation of image data for quantitative information, even as data are still accumulating.

2.1. Detector array

The solid-state detector array is composed of 384 elements each $1 \times 1\ mm^2$ area, fabricated at the Instrumentation Division, BNL, using a 400 μm thick high-resistivity (4–6 kΩ cm) n-type Si(1 1 1) wafer [2,3]. The elements are arranged in an annular array (20×20), with a central hole for the beam, which permits a detection solid-angle of ∼1500 msr to be achieved. The array is cooled to −35 °C using Peltier cooling elements mounted on a water-cooled copper heat-sink. The issue of charge-sharing between pixel pads is addressed using a heavy metal foil mask to absorb X-ray that may otherwise share signal between detector elements [4]. The mask is made from molybdenum sheet (125 μm thick) by lithography and chemical machining. The mask is aligned visually and then checked under an IR microscope; silicon is transparent to infra-red light. The back-side aluminium is patterned in registry with the pixels. Placing the mask so that no light is seen guarantees its alignment.

2.2. Analogue processing

Detector pads are wire-bonded to dedicated pre-amplifier channels on 32 channel HERMES analogue processing ASICs, designed at the Instrumentation Division, BNL [3]. Each channel implements a low-noise preamplifier with a p-channel input MOSFET, a high-order shaper and baseline stabilizer [3,5]. The preamplifier incorporates an n-channel MOSFET in feedback, operating in saturation to realize a low-noise fully compensated continuous reset circuit [6]. The configuration is self-adaptive to leakage currents from the sub-pA to the nA scale. The second and third stages of the shaper provide two pairs of complex conjugate poles, forming a fifth order complex semi-Gaussian shaper providing better noise filtering performance at high count rate than low order shapers. The analogue processing chain has adjustable peaking time (0.5, 1, 2, 4 μs) and gain (750 mV/fC, 1500 mV/fC) [3].

2.3. Peak-detection and time-over-threshold

The method for pile-up rejection uses time-over-threshold (ToT), the length of the analogue quasi-Gaussian pulse measured at a fixed threshold. ToT follows a curve which increases monotonically with pulse-height for normal (no pile-up) pulses. Pile-up events exhibit longer ToT for a given pulse-height and follow a different curve enabling these to be discriminated using a 2D coincidence condition on amplitude and time [7]. The chip developed for this purpose also addresses the issue of multiplexing these analogue pulses into a shared ADC pair. This ASIC, known as SCEPTER (simultaneous capture of events with programmable timing and energy readout) provides both a sample-and-hold action to multiplex the analogue levels to one ADC for amplitude measurement and also produces a second analogue pulse with an amplitude proportional to ToT aimed at a second ADC. It can cope with up to 8 simultaneous events on the 32 input channels without loss. It also registers the channel address of the event. Data can be read out at a rate comparable to the average input rate; this implies a capability for acquisition of events at an average rate of up to 30 MHz, cumulative across the 32 inputs [7].

2.4. HYMOD parallel processor

Amplitude and ToT pulses are digitized using 12 fast 14-bit dual ADCs on an interface mezzanine board mounted on a HYMOD processor. HYMOD is a pipelined, parallel processing engine developed at the CSIRO for machine vision applications and applied here for real-time processing of detector events. The latest model, HYMOD2, features a 128-bit data interface, 166 MHz Xilinx Virtex 2-Pro field-programmable gate-array (FPGA) connected to 6 large static RAMs, 166 MHz Motorola PowerPC co-processor and ample fast serial (12×3.125 Gb/s) and Ethernet ports (2×1 Gb/s). In a multi-HYMOD configuration, the fast serial ports deliver data directly between the FPGAs without software overhead.

In the final detector concept, HYMOD performs pile-up rejection, energy calibration mapping and DA projection in the FPGA, with image accumulation in the conventional PowerPC CPU. It receives the real-time event stream through an optic fibre from a front-end data capture processor, which samples stage XY and controls and services the SCEPTER array and fast ADCs, which are local to the detector array. Image display and user control will be performed using software on a standard workstation linked to the HYMOD through a local-area network. Interaction with other beam-line equipment will be performed by the HYMOD board PowerPC acting as an EPICS node.

2.5. 3PL parallel language

Code for the HYMOD's FPGA is developed using a compiler called 3PL ('Parallel Pipeline Programming Language'). 3PL is the culmination of over a decade of CSIRO research in fine-grained massively parallel data processing. Parallel algorithms are encoded in 3PL and its compiler configures an FPGA into a single-purpose 'computer' to execute them. 3PL unlocks the inherent parallelism of FPGAs in several ways: (i) Thousands of arithmetic and logical operations may occur in parallel on each clock cycle. Independent parts of the program execute independently and are unaffected by processing 'load' elsewhere. (ii) Each operation occurs only when its input data are available. This applies to individual adds or multiplies right up to large processing blocks. Data 'flows' through the operation sequence with successive stages of the pipeline operating simultaneously on different data. (iii) The 'control logic' of the program executes in parallel with the data operations. There are no 'load', 'store', 'jump' or housekeeping instruction delays as suffered by conventional processors.

These aspects combine so an FPGA chip with modest clock rates can easily out-perform the latest multi-GHz conventional processors for many specific tasks. The 3PL language superficially resembles C, but its language compiler emits a netlist for the FPGA. Using the high-level language 3PL to implement parallel algorithms is enormously simpler than designing the hardware by means of current hardware description languages like VHDL or Verilog because 3PL automatically generates the tedious control logic for the program.

2.6. Spectrum deconvolution: Dynamic analysis

The *Dynamic Analysis* (DA) method builds a matrix transform to perform the task of spectral deconvolution of overlapping element spectra, including fluorescence lines and detector artefacts, such as tailing and escape peaks [1]. The method was originally developed at the CSIRO to project quantitative elemental images derived from proton induced X-ray emission (PIXE) data for trace element imaging using the CSIRO scanning nuclear microprobe (NMP) [8]. The technique is part of the *GeoPIXE* software system used in a number of NMP and synchrotron laboratories worldwide [9]. The DA method and GeoPIXE have been recently extended to handle Synchrotron X-ray Fluorescence (SXRF) data [10].

The *Dynamic Analysis* (DA) method lends itself to real-time processing of detected X-ray counts on an event-by-event basis. Each event is tagged by detector number and current XY position of the sample stage for imaging. The detector number is used to select the detector energy calibration to map the event onto the correct DA matrix column and these terms are accumulated into the image pixel selected by the associated XY tag. This close coupling of scan coordinates with data acquisition relaxes any constraints on dwell time per pixel, enabling high definition images to be collected. Image sizes of 500×500 pixels or more at dwells of ~1 ms or less are envisaged.

Progress in GeoPIXE and the DA method in the past 2 years has seen it adapted for SXRF and installed at the APS in sectors 2 (2-ID-E), 13 (GSE-CARS) and 20 (PNC-CAT), which now has full-spectral data acquisition needed by GeoPIXE and at the NSLS and CLS. An export option has been developed in GeoPIXE to export the DA transform matrix for use in real-time event-by-event processing. It also exports the energy calibration data for all elements of a detector array needed to map each event onto energy and DA matrix column.

2.7. 3PL/HYMOD implementation of DA

The DA method is well suited to parallel execution. The first stage in the processing pipeline filters out events whose time-over-threshold lie outside the limits for the particular energy. These limits are stored in look-up tables addressed by the energy value. The next stage corrects the energy for the particular detector. Again a look-up table is used, where the detector number and energy are used to address the memory in which the calibration table is stored. The processing pipeline then diverges into 20 parallel branches each of which accumulates concentration contributions for a specific element. In each branch the event energy is used as an address to the DA matrix look-up table which performs the deconvolution, the values from the table being accumulated over successive events on the current XY pixel.

Because the processing chain is a pipeline, successive stages can hold separate events and all stages in the pipeline can execute simultaneously. Thus the separate stages of pileup rejection, energy correction, 20 deconvolutions and 20 accumulations are all executed in parallel, with different events at different stages of the pipeline. The parallel implementation of DA requires just 208 lines of 3PL code.

3. Progress and results

Results reported for the monolithic detector array in 2003 indicated an energy resolution of 205 eV (Mn Kα using ^{55}Fe) at 10 KHz data rates, confirming the performance of the detector array and HERMES front-end [2,3]. This was improved over 2004 with 184 eV reported, cooled to $-26\,^{\circ}$C and using a peaking time of 4 μs (Fig. 1) [4]. A negative aspect of this spectrum is the poor peak-to-background ratio (~200). This is largely due to charge sharing between pixels, which gives rise to the incomplete charge collection feature in the spectrum - the long shelf-like tail. This is an important parameter in PIXE and SXRF as incomplete charge collection associated with intense major element lines (e.g. PIXE) and elastic/inelastic scatter peaks (SXRF) can seriously degrade detection sensitivities. The addition of the Mo mask helps control incomplete charge collection improving peak-to-background to greater than 1000 (Fig. 2) [4].

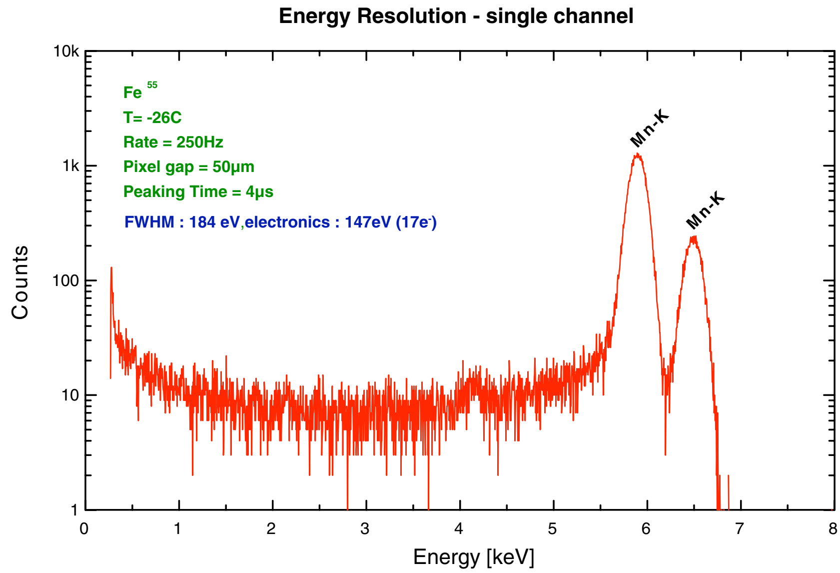

Fig. 1. ^{55}Fe test spectrum for one channel of the detector array, without an absorptive mask to combat charge-sharing between pixels. The peak-to-background is ~200.

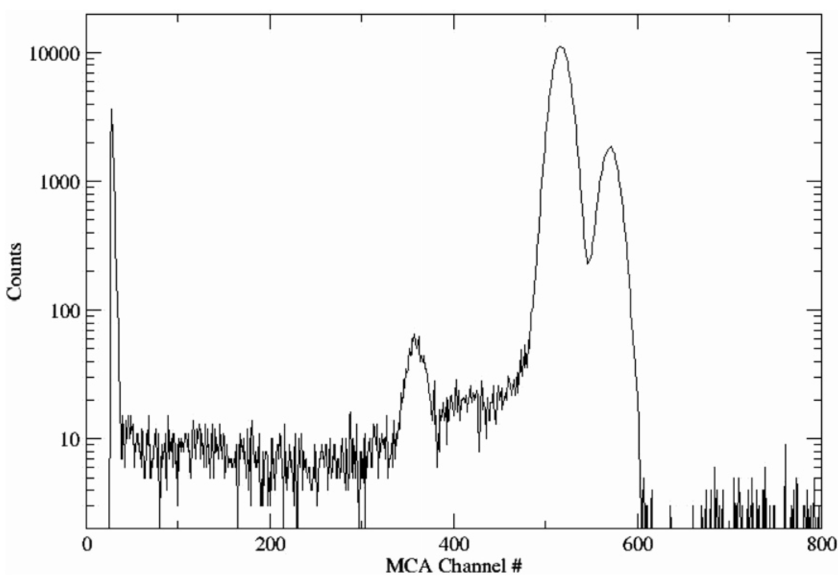

Fig. 2. ^{55}Fe test spectrum for one channel of the detector array, with a 125 µm Mo absorptive mask to combat charge-sharing between pixels. The peak-to-background is >1000.

The performance of SCEPTER was tested in an experiment using elastic scattering of a monochromatic 8 keV beam at the NSLS onto a 1×1 mm^2 silicon diode detector. Fig. 3 shows a biparametric plot of amplitude versus time-over-threshold (ToT) [7]. The locus of ToT versus E without pile-up is clearly seen, as well as the characteristic increased ToT for a given amplitude due to pile-up. Fig. 4 shows the corresponding spectrum without any correction (light-grey, or green in web version of article). The dark-grey spectrum (red in web version) corresponds to the biparametric coincidence selection set in Fig. 3. Despite a fairly loose biparametric coincidence selection, the dark-grey spectrum rejects the long pile-up tail that would otherwise degrade trace element detection limits.

Tests of the HYMOD processor as a platform for real-time detector data processing used a pair of HYMOD boards: one (#1) was configured to emulate the SCEPTER and fast ADC data source from a real detector and a second (#2) was configured with the 3PL/HYMOD implementation of DA outlined above, essentially as it would in the real detector system (Fig. 5). In a typical test, a full-spectral data-set, with the addition of simulated ToT, was compressed and loaded into the memory of HYMOD #1. It was then uncompressed and transmitted in real-time over the fast serial links to HYMOD #2 for processing.

Fig. 6 shows a test data-set of a fluid inclusion in quartz, collected on the 2-ID-E X-ray microprobe at the APS. The data-set contains 25 million events. Processing the data-set,

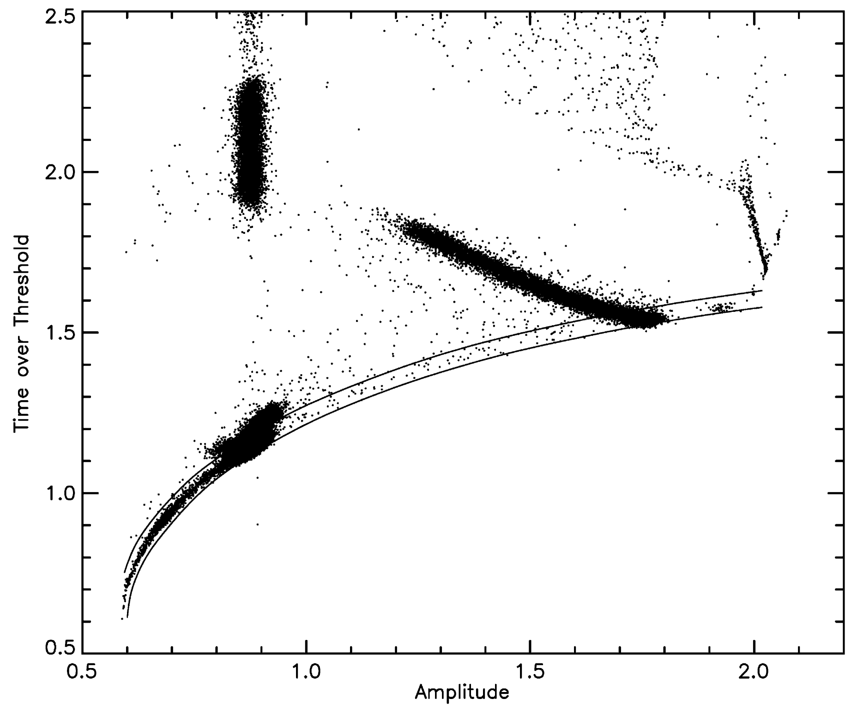

Fig. 3. Biparametric spectrum of time-over-threshold versus pulse amplitude for a monochromatic 8 keV X-ray beam at a count rate of 22 kHz. The lines mark the field that rejects pile-up.

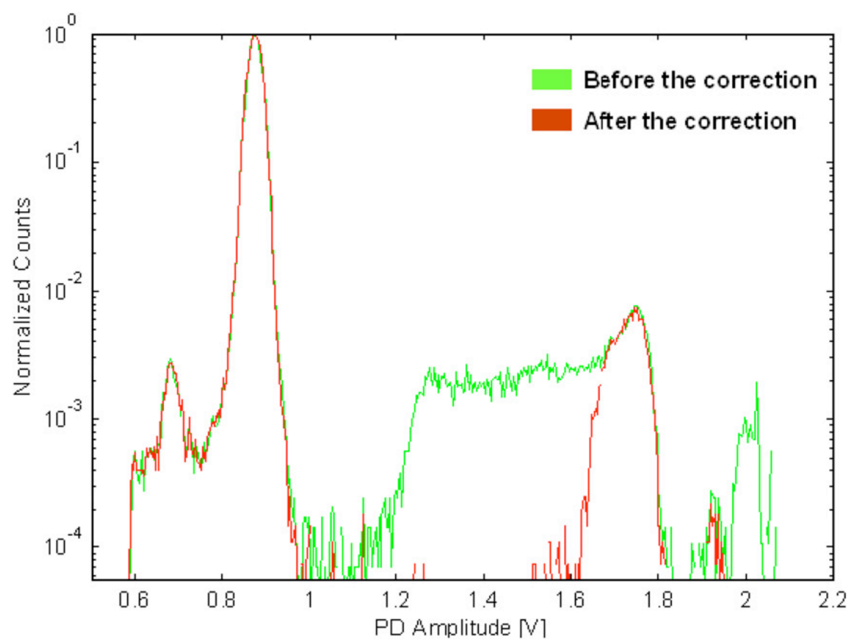

Fig. 4. Monochromatic 8 keV X-ray spectrum without (light-grey, or green in the web version of this article) and with (dark-grey, or red in web version) the application of the selection field shown in Fig. 3 to reject pile-up.

with deconvolution and projection onto 20 element images in real-time in HYMOD, is completed in 250 ms, giving a real-time processing speed of 10^8 events per second. This compares with the processing rate of a conventional detector array and processor of up to around 10^6 events per second.

The final link in the chain will be to complete the fast ADC interface between SCEPTER and HYMOD. A 32-channel prototype of the detector concept that combines all elements from detector array to HYMOD processor is under construction for testing at the NSLS synchrotron in August, 2006.

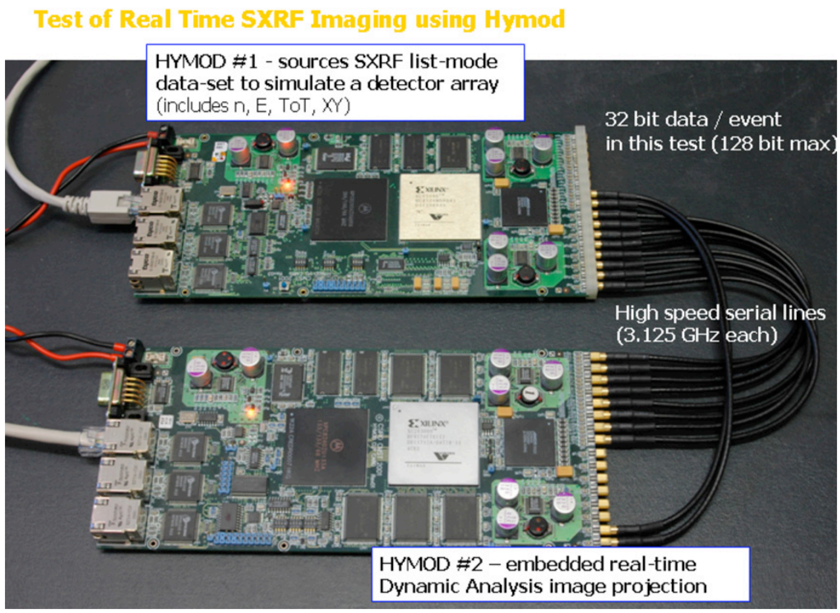

Fig. 5. HYMOD-based DA test unit. HYMOD #1 simulates a SCEPTER/ADC array and HYMOD #2 executes the 3PL/HYMOD implementation of DA at a processing speed of 10^8 events per second.

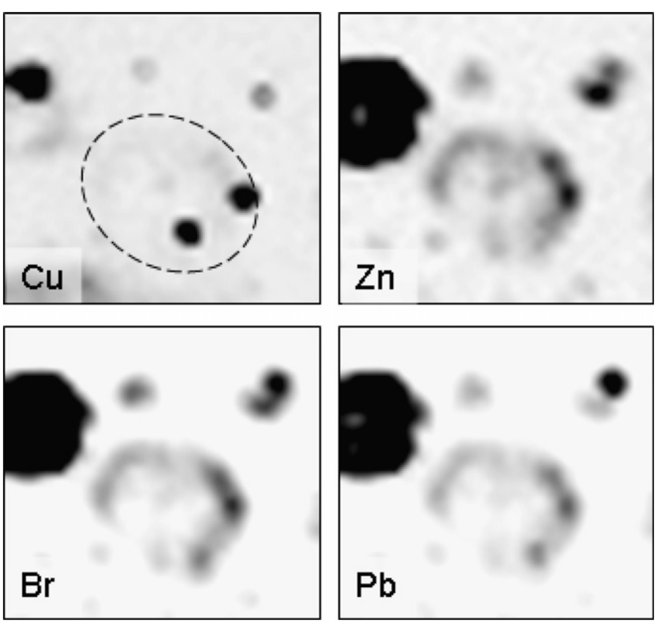

Fig. 6. Test full-spectral data-set (2.5 10^7 events) of a fluid inclusion in quartz collected on the 2-ID-E X-ray fluorescence microprobe at the APS.

4. Conclusions

All major sub-systems of a high performance spectroscopy detector system have been demonstrated. The detector array and analogue ASIC front end, show energy resolution at ∼184 eV (Mn Kα) and peak-to-background greater than 1000 using masking to reduce charge sharing. The new peak-detecting derandomizer ASIC (SCEPTER) provides a tool for pile-up rejection and acts as an analogue multiplexer and FIFO to simplify the ADC stage and interface to the HYMOD parallel processor, which has demonstrated its ability to perform real-time deconvolution and image projection at 10^8 events per second. And, HYMOD sampling of XY stage coordinates relaxes practical constraints on pixel advance rates.

A 32-channel prototype is nearing completion for testing of the complete detector concept at the NSLS. Once the concept is proved, construction effort will shift to a full 384 element system, aimed at synchrotron X-ray spectroscopy and proton microprobe applications, which in essence combines 12 of these 32-channel processing paths in parallel. The completed system offers the potential of 1–2 orders of magnitude increase in data rates in X-ray and proton microscopy, with full spectral deconvolution of elemental components, to realize a true elemental microscope, with interactive quantitative images available continuously to users.

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