A Low Cost, Highly Integrated 5.8 GHz Low-IF Transceiver for 1.5 Mbps Streaming Data Applications

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Abstract — **A highly integrated 5.8 GHz, SiGe BiCMOS transceiver IC has been developed for use in digital cordless phones, and streaming audio and video applications. The transceiver IC includes a double downconversion receiver, a direct upconversion transmitter, VCO / PLL / modulator, Low-IF filter, RSSI and demodulator. This IC has excellent performance with better than –100 dBm receive sensitivity and 0dBm transmit power output over 125MHz in the 5.8 GHz ISM band. This transceiver IC supports TDD, BFSK modulation at 1.536Mbits/sec**

Index Terms — **Transceiver, RFIC, upconverter, downconverter, VCO, PLL, modulator, demodulator, digital cordless phone**

I. Introduction

Two factors facilitated migration from the 900MHz to 2.4GHz ISM bands: the band became congested with a rapidly increasing number of devices [1], and the technology advanced so that low cost, highly integrated transceivers could be inexpensively produced in large volume. Today, the 2.4GHz ISM band is heavily congested with DCTs (digital cordless telephones), Bluetooth devices, 802.11b/g networks, and microwave ovens among others. This has encouraged communications equipment manufacturers to develop products using the 5.8GHz ISM band. Initial implementation of these devices is usually accomplished by up-conversion of an integrated 2.4GHz transceiver using a separate LO and mixer. This adds cost, complexity and system performance degradation as compared to a fully integrated solution. In addition, state-of-the-art IC process technologies utilizing low-cost SiGe BiCMOS process have enabled dramatic increases in operating speed allowing the development of highly integrated 5.8GHz transceivers. Previous work at 5.8GHz has predominantly been focused on WLAN applications [2]-[5]. The 5.8GHz ISM band transceiver presented here is a highly integrated device supporting TDD, BFSK modulation at 1.536Mbits/sec. It integrates:

- LNA.
- Dual conversion from RF to 1.024MHz IF.
- Calibrated channel selection filter.
- FM demodulator.
- Data slicer.
- RSSI.
- TX data shaping filter.
- Dual-port modulated Δ–Σ Fractional-N Synthesizer/VCO for BFSK TX data.
- Up converter of VCO to 5.8GHz.
- Baseband interface and control logic including PA control.

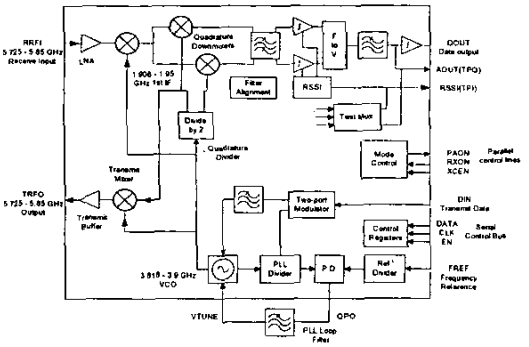

Figure 1: Block diagram of integrated 5.8GHz transceiver

This paper will present an overview of the transceiver architecture and discuss the performance that was achieved. The overall architecture of the transceiver is shown in Figure 1. The transceiver chip is realized on a SiGe BiCMOS process to achieve the low cost and high performance objectives. Figure 2 shows a photograph of the transceiver chip.

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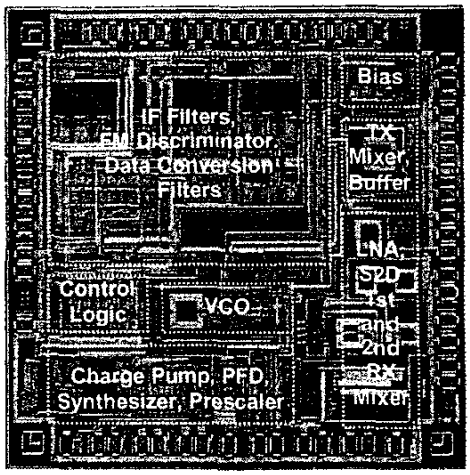

Figure 2: Photograph of transceiver die.

II. Receiver

The receiver has a dual-conversion super heterodyne architecture, with a high 1st IF (1.95GHz) and a low 2nd IF (1.024MHz) to reduce image-filtering requirements. A cascode LNA is integrated on-chip, as shown in Figure 3 resulting in a receiver sensitivity of better than –100dBm at 1.536Mbps and 12.5% BER. A majority of the circuitry in the receive path is implemented differentially to increase noise immunity and isolation, both of which are increasingly difficult problems at 5.8GHz. The first down mixer converts the signal to 1.95GHz. The second stage converts the signal to 1.024MHz and provides an I/Q output. The low-IF is filtered using an auto-calibrated, active polyphase filter to perform channel selection and image rejection. This signal is passed through a set of limiting amplifiers that simultaneously produces a RSSI signal. For larger input signals, 20dB of attenuation is added to the receive path to increase the dynamic range of the receiver. The limited signal is passed through a frequency to voltage converter to linearly demodulate the BFSK data. A 768 KHz low-pass filter removes any high frequency content from the received data before processing the data by an on-chip data slicer producing a NRZ output for the baseband chip.

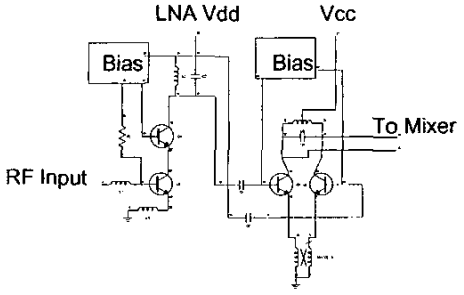

Figure 3: Simplified LNA - S2D schematic

III. Transmitter

The BFSK modulation is accomplished with two paths in the frequency synthesizer. The first is a fast analog modulation path that scales the logic-level input data, and filters it with a low-pass filter. The low-pass filter is tuned to give a 1.4MHz nominal 3dB bandwidth point to optimally shape the output spectrum for 1.536Mbits/s data. This filter feeds the internal modulation port of the VCO tank circuit providing ±341.33kHz deviation. The same input data also has a slower path that is limited by PLL loop filter bandwidth. It merges the instantaneous data value with the PLL programming to adjust the division frequency between the VCO and the phase comparator. This scheme assures that the frequency deviation will be maintained independently of the DC content of the input data. The data modulated on the VCO nominally at 3.9GHz is then mixed with itself divided by two to produce the 5.8GHz output with 512 kHz deviation. Finally the output is amplified resulting in a 0dBm output. The RF transmit chain of the ML5800 transceiver IC consists of an up convert mixer and a buffer stage to provide output power at 5.8GHz. The mixer consists of a

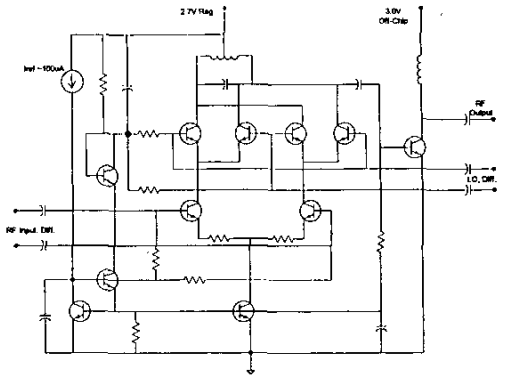

Figure 4: Simplified schematic of the transmit mixer

differential pair "Gilbert Cell" which is followed by a single stage common emitter amplifier as shown in Figure 4. The 1.95GHz LO frequency is obtained by dividing the 3.9GHz IF frequency by two. The up conversion process uses low side LO mixing, and the sum components of the two frequencies is retained by the tuning tank at the inter-stage between the mixer and the buffer amplifier. The tank serves multiple purposes and is one of the most critical parts in the design of the transmitter chain.

The transmit chain is also designed to suppress unwanted spurious emissions to meet radiated output power requirement. The mixer design uses BJT devices, and contains 30-Ohm resistive emitter degeneration at the gm stage to accommodate the high voltage swing coming out of the VCO. It draws 10mA from a 2.7V on-chip regulated supply and has 6dB of conversion gain with an IF output of 200mV peak. The output buffer after the mixer draws 12mA and uses an off-chip unregulated supply thru an RF choke. It is a single stage common emitter BJT and provides an additional power gain of 15dB. It has an off-chip matching network, which matches the output impedance to 50-Ohm load and also provides additional spurious filtering. One of the main challenges was providing the appropriate output impedance to the buffer amplifier, including package parasitics, so that off chip matching is possible. At 5.8GHz, package pins and bond wires inductances make it difficult to match the device output. Designing an off chip matching network using surface mount components is also challenging. The divide by two part of the transmit chain is a simple

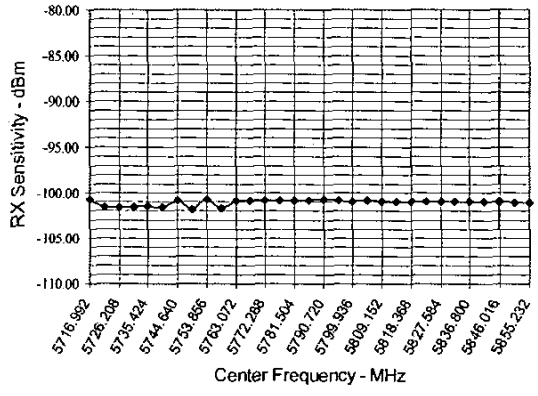

Figure 5: Receiver sensitivity vs. frequency

D-flip-flop implemented with differential pair BJT's. All the circuits are biased with reference PTAT currents for gain stability over temperature.

IV. Synthesizer

The LO, shared between the transmitter and receiver, is a second-order Σ–Δ fractional-*N* PLL operating at a nominal frequency of 3.9GHz derived from a 6.144MHz input reference. The 2:3 ratio between VCO frequency and transmitter output greatly reduces VCO pulling by the transmitter output. The prescaler used in the PLL is a divide by 16/16-½ design implemented using a phase shifter and the quadrature division of the VCO output. This scheme effectively doubles the update rate of the loop as compared to a more traditional divide by 16/17 scheme[6] resulting in lower phase noise. The necessary frequency resolution of the synthesizer is 341.33Khz requiring a modest fractionalization of nine thereby reducing the amount of logic required for the Σ–Δ modulator. The VCO's tuning sensitivity and VCO modulation port sensitivity varies by 3:1 over the wide tuning range of the transceiver. First-order compensation for these variations is included in the PLL charge pump and modulation port driver. Using a simple external second order loop filter, locking times on the order of 60us have been achieved.

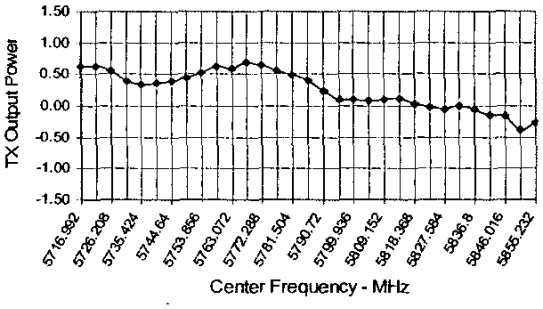

Figure 6: Transceiver output power vs. frequency

V. Baseband Interface

The baseband interface of the 5.8GHz transceiver is compatible with existing 900MHz and 2.4GHz transceivers. The interface consists of a three-wire serial port to configure the transceiver, and two mode control inputs. The mode control signals consist of an enable signal, which places the transceiver in a

low-current consumption state, and transmit/receive control. Additional outputs are provided for transmit power control and external PA sequencing. When the transceiver is switched from transmit to receive or the chip is taken out of the power down state, the IF filters are automatically calibrated by injecting a calibration tone into the IF circuitry.

VI. Results

Figure 2 shows the completed die that was subsequently assembled and tested in a 32-pin package. The die size is 2.56 x 2.60mm. Figures 5 and 6 show the overall chip receiver and transmitter measured performance as a function of operating frequency. The receiver shows better than -100dBm sensitivity, thus meeting the design requirements. The transmitter performance shows better than -2.5dBm power output over the full 5.8GHz frequency band. The operating currents were measured to be less than 1μA in standby mode, 70mA in receive mode, and 60mA in transmit mode. Table 1 summarizes the measured results. The transceiver performs well over the commercial temperature range.

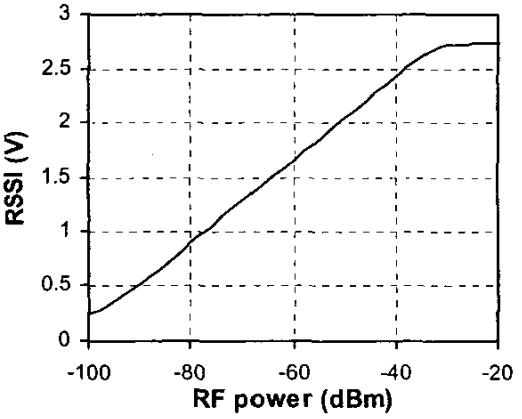

Figure 7: shows the RSSI performance and demonstrates the dynamic range of the receiver.

Thousands of transceiver ICs from several different wafer runs have been tested on ATE and bench test setups. The measured data agrees with simulation and meets the high performance and yield expectations.

Table 1. Measured Results and Specifications

Sensitivity at 12.5%BER	-101dBm
Sensitivity at 0.1%BER	-94dBm
Frequency Range	5.725 -5.850GHz
Data Rate	1.536Mbps
Transmit Output Power	0dBm
Supply Voltage	2.7 - 3.6V
Receive Supply Current	67mA
Transmit Supply Current	60mA
Die size	6.7mm^2
Package	32LPCC5x5

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