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SOME CONSIDERATIONS ON TUNNELING LOSSES IN FIELD-EFFECT DEVICES FOR LOW-VOLTAGE MICROCONTROLLERS

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The loss power density associated with the tunneling current in a typical MOS cell with a floating gate is evaluated for high electric-field strengths in the oxide layer. Furthermore, problems related to oxide thickness are discussed.

Keywords: Loss power density; tunneling current; MOS cell; oxide thickness

1. INTRODUCTION

The tunneling current in MOS cells for low-voltage microcontrollers based upon EEPROM plays a crucial role in understanding the physical electronics of those field-effect devices. The above current is very sensitive to the thickness of the oxide layer in a given MOS cell because the electric field in this layer depends on the above thickness and the current depends strongly on the electric-field strength [1–4].

On the other hand, it is important to recall that Al-SiO_2-Si devices with floating gate will be considered. In effect, these devices are the crucial elements in low-voltage microcontrollers based on EEPROM. These devices have two gates: the control gate and the floating gate [1–4]. When the drain voltage is reduced from 5 V to 3 V, the corresponding charge pump output voltage also decreases [2, 3]; consequently, the control gate voltage becomes smaller. This fact

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implies a decreasing of the voltage drop across the tunnel oxide [2, 3]. The diminished tunneling of carriers onto the floating gate originates a slow erase operation giving rise to EEPROM fallout [2, 3].

In the following, we will consider n-channel devices and we will study the loss power density associated with the tunneling current for relatively high electric-field strengths in the oxide layer. At this point, we can claim that the oxide thickness plays a significant role; in fact, some problems related to this parameter will be discussed very briefly.

2. THEORETICAL FORMULATION

The magnitude of the tunneling current density in question obeys the following relationship [1 – 5]:

$$J = \frac{e^3 E^2 m_0 E_g^{-3/2}}{16\pi^2 \hbar m_n^*} \exp\left[-\frac{4(2m_n^* E_g^3)^{1/2}}{3e\hbar E} \right] \tag{1}$$

where e is the electron charge, E is the magnitude of the electric-field strength in the oxide layer of the n-channel MOS considered, m_0 is the electron rest-mass, m_n^* is the tunneling electron effective mass, $\hbar$ is the reduced Planck constant and E_g is the barrier height of Si and SiO_2 at cathode side.

If E is sufficiently high, the exponential in Eq. (1) approaches unity and we can conserve the preexponential term so that we can write:

$$J \approx e^3 E^2 E_g^{-3/2} / (16\pi^2 \hbar) \tag{2}$$

since $m_n^* \approx 1.1\, m_0$ (silicon).

On the other hand, the associated power density (W/m^3) is given by $P = JE$ so that by virtue of Eq. (2) we have:

$$P \approx \frac{e^3 E^3 E_g^{-3/2}}{16\pi^2 \hbar} \tag{3}$$

Since $E = V_{ox}/t_{ox}$ (where V_{ox} is the voltage drop across the tunnel oxide and t_{ox} is the oxide thickness), formula (3) is a good approximation because, in practice, t_{ox} must be small (typically

$t_{ox} \approx 100$ Å; see, for example, Ref. [6]) so that E becomes high. Then, from Eq. (3) it follows:

$$P \approx \frac{e^3 V_{ox}^3 E_g^{-3/2}}{16\pi^2 \hbar t_{ox}^3} \tag{4}$$

that is to say, if t_{ox} is sufficiently small, tunneling losses per unit volume are inversely proportional to t_{ox}^3.

On the other hand, by taking into account that V_{ox} decreases when the drain voltage is reduced from 5 V to 3 V (see the introduction of this paper), then E is not too high and, as a consequence, formula (3) is not applicable. Certainly, decreasing of V_{ox} and a relatively small value of t_{ox} produce a moderate value of E; for a discussion on values of t_{ox}, see Refs. [2, 6]. At any rate, optimization of the tunnel oxide thickness constitutes a crucial problem. Variation in critical dimension on this thickness influences the so-called erase coupling ratio and program coupling ratio which determine the voltage induced onto the floating gate from the control gate and the drain, respectively [2]; these ratios are used to evaluate EEPROM cells [2]. In particular, the erase coupling ratio, that is, the fraction of the control gate voltage induced onto the floating gate is [2]:

$$R_e = C_{fc}/C \tag{5}$$

since [2]:

$$\frac{C_{fc}}{C} = \frac{V_{fg}}{V_{cg}} \tag{6}$$

where C is the total capacitance on the floating gate which is given by:

$$C = C_s + C_{fc} + C_{fs} + C_d \tag{7}$$

where C_s is the capacitance of the floating gate to the source, C_{fc} is the capacitance of the floating gate to the control gate, C_{fs} is the capacitance of the floating gate to the substrate, and C_d is the capacitance of the floating gate to the drain. On the other hand, V_{fg} is the floating gate voltage and V_{cg} is the control gate voltage which is induced onto the floating gate during the erase operation.

With respect to the program coupling ratio, R_P, we have [2]:

$$R_P = C_d/C \tag{8}$$

Also we have [2]:

$$\frac{V_{\mathrm{fg}}}{V_{\mathrm{d}}} = \frac{C_{\mathrm{d}}}{C} \tag{9}$$

where V_{d} is the drain voltage. From formulae (8) and (9) it follows:

$$R_P = \frac{V_{\mathrm{fg}}}{V_{\mathrm{d}}} \tag{10}$$

Finally, by virtue of Eq. (4) and by the fact that both C_{d} and C_{fc} are inversely proportional to t_{ox}, it follows that P is approximately proportional, on the one hand, to C_{d}^3 and, on the other hand, to C_{fc}^3 when t_{ox} is sufficiently small.

3. CONCLUDING REMARKS

Formula (4) in conjunction with the considerations associated with the capacitances involved in the above exposition, may be considered as the nucleus of the paper. On the other hand, we wish to remark that our formulation can be used to understand the problems related to the electrical parameters of the 5 V and 3 V microcontrollers with EEPROM of Motorola; these problems have been reported in Ref. [2] and their relation to the tunnel oxide thickness constitutes a crucial question.

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