Power Integrity Characterization and Correlation of 3D Package Systems Using On-Chip Measurements

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***Abstract*—System power integrity characterization for low-power high-speed memory interface in a 3D package system is a challenging task due to probing difficulties imposed by small form factor. In this paper, power integrity measurements including supply noise, PSIJ sensitivity and PDN impedance curve using on-chip noise generator and monitors are presented. On-chip measurement data are validated by off-chip sense line measurements. Good correlations between simulation and measurements close the loop between analysis and verification for the system power supply delivery design.**

Keywords-power integrity, PDN characterizatin, PDN correlation, supply jitter sensitivity, on-chip measurements, power supply noise

I. INTRODUCTION

It's challenging to design a clean power supply for low-power high-speed mobile memory interface. As the ever increasing bandwidth requirements from mobile applications such as HD video streaming, data rate of I/O interface keeps increasing to multi gigahertz range. Although mobile devices usually use low power design, it runs at low voltage supply that has small voltage margin. Mobile applications often require constant power mode shifts which cause big noise during the power mode transition. However, low latency requirements such as fast wakeup require the devices to transact before the supply noise settles down. Thus it's crucial to characterize the whole system power supply and accurately account the power-supply-induced-jitter (PSIJ) to satisfy a tight timing budget.

Mobile systems often uses 3D package such as Package-on-Package (PoP), Multichip Package (MCP) and System-in-Chip (SIP) due to their small form factor. The compact 3D geometry poses several difficulties. First, it limits pin count and results in high signal to power ratio. This causes bigger loop inductance, which causes bigger dI/dt noise, and also limits possibility of placing test pads. Second, there are tight couplings between supply rails, which pose big transfer noise. Third, characterization becomes difficult. Sense line probing needs extra pads, and have on-chip IR drop issue caused by the distance between the probed location (often at high metal layer) and the real circuit supply (at the gates and diffusions). Probing at package pin and PCB connector often has big distortion from on-chip supplies because of coupling and reflection issues. Thus on-chip measurements provide clean solution for in situ power measurements. The compact self-contained on–chip module is detached from the regular chip thus eliminates interference. They can be placed at close to where the circuit is to measures the real power supply seen by the circuit. Input and output for the module are digital signals, thus it eliminates the signal integrity problems. Furthermore, unlike external probing need to be placed at each location for each rail, these on-chip modules can share inputs and outputs, and can also be multiplexed with other control signals.

This paper presents on-chip techniques for power integrity measurements including supply noise, PSIJ sensitivity as well as PDN impedance profile. The measurements were taken on a test vehicle built on two die stacked PoP system as shown in Fig 1 for low power high speed memory interface [1]. Section II reviews the on-chip measurement circuit and techniques, section III describes the modeling and simulation methodology, and section IV presents the set up and procedures for all the measurements. Finally, sense line probing validated the on-chip measurements results, and correlations between measurements and simulations close the loop of power design analysis and verification.

II. ON-CHIP MEASUREMENT CIRCUIT AND TECHNIQUES

In the past, various on-chip supply techniques have been developed. Some method observes over- and under-shoot events over certain time window [3], some reconstructs repetitive noise in sub-sampling scope mode [4]. However neither of them covers a very high bandwidth to ensure stringent power requirements. In [5], an efficient and accurate on-chip supply noise characterization method and measurement circuits were presented. In this test vehicle, the test chip has improved the on chip circuits to achieve higher frequency range and better accuracy to enhance the usability of this circuit [6].

Each on-chip measurement module is made up of one noise generator and two noise monitors, as shown in Fig 2. The noise generator is a series of controllable current source [x1, x2, x4, x8] connected to power supply, as depicted in Fig. 3. The amplitude is controlled through the registers n_vdd[0..3], and the frequency is controlled by the signal NCLK. When NCLK is set as a clock signal, the resulting current is also a clock-shaped signal, with the same fundamental frequency.

The two noise monitors are identical. Each monitor includes a sample-and-hold (S/H) circuit as the sensing front-end, a ring type VCO as the voltage-to-frequency converter and a digital counter ADC, as shown in Fig. 4. The digital counts

are stored in the registers, and read out through the registers. The mapping relationship between the real voltage and register count is established through a procedure called "DC calibration".

Only one monitor is required to capture the time-domain supply waveform. This can be used to measure supply dynamic change, such as intentional injected noise and self generated noise, including read-to-write-to-read transactions and power mode shifts etc. For a system with a clock rate at 3.2GHz, beyond 10GHz measurement is required to ensure signal integrity. In this test chip implementation, several techniques were combined to achieve high bandwidth. In the S/H block, PMOS switches were used as samplers and ring-type VCOs were used in hold mode. PMOS switches were convenient to measure VDD supply, and the simple design ensured their ability to achieve high frequency. A ring-oscillator was used because it can easily achieve several times of FO4 time to obtain high bandwidth. The output of the VCO was the input to a 16-bit counter. The counters were enabled in the same time window as the hold circuit, and the rising edges of the oscillations were counted. Thus, the higher counts reflect higher frequency, which was controlled by higher voltage. Thus a final relationship between digital counts vs. voltage level could be established. So, this design mitigates complexity of outputting the high frequency signal directly.

Many circuits have frequency dependent behavior, so it's desirable to reveal more frequency domain noise insights, such as PSD distribution and PSIJ-sensitivity profile. Typical supply noise can be characterized as cyclo-stationary random process. Hence the obtained auto correlation can be used to describe many statistical aspects of the circuits. To obtain auto correlation of the two measurements, the two monitors were simultaneously operated, controlled by two clocks with the same frequency, with a precisely controlled delay. Details will be described later.

PDN impedance profile is another desired design parameter. Knowledge of this parameter can help trade off and optimize power system design among circuits, package and PCB. Because voltage is a simple product of impedance and current, thus impedance over frequency can be derived by the ratio of *v(f)* over *i(f)*. Noise monitor can clearly identify each voltage frequency component, however obtaining the current amount over frequency is not as easy. In [7] periodical sinusoidal square current waveforms were obtained using combined clock groups running at different cycle times. With the on-chip measurement hardware, noise generator can be used to obtain on-chip current. Set the regular chip at sleep mode to minimize background noise and interference, while keep the detached on-chip measurement circuits at running. NCLK is set as a clock, and swept over the target frequency range. By controlling registers n_vdd[0..3], certain amount of current is injected into the system, and then noise monitor is used to measure noise at that particular frequency. NCLK controls the transistor gates, thus the induced drain current has the same fundamental frequency and their harmonics. The current amplitude could be obtained from the circuit design team, also can be obtained by measuring the difference of current flowing into the PDN between the sleep mode and after the injection. VRM module often provides sensing resistors and can read their voltage drop to derive the whole current flowing through the VRM thus the whole PDN. If this can't be accessed, some board level modification can be done to allow the measurement. Although the current has multi tones, not the single fundamental frequency as preferred, most of the energy were still captured at this basic frequency, and thus could be used as a very good approximation. In the test vehicle, this measured current amount was also compared with the circuit designer's own estimation and approved the assumption. The derived decap amount from the PDN impedance curve matched very well with the circuit implementation, this also proves the validity of the current amount approximation.

III. PDN MODELING

The power delivery is essentially made up of VRM, PCB, 3D package and on-chip power grid. Paper [2] describes the details of how to model the system power delivery, and this paper adopts the same procedure. PCB is modeled as RLC unit-cells in arrays, including the decoupling capacitors placed at the right locations. 3D package uses PEEC models, with the parameter extracted from 3D field solver such as Ansoft Q3D because there is no predetermined ground return path for many of the power traces and wire bonds. On-chip power grid uses the lumped RC models. All the models were stitched together and system level simulations were run using HSPICE in both frequency domain and time domain. Good correlations with measurements prove the validity of the modeling methodology.

In order to accommodate simulation capacity and efficiency, some model-order-reduction (MOR) is done. MOR also revealed insights of the system power modeling by extracting out the dominant parameters for system behavior. Optimization for performance could also be exercised for future system enhancement.

In this particular POP test vehicle, Controller and DRAM share the same regulator and are tied at PCB. Thus there are two resonant frequencies for each device. Depending on probing from DRAM or Controller, the two resonant peaks shift around, determined by effective package inductance and on chip decoupling capacitance. After the peaking range, the descending slope is determined by the on-chip decoupling capacitance amount, which is the same for the two chips in the system. Both phenomena were nicely captured using the modeling methodology and measurement procedure, and they have a very good correlation as shown in Fig. 5.

IV. MEASUREMENT SETUP AND CUSTOMIZED FLOWS

Fig. 6 shows one example measurement setup for PSIJ-sensitivity measurements. All control signals of NCLK, VCLK1 and VCLK2 are set as external clocks. NCLK set the frequency point for measurement, and was swept over the target range. VCLK1 and VCLK2 were also clock signal set at a different frequency, which determined the accuracy, with varying delay τ, which set the Nyquist frequency of this measurement.

Noise generator strength is controlled through registers n_vdd[0..3], and noise monitors results are read out through registers CNT1 and CNT2. This whole module is self

contained, and can be detached from the regular chip operation. This nice feature ensures minimum system back ground noise possible.

Digital codes in CNT1 and CNT2 are mapped to real voltage numbers through a procedure called "DC calibration". This DC calibration is obtained by sweeping the supply rail DC voltage, and recording the digital counts. DC voltage can be set through either external supply or VRM. At each preset DC value, multiple measurements should be taken, and the average value should be used in order to eliminate randomness. Usually the two monitor designs are identical, thus the DC calibration curve only has slight difference.

While two monitors are used simultaneously, the frequency domain noise aspects can be extracted through auto correlation. The measurement is to set VCLK1 and VCLK2 at the same frequency, and precisely control the delay τ. The auto-correlation can be calculated as:

$$R(\tau) = E\{[V_{dd}(t)][V_{dd}(t+\tau)]\} \quad (1)$$

Power-Spectral-Density (PSD) can be derived as:

$$S_{vdd}(f) = \int_{-\infty}^{+\infty} R_{vdd}(\tau) \cdot e^{-j2\pi f\tau} \cdot d\tau \quad (2)$$

From PSD values, noise amplitude can be further derived:

$$V_{dd}(f) = \sqrt{2 \cdot S_{vdd}(f)} \quad (3)$$

In order to correlate the noise monitor frequency domain measurements, sense line measurements under the same system condition were also taken and compared against each other. Fig. 7 shows a good correlation for the noise monitor measurements and the sense line measurements, which greatly boosts the confidence of the measurement methodology.

An example of the time-domain power supply measurement is during the power mode transition. When power mode changes from idle mode to full activity, all IO driver circuits and the clock circuits start to sink current, and this sudden current load change causes big ringing. Because a typical PDN impedance curve peaks at the mid-frequency range, although the sinking current did not necessarily have the biggest component at that peaking frequency, the resulting noise still peaks at that mid-frequency point. This means the ringing dies out in multi clock cycles, and this places constraints on how fast the system can wake up. The simulation used the correlated PDN models, and obtained the realistic current waveform from circuit group. The results of the time domain simulation correlated well with the time domain measurements, as shown in Fig. 8. Except the ringing present in both power modes, the transitional waveform correlates very well.

PSIJ-sensitivity curve is a circuit characteristic, not altered by system operation or noise level. Fig. 6 demonstrates the set up of this measurement. The system is operated in a certain mode, such as continuous read with PRBS7 data pattern. Then set NCLK to be a desired frequency and inject certain amount of current into the PDN, use two noise monitors to measure the noise spike designated as *v(f)*. Connect data output to a real time scope, record the data jitter frequency *j(f)* using the scope's embedded jitter software. When the noise amount is in a design allowed strength range, jitter is nicely responding to injected noise at a fixed coefficient. This ratio is taken as the jitter sensitivity:

$$PSIJ\ senseivity(f) = j(f)/v(f)\ (ps/mV) \quad (4)$$

In order to further improve accuracy, at one frequency point, two measurements can be performed and their average is taken.

In the test chip measurements, three process corners depicted as FF, TT and SS are measured, and each corner has two samples. As shown in Fig. 9, there are distinctive differences across the three corners, however variation in each corner is negligible. As predicted, FF corner has the best PSIJ sensitivity, and SS corner has the worst one. The peaking frequency and value and the slope rate matches the simulation very well.

As shown before in the PDN modeling section, great correlation results of PDN impedance was achieved. In order to further improve measurement accuracy, at each frequency point, two measurements with different strength are taken, and impedance is derived as

$$z(f) = \frac{\Delta v(f)}{\Delta i(f)} = \frac{v_2(f) - v_1(f)}{i_2(f) - i_1(f)} \quad (5)$$

When PDN profile is obtained, the descending slope after the resonant peak is determined by the on chip decaps. Through some simple math, the decap amount could be derived. The measured decap amount achieved within 5% error with APACHE ACE extraction of this test chip. Vice versa, when current amount is very hard to measure, the known decap amount can be used to calibrate the PDN curve.

V. CONCLUSION

On-chip techniques for power integrity characterization including supply noise, PSIJ sensitivity as well as PDN impedance profile have been presented. Measurements results on a low power high speed mobile memory interface have been shown, and good correlations have been achieved between simulation and measurements, thus close the loop between design analysis and verification.

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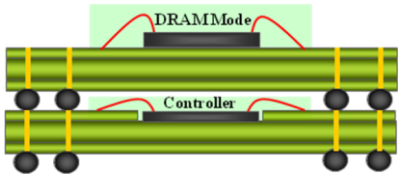

Figure 1. Test vehilecle POP package illustration

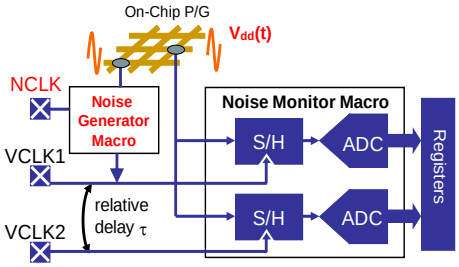

Figure 2. On-chip power measurement module hardware schematic

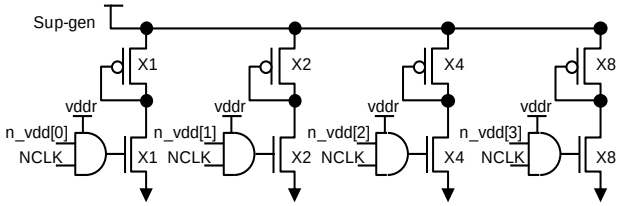

Figure 3. On-chip noise generator schematic

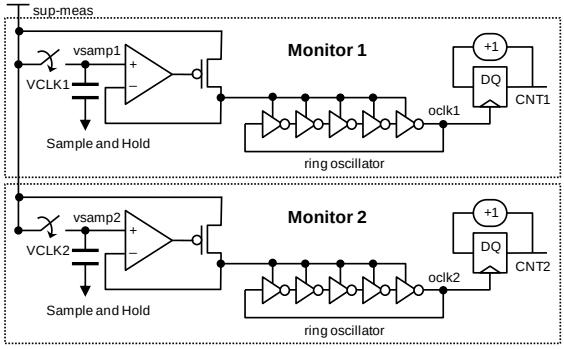

Figure 4. On-chip noise monitor schematic

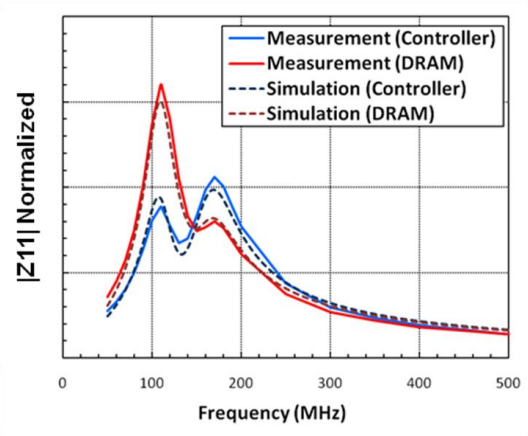

Figure 5. Controller and DRAM PDN impedance curves

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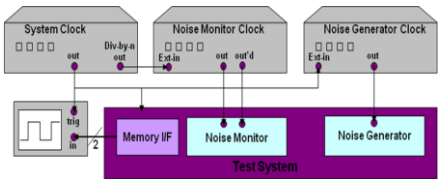

Figure 6. PSIJ-sensitivity measurement setup

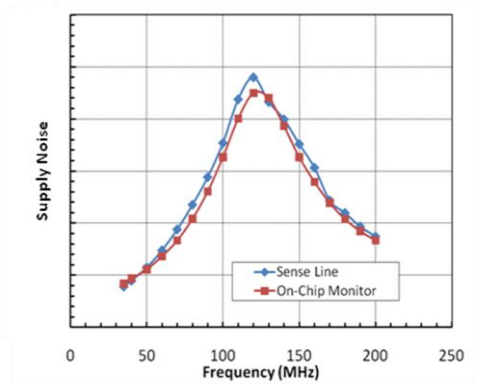

Figure 7. On-chip noise monitor measurements correlation with senseline measurements under noise injection

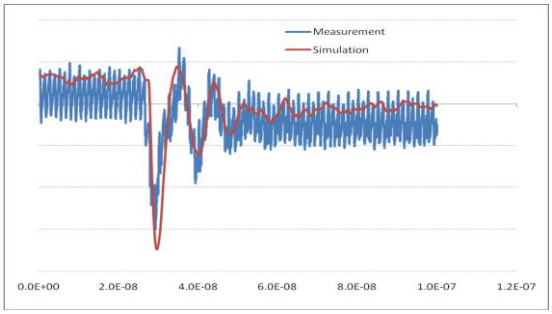

Figure 8. Measurement vs. simulation for controller power mode transistion from idle to active

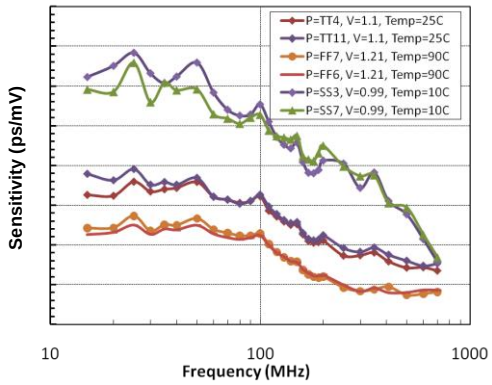

Figure 9. PSIJ-sensitivity results across chip design corners