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Efficient Multi-Standard Software Defined Radio receivers implementation using Frequency response masking

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ABSTRACT

The compatibility of the filter bank with different communication standards requires dynamic reconfigurability. The polyphase channelizer has the advantage that the channel filter can be adjusted to better approximate the ideal magnitude response.Hanning Window functions can also be used to improve the side lobe response without any of the performance penalties associated with the FFT channelizer. The proposed FB offers reconfigurability at the architectural level and at the channel filter level and is capable of extracting channels of nonuniform bandwidths corresponding to multiple wireless communication standard from the digitized wideband input signal.

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INTRODUCTION

Wide band architectures are also useful in a number of niche applications for military and civil defense, including signals intelligence and electronic warfare. The ability to support multiple communications channels per RF band is a fundamental process for many software defined radio platforms. Non-uniform channelization accounts for a significant portion of the digital signal processing workload in the base station receiver and can be difficult to realize in a physical implementation. Channels within the frequency band are dynamically allocated to the radio standards.

A key element of the wideband receiver architecture is the channelization technique that is used to isolate the independent communication channels contained within the wideband signal. On the receiver side, the channelizes extracts the channels of interest from the digitized RF bands, and then forwards these channels on to channel processing for demodulation and decoding. This paper will compare and contrast three of the more popular channelization techniques: Digital down Conversion, Frequency Domain Filtering, and Polyphase FFT Filter Banks. Digital-Down Converters (DDCs) have become a cornerstone technology in communication systems.

Apart from low complexity reconfigurability is another key requirement of channel filters in SDRs because the filter specifications change in accordance to the selected communication mode. The frequency response masking and coefficient decimation techniques can be implemented with a Polyphase Filter to improve the reconfigurability and reduce the Hardware complexity. This can be developed in LABVIEW with its flexible components and implemented in the hardware for testing and can be developed as a standalone effective wideband receiver for software defined radio applications.

Software Defined Radio:

Software-defined radios (SDRs) are adaptable transceiver systems that learn and adapt to transmission and channel environments with software. A key element of an SDR architecture is the channelizer, which is used to isolate independent communication channels within a wideband signal. A channelizer needs to support multiple channel processing elements, wherein the channels of interest can be extracted and then forwarded on for demodulation and decoding.

There are three predominant channelization architectures used in SDR designs. These include digital down conversion (DDC), frequency domain filtering, and polyphase Fast Fourier transform (FFT) filter banks.

The polyphase FFT filter bank is the most efficient choice because it assumes redundancy within the frequency of the wideband channel. This structure makes use of a polyphase filter to isolate and decimate the

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various channels and then employs an FFT to efficiently convert each channel to baseband. Although this technique is limited to channel structures consisting of equally spaced channels, it requires only a single fast impulse response (FIR) filtering structure and an FFT, which increases its efficiency.

Proposed work:

The frequency response masking and coefficient decimation techniques can be implemented with a Polyphase Filter to improve the reconfigurability and reduce the Hardware complexity. This can be developed in LABVIEW with its flexible components and implemented in the hardware for testing and can be developed as a standalone effective wideband receiver for software defined radio applications.

Furthermore this technique generates linear phase FIR filters, which have advantages such as guaranteed stability and are free of phase distortion. However, usually the problem with FIR filters is the high complexity for sharp filters therefore the frequency-response masking technique results in filters with very sparse coefficients. Since only a very small fraction of its coefficient values are nonzero, its complexity is very much lower than the infinite wordlength minimax optimum filter [J.Mitola, 2000.]. With an additional multiplierless design method the complexity can be reduced to a minimum.

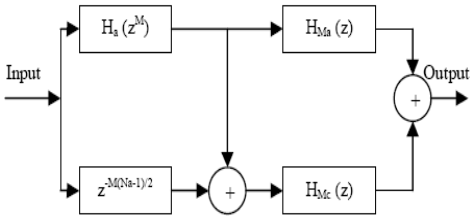


Fig. 1: FIR filters architecture based on FRM technique.

Frequency response masking technique:

Reconfigurability of the receiver must be accomplished in such a way that the filter bank architecture serving the current communications standard must be reconfigured with least possible overhead to support a new communication standard while maintaining the parallel operation .To realize a filter bank which can be reconfigured to accommodate multiple standards with reduced hardware overhead, we have proposed a frequency response masking (FRM) based reconfigurable filter bank (FRMFB).The FRM technique was originally proposed for designing application-specific low complexity sharp transition-band finite impulse response FIR filters.

FRM approach is to achieve following advantages:

(1) Incorporate reconfigurability at the filter level and architectural level,
(2) Improve the speed of filtering operation
(3) Reduce the complexity.

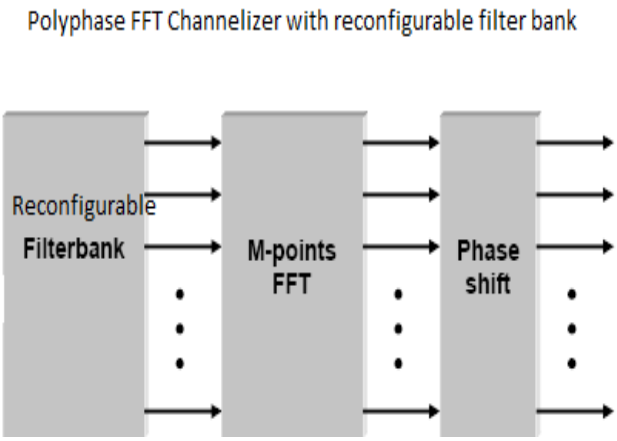


Fig. 2: Polyphase FFT channelizer with reconfigurable filter bank.

Polyphase FFT:

Switching between filterbank techniques can meet the required bandwidth channels for multiple wireless communication standards from the digitized wideband input signal. The polyphase FFT filter bank channelizer improves upon the efficiency of the frequency domain filtering technique by assuming redundancy within the

frequency plan of the wideband signal. The polyphase filter is created through the decomposition of low pass filter used to provide channel isolation on a per channel basis.

- Channel filter response can be adjusted.
- Degrade the side lobe performance.
- Filtering performance adaptation.

The FFT-summation and polyphase-FFT techniques are both very effective in improving several aspects of signal detection performance over the simple FFT filter bank.

Coefficient decimation filter:

Coefficient decimation is the technique to implement reconfigurable FIR filters. It is based on decimating or interpolating a fixed set of impulse response coefficients. Here different frequency responses are obtained by without changing the coefficient values. Interpolating the impulse response results in a compression of the frequency response. However, decimating it will deteriorate the frequency response to possibly break the specifications. The resulting filter coefficients can decrease the filter order required for a given approximation error in the reconfiguration modes.

System configuration:
LABVIEW 2010
ELVIS DAQ

Application:

Military and civil defense, Signals intelligence and electronic warfare and FM receiver.

System implementation:

1) Coefficients Decimation filter
2) Frequency Response Masking
3) Switching between the filter banks according to the multi standard with non uniform channel bandwidth
4) Polyphase FFT

Reconfigurability:

The complexity of an FIR filter is dominated by the number of adders needed to realize the coefficient multiplication operation. In this section, we are comparing the number of adders required to realize the channel filters for D-AMPS and PDC standards for our proposed architecture with the reconfigurable BSE method in [R. Mahesh and A. P. Vinod, 2006.] and a reconfigurable CSD-CSE method designed by us based on algorithm proposed in (R.I. Hartley, 1996).

Architecture Level Reconfigurability

The architectural reconfigurability of the channel filter can be illustrated using a dual-mode channelizer.Let *fp1* and *fp2* be the passband and *fs1* and *fs2* the stopband frequencies of the channel filters corresponding to two standards of operation respectively. Reconfigurability can be achieved by using the same subfilters in Figure 1 for both the standards. The parameters *fap* and *fas* remains unchanged for both the standards (same modal filter being employed for both standards) and the masking filters, being implemented using LUTs, can be reconfigured by just swapping the LUT values.

The basic idea behind the FRM technique is to compose the overall sharp transition-band filter using several wide transition-band subfilters (M. M. Peiro, E. I. Boemo, and L. Wanhammar, 2002). Given a prototype symmetrical impulse response linear phase low-pass filter $H_a(z)$ of odd length *Na*, its complementary filter $H_c(z)$ can be expressed as

$$H_c(z)=z^{-M\frac{(Na-1)}{2}}-H_a(z) \quad (1)$$

Replacing each delay elements of both filters by M delays, two filters with transfer functions $H_a(z^M)$ and $H_c(z^M)$ are formed. The transition widths of $H_a(z^M)$ and $H_c(z^M)$ are a factor of M narrower than that of $H_a(z)$. In the FRM technique, two filters $H_{Ma}(z)$ and $H_{MC}(z)$, are cascaded to $H_a(z^M)$ and $H_c(z^M)$, respectively as shown in Figure 1. The transfer function of the entire filter is given by

$$H(z)= H_a(z^M)\, H_{Ma}(z)+ H_c(z^M)\, H_{MC}(z) \quad (2)$$

Note that the group delay of the filters $H_{Ma}(z)$ and $H_{Mc}(z)$ must be equal, and M(Na-1) in the equation (2) must be an even number. The basic architecture of the proposed channel filter is same as in Figure 1. The masking filters are generally of very low order and hence can be implemented completely using look up table (LUT) without employing any hardware multipliers. As hardware multipliers are not used, our architecture results in significant power reduction. The proposed multi-standard channel filter offers reconfigurability in two levels, namely architecture level and filter level.

$$m = \lfloor f_p M \rfloor, f_{ap} = f_p M - m, f_{as} = f_s M - m, f_{map} = f_p,$$

$$f_{mas} = \frac{m + 2 - f_{as}}{M}, f_{mcp} = \frac{m - f_{ap}}{M} \text{ and } f_{mcs} = f_s \tag{3}$$

where *M* is the up-sampling rate for *Ha(z)*, *fp* and *fs* are the passband and stopband edges of the overall filter, *fap* and *fas* are the passband and stopband edges of the modal filter *Ha(z)*, *fmap* and *fmcp* are the passband edges and *fmas* and *fmcs* are the stopband edges of the two masking filters respectively. Thus by suitable selection of the passband and stopband edges of the modal and the masking filters, any sharp transition band

FIR filter can be implemented with minimum complexity.

Design Results:

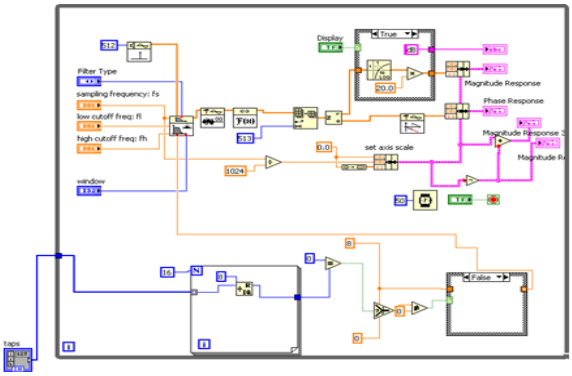
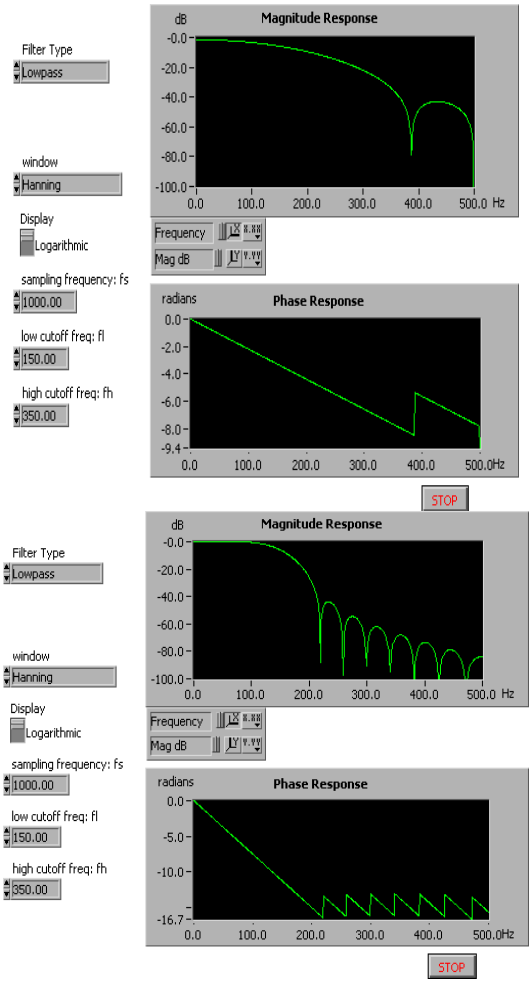


Fig. 3: Coefficient decimation filter bank.



Conclusion:

The basic idea is to keep every M^{th} coefficient of an FIR filter unchanged and replace all other coefficients by zero to obtain multiple frequency band at integer multiples of 2π /M.The Resulting reconfigurable architecture can extract the narrow band channels of non uniform bandwidth in very low complexity. The DDC offers excellent flexibility with the user able to select the bandwidth and centre frequency of a channel with high level of resolution. Architectures such as these are a cost effective solution for down-conversion in multi-channel digital receivers, and represent a critical building block for flexible software defined radios of the future.

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