# Modeling of Advanced Memories

A. Makarov, S. Selberherr, and V. Sverdlov
Institute for Microelectronics, TU Wien, Gusshausstraße 27-29/E360, A-1040 Wien, Austria
Email: {makarov|selberherr|sverdlov}@iue.tuwien.ac.at

***Abstract* — Results of modeling of advanced memories, such as one-transistor/no capacitor random access memory (Z-RAM), Resistive RAM (RRAM), and Spin Transfer Torque Magnetic RAM (STTRAM), are presented.**

Memory is an indispensible important component of any modern integrated circuit. While MOSFET scaling has reached tremendous advances, semiconductor memory scaling is lagging behind. Standard DRAM cell scaling is hampered by the presence of a capacitor which is difficult to reduce in size. Z-RAM uses a bitcell composed of a single transistor without a capacitor (1T/0C) ("Z" stands for Zero capacitor), unlike traditional one transistor plus one capacitor (1T/1C) DRAM bitcells. The advanced Z-RAM bitcells built on a multiple-gate MOSFET (MuGFET), where the parasitic bipolar transistor [1] is utilized, which exists in SOI MOSFETs. The current flows through the body of the structure and is thus much increased. The majority carriers generated due to impact ionization are stored under the gates. The stored charge offers a good control over the current. The threshold voltage is modified by the stored charge guaranteeing two states of the bipolar transistor with high and low current, correspondingly. The stored charge for the two states is shown in Fig.1. Fig.2 demonstrates the excellent scalability of a Z-RAM bitcell based on a MuGFET with the 10nm thin body [2]. The use of vertical gate-all around transistors extends the Z-RAM roadmap to future generations.

Charge-based memories including flash are, however, gradually approaching the physical limits of scalability, and the search for new nonvolatile memory concepts has significantly accelerated. Several new memory structures as potential substitutes of the flash memory were invented and developed: a technology of phase change RAM (PCRAM), spin transfer torque RAM (STTRAM), carbon nanotube RAM (NRAM), copper bridge RAM (CBRAM), racetrack memory, and resistive RAM (RRAM). A new type of nonvolatile memory must exhibit low operating voltages, low power consumption, high operation speed, long retention time, high endurance, simple structure, and small size.

One of the most promising candidates for future universal memory is the resistive random access memory (RRAM) [1]. It is based on new materials, such as metal oxides and perovskite oxides. This type of memory is characterized by high density, excellent scalability, low operating voltages (<2V), fast switching times (<10ns), and long retention time. We developed a stochastic model of the bipolar resistive switching mechanism based on electron hopping between the oxygen vacancies along the conductive filament (CF) in an oxide layer. The CF is formed by localized oxygen vacancies ($V_o$) [3] or domains of $V_o$ (Fig. 3). Formation and rupture of a CF is due to a redox reaction in the oxide layer under a voltage bias. The hysteresis cycle modeled with the model is shown in Fig.4 [4].

The spin transfer torque random access memory (STTRAM) is another promising candidate for future universal memory. The reduction of the current density required for switching and the increase of the switching speed are among the most important challenges in this area. A decrease in the critical current density for the penta-layer magnetic tunnel junction was reported in [5]. By numerically investigating the dynamics (Fig.5) of the switching process in a junction composed of five layers we present the methodology on how to reduce the switching time by using a composite soft layer (Fig.6)[6].

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## References

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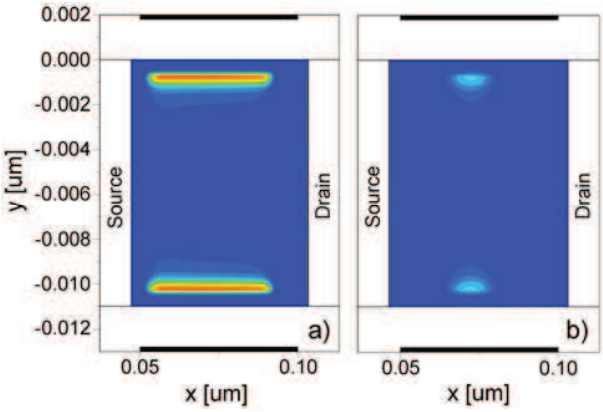


Fig. 1. Simulated hole concentration along the fin in states "1" (a) and "0" (b) for a 50-nm Z-RAM device.

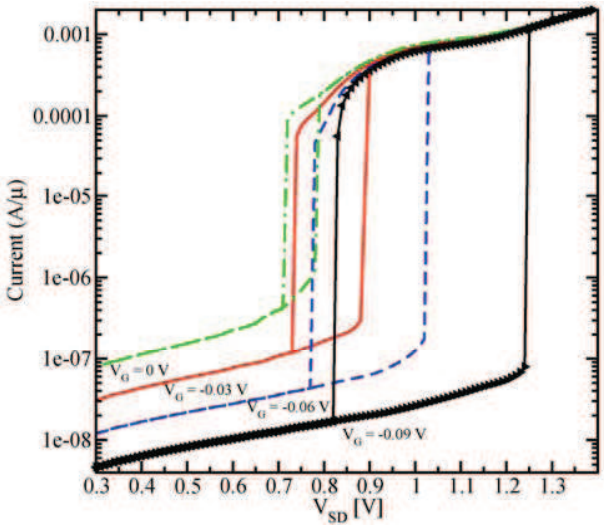


Fig. 2. Simulated hysteresis for a 50-nm Z-RAM device.

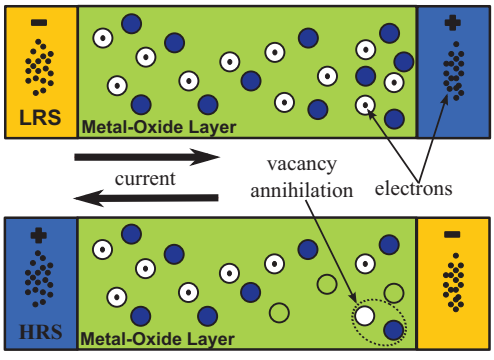


Fig. 3. Schematic illustration of the conducting filament in the low resistance state (top) and the high resistance state(bottom).

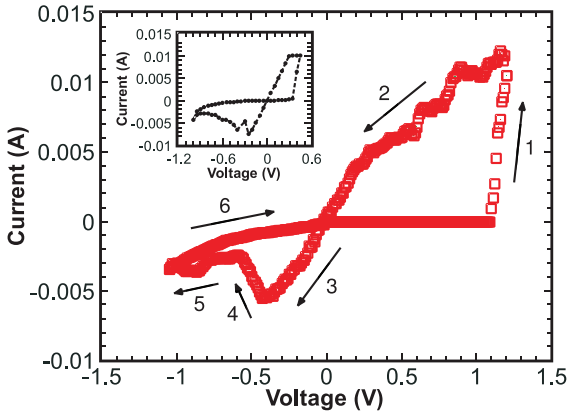


Fig. 4 *I-V* characteristics showing the hysteresis cycle obtained from the stochastic model. Inset: hysteresis for *M*-$Cu_xO$-*M* .

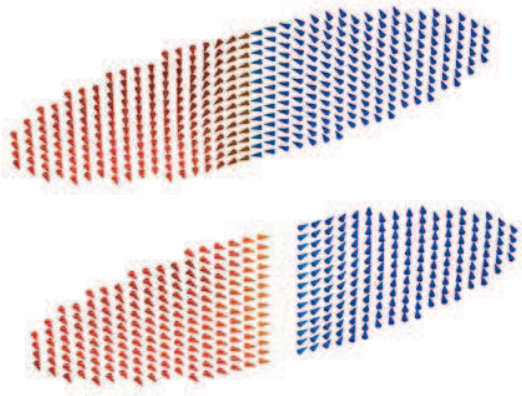

Fig. 5. Snapshots of the magnetostatic exchange field for the standardat (top) and composite (bottom free magnetic layer.

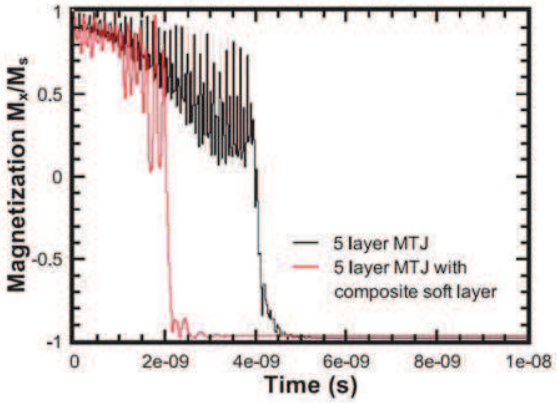


Fig. 6. Magnetization evolution in the free magnetic layer. Faster switching is predicted for the composite layer.