A 1ps-Resolution Integrator-Based Time-to-Digital Converter Using a SAR-ADC in 90nm CMOS

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***Abstract*—We propose a time-to-digital converter (TDC) that uses a G_m-C integrator to translate the time interval into voltage, and quantizes this voltage with a SAR-ADC. The proposed method is capable of achieving pico-second resolution, avoiding limitations in delay-chain-based TDCs, such as limited resolution to the buffer delay, mismatches, and voltage surge. Furthermore, taking the advantages of SAR-ADC, small area and low power consumption of voltage quantization are attainable. The chip was fabricated in 90nm CMOS. Its measured DNL and INL are -0.6/0.7 LSB and -1.1/2.3 LSB, respectively, with 1ps per LSB in a 9-bit range.**

I. INTRODUCTION

Recently, time-to-digital converters (TDC) have been increasingly demanded in clock generators, ADCs, on-chip jitter measurement, and time-of-flight (TOF) meters. The last ones are used for industrial, medical and entertainment applications such as laser rangefinder, nuclear experiments, and 2D/3D imaging systems. The time resolution of a TDC is a key factor for the measurement accuracy. For example, in a laser rangefinder, a 1mm precision requires 6.7ps minimum resolvable time. In a TOF imaging system for medical applications, a high resolution TDC enhances the contrast of the generated image.

The delay-chain TDC has been conventionally used due to its simple implementation. However, its time resolution is limited to a buffer propagation delay (around 20ps in 90nm CMOS), unsatisfying advanced applications. To enhance the resolution, a Vernier chain TDC can be employed where the resolution becomes the subtraction of two buffer delays. In this architecture, a DLL calibration loop is typically used for global calibrations against PVT variations [2]. This incurs more area and power consumption and the resolution is still limited to the mismatches buffers at each stage. A pipeline TDC has been proposed by using time amplifiers (TA) to amplify the time residue for further quantization in the following stages [3]. High resolution and long range can be available but the nonlinearity and mismatches of TAs require tough calibration effort. A stochastic TDC utilizing the process variations of arbiters to accumulate a transfer function achieves high resolution but its detectable range is inherently

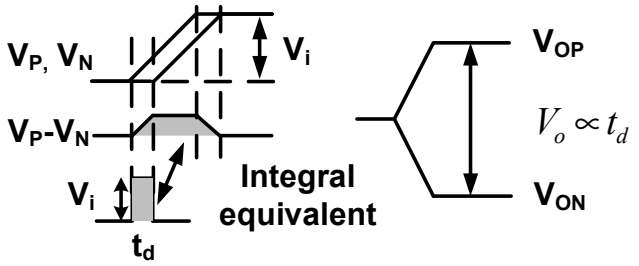


Figure. 1 Concept of the integrator-based TDC. The time difference t_d is propotional to the integration of the voltage difference. The integrated voltage V_o can be digitized by an ADC.

short and its resolution is dependent on the technology used [4]. A Delta-sigma TDC utilizing oversampling and noise-shaping enhances the resolution. However, the signal bandwidth is low (no more than 3MHz) and the resolution is limited by the oversampling ratio (OSR) [5].

Prior to the solutions that are discussed above, a noticeable type of TDCs was once realized with a constant current charging a capacitor followed by an ADC. Theoretically, these integrator-based TDCs can achieve high resolution by increasing the current, reducing the capacitance, or increasing the resolution of the ADC. In the past, however, the latter two approaches were impractical when implementing on integrated circuits (IC) due to the low density of capacitors, and the unreasonably large power and area consumptions of an ADC, such as pipeline, flash and delta-sigma. Hence, on-chip solutions typically employed a dual-slope-counter with large capacitors, where area, resolution, and bandwidth were limited [1].

In this paper, we solve these issues through designing a successive-approximation-register (SAR)-ADC featuring low power consumption and small area occupation. We propose an architecture for a high resolution TDC, using a G_m-C integrator followed by a SAR-ADC. Metal-oxide-metal (MOM) capacitors are implemented so that relative small capacitors are available. With the small capacitors, a conventional integrator using switched current sources can

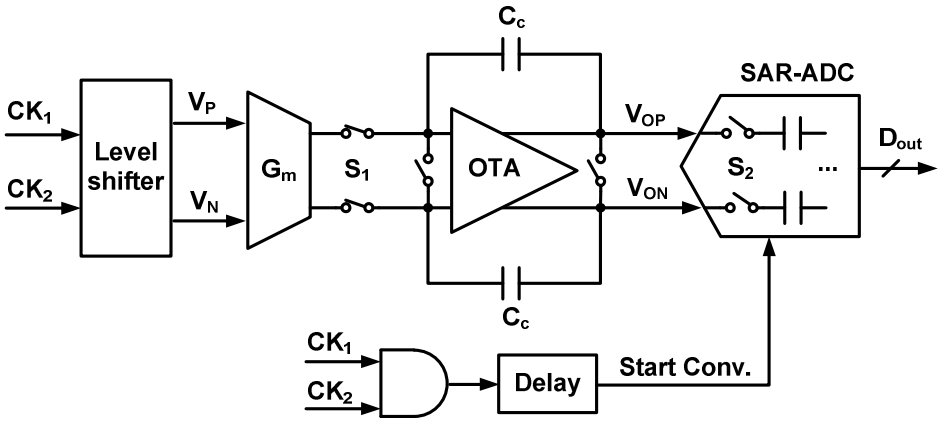


Figure. 2 Architecture of proposed integrator-based TDC.

suffer charge injection, charge sharing, and clock feed-through. Moreover, the dead-zone and the discontinuity of the switching operation can also cause error charges. Thus, we designed a continuous-time fully differential G_m-C integrator where the integration is not controlled by switches.

II. INTEGRATOR-BASED TDC

The concept of the proposed integrator-based TDC is shown in Fig. 1. The integrator receives two input signals, V_P and V_N, with a delay, t_d, and certain transition slopes. The integral of the subtraction of V_P and V_N, i.e. the area of the shadow, is equivalent to the area of a rectangular, as shown in Fig. 1. Thus, we have (1), where V_i equals the amplitude of the input signals.

$$\int (V_P - V_N)dt = V_i \cdot t_d \tag{1}$$

By using a fully differential G_m-C integrator, we can have (2) and (3), where I_c, G_m, C_c, and V_o are the differential charging current, the transconductance, the loading capacitor, and the differential output voltage that can be digitized by an ADC, respectively. The time resolution is derived in (3), where t_{res} and V_{LSB} stand for time and voltage resolutions, respectively. Equation (3) is the basic for designing the proposed high resolution TDC where limitations in delay-chain-based TDC do not exist.

$$V_i \cdot t_d = \frac{I_c t_d}{G_m} = \frac{C_c V_o}{G_m} \tag{2}$$

$$t_{res} = \frac{C_c V_{LSB}}{G_m V_i} \tag{3}$$

The architecture of our proposal is shown in Fig. 2. A level shifter is interfaced to the G_m cell to let it work in the saturation region. An OTA is used as a miller amplifier to increase the linearity and the dynamic range. A self-clocked SAR-ADC starts the conversion after the integration. Fig. 3 shows the timing diagram of the operation of the proposed TDC. The level shifter shifts the input digital levels to proper values, with a small amplitude to ensure the enough linearity of the G_m cell, without changing the time interval. Since only the differential input is integrated, the integration stops when

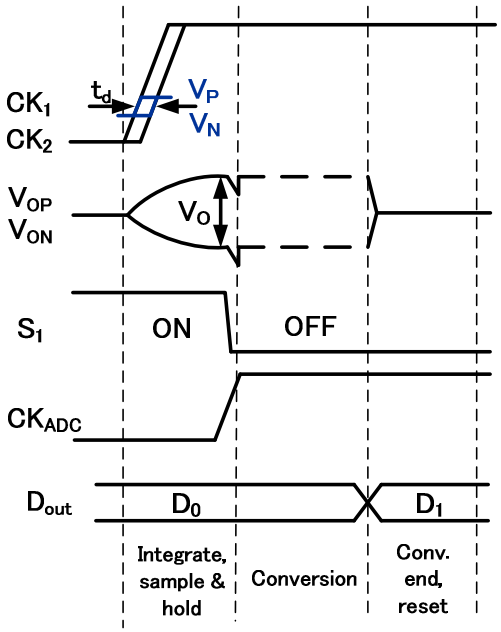


Figure. 3 Timing diagram.

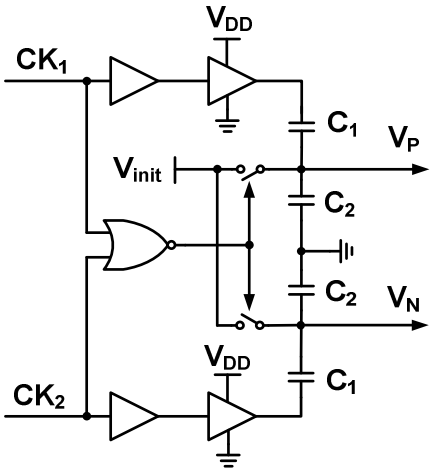


Figure. 4 Capacitive level shifter.

both CK_1 and CK_2 reach high level. After the voltages settled on C_c, S_1 is off, and S_2 is on. Since the feedback still overrides the OTA, and the current path from the G_m cell to C_c is cut off, the output voltage will be held and copied to the sampling capacitors of the SAR-ADC. Then the conversion starts and ends, followed by the data output and reset of the integrator.

III. Circuits Design

A. Level Shifter

A capacitive level shifter without static current flowing has been designed, as shown in Fig. 4. Before the rising of digital inputs CK_1 and CK_2, V_P and V_N are preset to an initial voltage, V_{init}. V_P and V_N transit by the amplitude V_i during the transitions of CK_1 and CK_2. V_i is calculated using (4), where V_{DD} is the power supply voltage. When both CK_1 and CK_2 fall down, the V_P and V_N are reset to V_{init}.

$$V_i = \frac{C_1}{C_1 + C_2} V_{DD} \tag{4}$$

B. G_m-C Integrator

A conventional G_m cell and a gain-boosted folded-cascade OTA have been designed, as shown in Fig. 5. In the G_m cell, source degeneration and a relatively large ($V_{gs} - V_{th}$) are used to increase the linearity. Since V_P and V_N transit at different time, unbalanced input feed-through and kick-back charges can cause minor errors at the input. Neutralizion transistors are used to alleviate this effect. Cascode current source is employed for a higher common-mode rejection ratio (CMRR). The feedback on the OTA suppresses the output voltage of the G_m cell and copies its current to integrate on C_c. Boosting OTAs in folded-cascode structure are used for a high DC-gain against the current leakage during the integration. C_c is small (450fF for each) for high resolution. As mentioned above, only differential input is integrated so that the integration stops when V_P and V_N reach the same value. By doing this, no switches are involved for the integration so that errors caused by the switches, such as dead-zone, charge sharing, and charge injection, are also avoided.

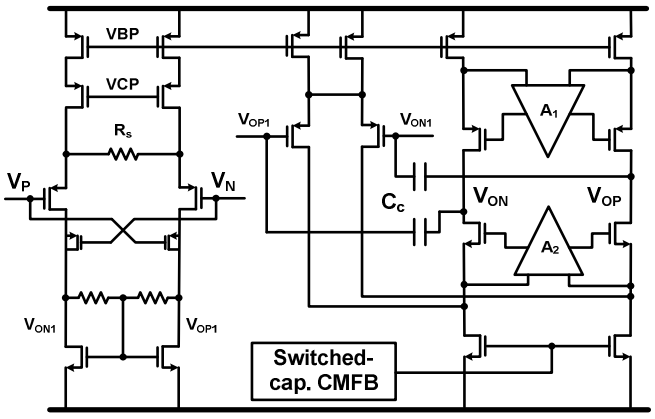


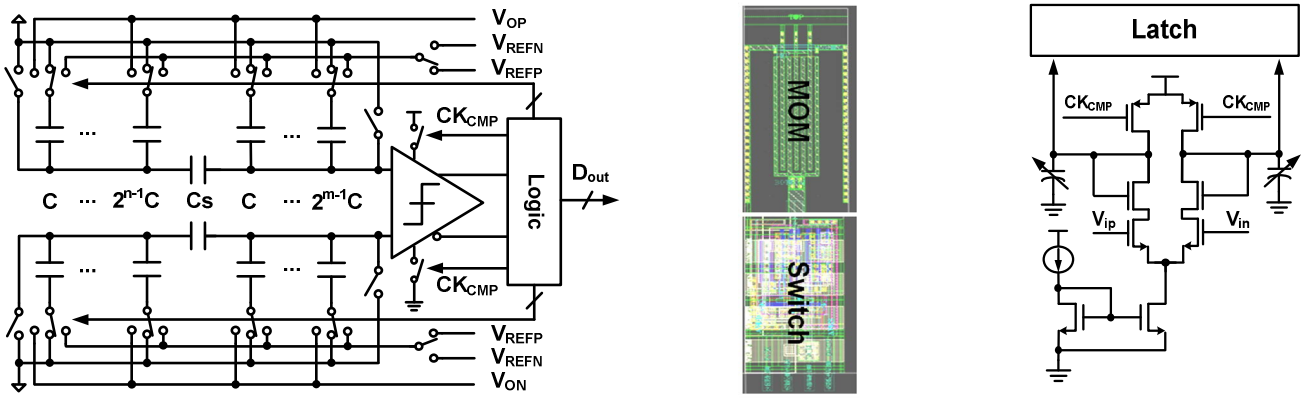
Figure. 5 G_m-C integrator.

C. SAR-ADC

Compared with other types of ADCs, a SAR-ADC features compact structure, small area, and low power consumption since only one CDAC is used for sample-and-hold and quantization, as well as one comparator, as shown in Fig. 6 (a). MOM capacitors are implemented taking its merit of high density and non-special process, comparing with metal-insulator-metal (MIM) capacitors [7]. Furthermore, attributed to the finger-type structure, a MOM capacitor is easy to be scaled like a CMOS transistor. Consequently, same pitches of capacitor and switch can be made and scaled with the number of fingers, which enhances the matching of the CDAC. The layout of the capacitor-switch unit with 15fF unit capacitance is shown in Fig. 6 (b).

Small total capacitance also reduces dynamic power consumption. Moreover, a dynamic comparator is introduced without static current flowing, as shown in Fig. 6 (c). Unlike [6], the tail current is used for higher CMRR but still operates dynamically. Therefore, the entire SAR-ADC only consumes dynamic power which is scalable with the clock frequency.

IV. Measurement Results



(a) (b) (c)

Figure. 6 (a) Topology of the SAR-ADC. (b) Capacitor-switch unit. (c) Topology of the dynamic comparator

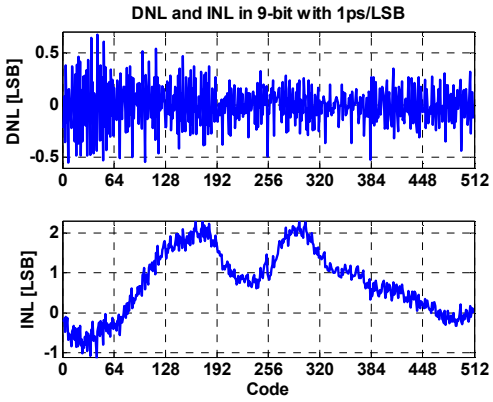


Figure. 7 Measured DNL and INL.

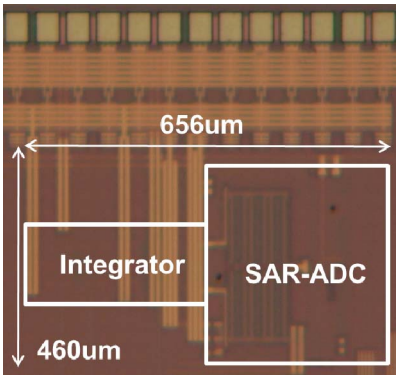


Figure. 8 Chip photo.

A prototype IC has been fabricated in 90nm CMOS using standard process. The core areas of the OTA and the SAR-ADC are 0.06mm^2 and 0.15mm^2, respectively. The SAR-ADC is with 12-bit topology achieving 9.8-bit effective number of bits (ENOB). If an actual 10-bit SAR-ADC is designed, the area of the SAR-ADC can be reduced to around 1/8. With 10MHz input clocks and 1.2V power supply, the current consumption is 17mA where the SAR-ADC consumes 0.83mA. Most current is consumed by the integrator due to the conventional topology but the major goal of this work is to demonstrate this architecture with a SAR-ADC. The power consumption can be significantly reduced by improving the design of the integrator.

To measure the DNL and INL, two frequencies with nominal 40Hz difference are input to the TDC, creating time ramps. The 10-bit output data are recorded by a logic analyzer. The histogram method was used to evaluate the DNL and INL. The result in the middle 9-bit is plotted in Fig. 7, where DNL and INL are -0.6/0.7 LSB and -1.1/2.3 LSB, respectively, with 1ps per LSB. Note that the result was obtained without any calibration on the integrator or the SAR-ADC. Comparing with some recent works, such as [3], this architecture relieves the calibration effort. Finally, the chip photo is shown in Fig. 8, and the performance comparison is listed in Table I.

V. Conclusion

TABLE I. Performance Comparison

	[2]	[3]	[4]	**This work**
Type	Vernier	Pipeline	Stochastic	Integrator
CMOS [nm]	130	130	65	90
Supply [V]	3.3	1.3	1.2	1.2
Resolution [ps]	37.5	0.63	3	**1**
Range [ps]	2000	1300	52	±256
DNL [LSB]	0.2	0.5	1.4	0.7
INL [LSB]	0.35	2	1.5	2.3
Area [mm^2]	0.22	0.32	0.04	0.31
Frequency [MS/s]	0.1	65	40	10
Power [mW]	150	10.5	8	20.4

We have proposed an architecture of the integrator-based TDC using a G_m-C integrator followed by a SAR-ADC, proving its capability of achieving high time resolution using the charge domain quantization. Although an ADC is introduced, the conventional area and power issues are solved by designing a SAR-ADC with small MOM capacitors and a dynamic comparator. The measured DNL and INL are -0.6/0.7 LSB and -1.1/2.3 LSB, respectively, with 1ps per LSB in a 9-bit range.

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