An On-Chip Automatic tuning circuit using Integration level Approximation Technique

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Abstract

On-chip automatic tuning circuit with proposed integration level approximation technique, designed in a 0.65m 3.3V CMOS process for tuning of the variation passive component. To verify tunning efficiency of proposed circuit, three types of 2nd-order biquad RC active filters were used. The cut-off frequency (f_c) error of filter with proposed tuning circuit can be reduced by new algorithm that considers the variation of capacitor value in capacitor arrays as well as the variation of normal component. This circuit runs fast so that it can be applied to real-time calibration also. This tuning circuit with 4-bits resolution achieves –1.6% ~ +1.5% cut-off frequency error for ±56% RC variation.

1. Introduction

This paper presents the design of the tuning circuit using the integration level approximation method. Passive components in VLSI circuits may generate the error of circuit operation due to fabrication deviation, temperature variation and aging etc. Along with the development of analog signal processing technique, the demands for the on chip accurate tuning circuit, in VLSI system, have increased, because the variation of passive component values alter the system performance.

Therefore, this paper presents the design of the tuning circuit; we called it as the integration level approximation method. It can reduce the large difference between code values and real output values which are drawback of the dual slope tuning circuit, and compensate the considerable variation of passive component with new algorithm of tuning. And it does not generate signal modulation in VLSI because the tuning codes are fixed in ordinary operation [1]. It could increase accuracy of passive component and reduce complexity of tuning circuit.

To reduce tuning error, the tuning circuit in this paper has to consider two properties as below. 1) One way to reduce tuning error is to use a simple A/D converter that is used for generating of more accurate tuning codes. 2) The variation of passive components occurs in the main circuit and tuning circuit contemporarily.

2. Tuning System

Fig.1 is a block diagram of the proposed tuning system with programmable arrays of parallel connected capacitor [4], which replaces capacitors in the normal circuit. This structure consists of three main blocks.

The first block is the integrator, which measures errors due to process tolerance. The variation range of resistor and capacitor values due to process deviation and temperature variation in VLSI are 27~80pF for the normal passive component values R=2.75MΩ, C=40pF.

The second block is the A/D converter which is implemented by 4-bit charge redistributed successive-approximation method with S/H. Each increment value of capacitor arrays in this A/D converter are different because the integration levels are distributed irregularly on increase or decrease of passive component values. And this fact causes serious quantization error of tuning code if we use normal dual slope tuning method. Thus, in order to reduce the error of quantization, thus preserving good accuracy, modified charge redistributed successive approximation A/D converter [3], which has irregular weighed quantization level, is used. Successive approximation converters that incorporate capacitor DACs are usually based on the “charge redistribution” principle. The DAC consists of binary-weighted capacitors $C_1 \sim C_M$ ($C_j=2C_{j-1}$,j=M, …. 2) and $C_0=C_1$ [7]. Thus, the charge redistributed successive approximation A/D converter has linearly weighted parallel capacitor and the switching of parallel capacitor was performed regularly. As noted in the previous section, in practical circuit, however, this A/D converter was implemented with nonlinear-weighted parallel capacitors and the selecting of

capacitor was occurred irregularly because the integrator generates nonlinearly distributed voltage as varying of passive component. In order to take very high accuracy, the CMOS transmission gate with dummy switch was employed as switch of weighted capacitors. These switches are controlled by control logic and selected capacitors decide comparison level. For example, in ordinary successive approximation A/D converter, the bottom plate of C_M is switched from ground to V_{REF} so that the top plate voltage increases by $V_{REF}/2$. It is similar to this architecture.

Finally the third block of this structure is digital control block, which provides accurate tuning code corresponding to passive component variation and controls capacitor arrays. In practical circuit, A/D converter is implemented with nonlinear-weighted parallel capacitors and the selection of capacitor occurs irregularly because the integrator generates nonlinearly distributed voltage as passive component varies(Fig 2.). To build up tunable characteristics, all capacitors in main circuit have to be replaced with programmable arrays of capacitor.

3. Integration Level Approximation

In Fig.3, it shows that total integration levels divided into +25 % deviation of increasing region and -75 % deviation of decreasing region from normal value. The irregular spread of array values due to enlarge the quantization error of tuning code. To overcome this drawback, this paper presents integration level approximation method. It can generate optimized tuning codes, which make tuned value closer to real values. The modified capacitor arrays, which are switched by tuning code in order to maintain RC product within ±1.5% deviation, reflect the fact that output values of integrator are irregularly distributed.

The output of integrator varies more widely when components value are decreased than when it operates at increasing range of component values. It is considered that the possibility of component variation in capacitor arrays too. The parallel capacitor arrays consist of a fixed capacitance, C_{min}, and random distributed switchable element. Each values of capacitor arrays is determined by previous considerations and it shown as below equation.

$$C_{tune}(i) = \sum_{z=z_{max}(i/8-1)}^{z_{max}} -\frac{z}{1+z}\{C_{nom}(i) - C_{nom}(i-1)\} \qquad i = 0,1,2,\cdots,16$$

, where z is the variation of RC time constant.

4. Simulation

The three types of 2nd-order biquad RC active filters were used to verify tuning efficiency of proposed circuit. The first one is normal biquad RC filter, which does not use tuning circuit, the second one is connected to the 5-bit dual-slope calibrator, and the last one uses proposed tuning circuit. In normal operation mode the dual-slope calibrator operated continuously, driven by the reference clock of nominal frequency 624kHz in [2]. The proposed tuning circuit can operate continuously also, however, driven by 10MHz-reference clock. Therefore, the proposed tuning algorithm has the advantage of dual-slope calibrator in real-time operation characteristic. In normal operation mode, the response shapes for the tuned filter are measured and shown in Fig. 4.

Table I show the simulation result of frequency characteristics with output voltage for each type of filters. For the 2nd-order biquad RC active filter, has 28kHz cut-off frequency, the simulation results for the variation of cut-off frequency are -33.2 % ~ +100 % at non-tuning, maximum +2.86 % at 5-bit dual slope tuning circuit in [1], and -1.5 % ~ +1.1 % at proposed tuning circuit with 4-bit resolution for 56% RC time constant variation. The simulated results of ±RC time constant compensation with integration level approximation are shown in Fig. 5.

5. Conclusion

The proposed on-chip automatic tuning circuit could apply to real time application because it runs with 10MHz-clock speed. And it adopts mixed control circuit, which consists of analog part of A/D converter and digital control logic. It is able to compensate the variation of cut-off frequency within ±1.5 % deviation at ±50 % RC time constant variation from normal value. And, it results in reduced area so that it is also quite good for lower area and error. It is possible to extend the resolution above 5-bit without huge increase of hardware complexities. The improvement of performance of the tuning circuit may be possible by increasing the resolution of tuning codes

References

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[2] A. Durham, J. Hughes, and W. Redman-White, "Circuit Architectures for High Linearity Monolithic Continuous-Time Filtering," *IEEE Trans. Circuits Syst.*-II, vol. 39, pp. 651-657, Sept. 1992.

[3] Behzad Razavi, *Principle of Data Conversion System Design*, IEEE PRESS, 1995.

[4] Lee Sung-Dae *et al* " Automatic Tuning Architecture of RC Time-constant due to the Variation of Integrated Passive Component" *Journal of The Korean Sensors Society*, vol.6, NO.3, pp115-122, Mar. 1997.

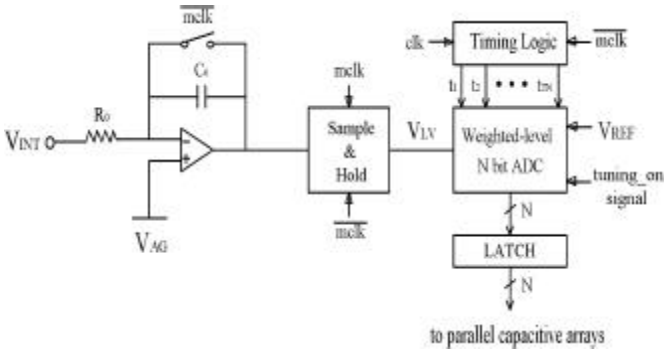


Figure 1. Full block diagram of tuning crcuit

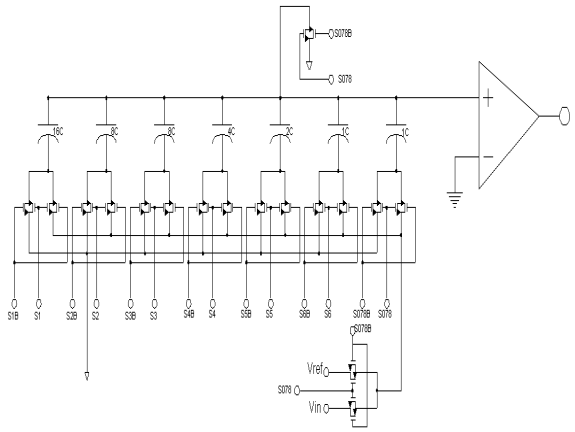
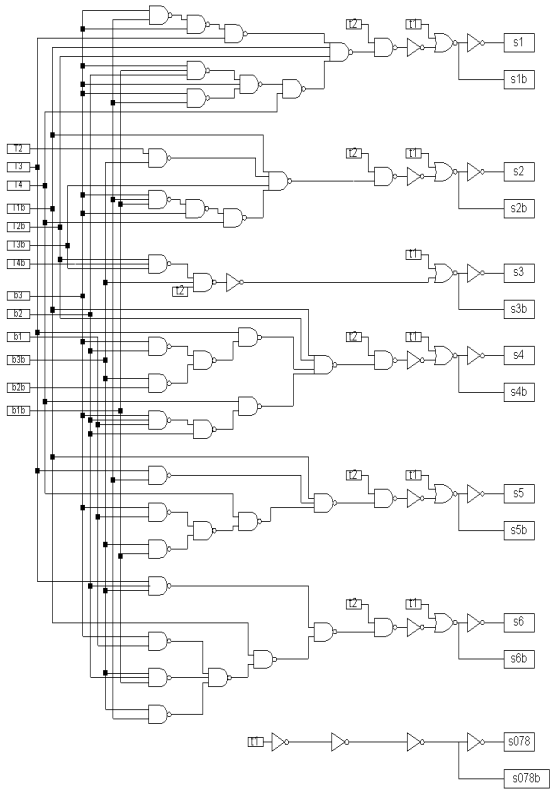
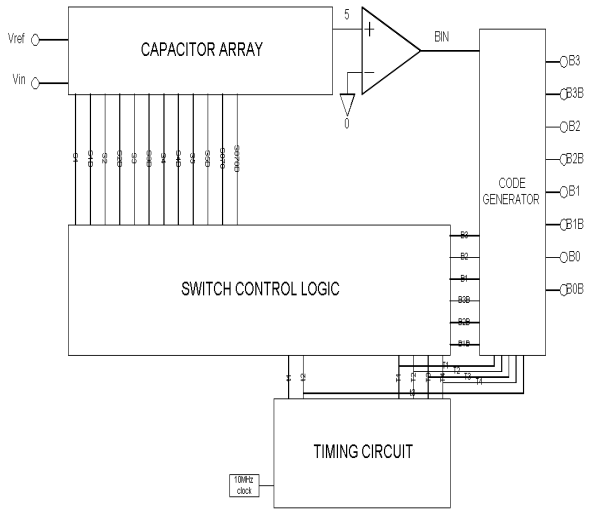


Figure 2. Charge-Redistributed Successive Approximation A/D Converter with non-linear weighted capacitor array



b) Switching circuit

Figure 3.Digital control block



a) Digital control block

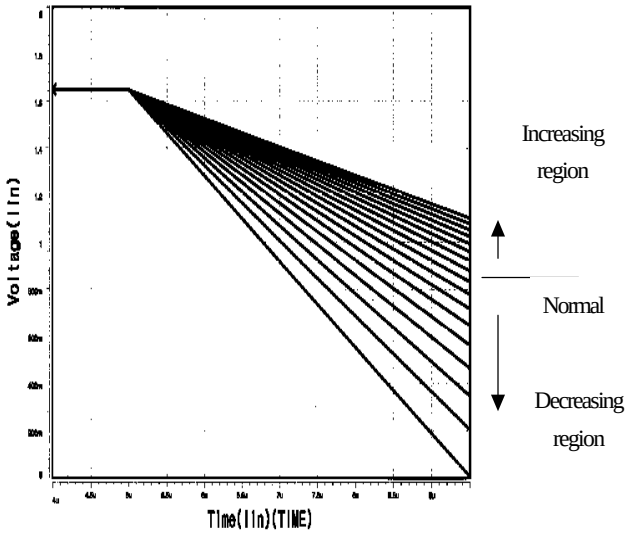
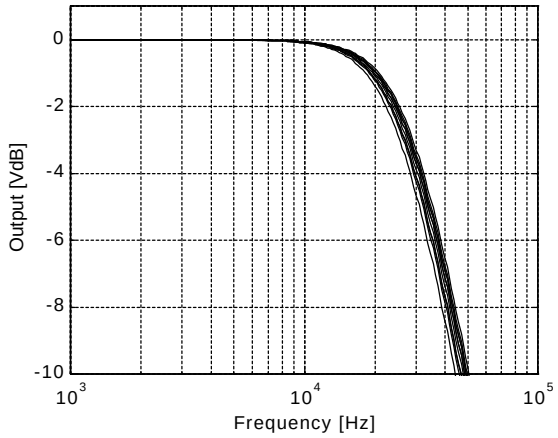
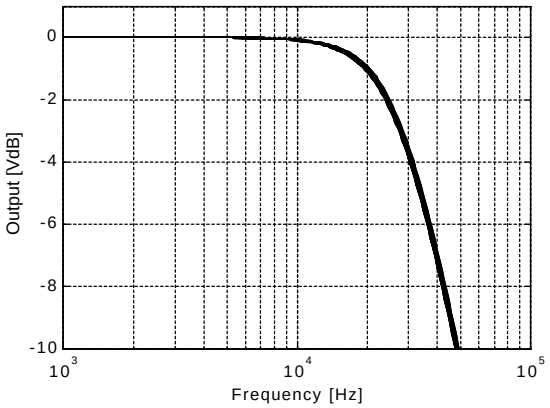


Figure 4. Integration level correspond to passive component variation



a) Using dual-slope calibrator



b) Using Proposed calibrator

Figure 5. The response shapes of tuned filter(2nd-order biquad active RC filter)

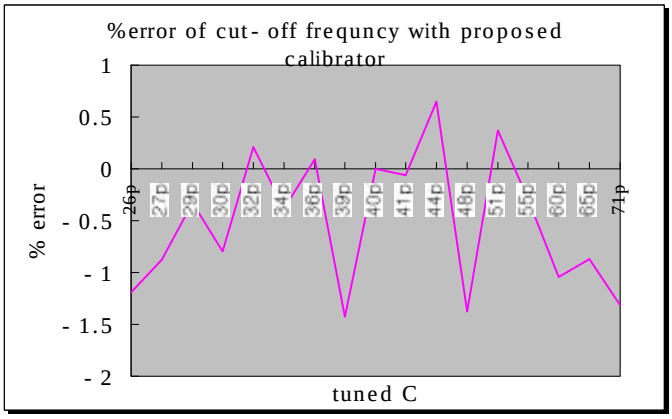


Figure 6. Cut-off frequency error of 2nd-order biquad RC active filter with propos-ed tuning circuit

Table I. The Comparison of simulated result

	Non-tuning	With dual-slope calibrator	With proposed tuning circuit
Maximum Calibrator Quantization Error	100%	+1.53%	-1.05%
F_c error	-33.2% ~ +100%	+2.86%	-1.43% ~ +0.65%