INDUSTRIAL APPLICATION OF HETEROSTRUCTURE DEVICE SIMULATION

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Abstract– We give an overview of the state-of-the-art of heterostructure RF-device simulation for industrial application based on III-V compound semiconductors. Results for Heterostructure Bipolar Transistors (HBTs) and for High Electron Mobility Transistors (HEMTs) are presented in good agreement with measured data of industrially relevant devices.

I. Introduction

With the shrinking of device dimensions and the replacement of hybrid mounted transistors by MMICs, device simulations and circuit simulations with distributed devices need to be carried out by state-of-the-art tools, accounting for physical effects on a microscopic level. Several questions during device fabrication, such as device optimization and process control, can today be addressed by device simulation. Several commercial tools, e.g. [1,2], and University developed simulators, e.g. [3], have been successfully employed for device engineering applications. With the rise of the III-V RF-industry complex heterojunction-based MMICs are in mass production in quantities of 10 millions and above [4] so far only known from the silicon industry. Thus, it is possible to extract a stable base of material parameters for all III-V compound semiconductors of interest, which can be used for device modeling issues.

II. RF-Device Simulators

In contrast to the silicon industry, where process, device, and interconnect-simulation tools form a continuous virtual workbench from material analysis to chip design, III-V simulation mainly focuses on device and circuit aspects. The latter is accompanied by few examples for MESFET technology simulation tools developed parallel to SUPREM e.g. [5]. For heterojunction devices, due to the extensive number of process steps, device simulation focuses on process control and inverse modeling e.g. of geometry. A common feature is the lack of a rigorous approach to III-V group semiconductor materials modeling. As an example modeling of AlGaAs, InGaAs, or even InAlAs and InGaP is restricted to slight modifications of the GaAs material properties. Another common drawback is the limited feedback from technological state-of-the-art process development to simulator development.

The device simulator MEDICI has been used for the simulation of AlGaAs/GaAs HBTs [6]. The device simulator Atlas from Silvaco [7] has further claimed the simulation of AlGaAs/GaAs and pseudomorphic AlGaAs/InGaAs/GaAs HEMTs. The two-dimensional device simulator PISCES [3] incorporates modeling capabilities for GaAs and InP based HEMTs and HBTs. A full set of III-V models and examples for GaAs-based, AlGaAs/InGaAs, InAlAs/InGaAs MESFETs and HEMTs is demonstrated as well as AlGaAs/GaAs, InP/InGaAs, and InGaP/GaAs HBTs. At the quantum level e.g. Gateway Modeling offers a one-dimensional Schroedinger-Poisson solver POSES [8] for charge analysis in HEMT devices for process control. The two- and three-dimensional device simulator DESSIS [2] by the ETH Zürich supplies a rich and extended set of models for device simulation. The capabilities were recently extended by a heterojunction framework to III-V materials. Critical issues as stated in Section III such as extensive trap modeling are solved. Using a simplified one-dimensional current equation quasi-two-dimensional approaches are demonstrated, formerly by the University of Leeds e.g. [9]. This approach has also been verified for a number of examples and for gate-lengths down to 50 nm [10]. It is available as a submodul of Agilents Advanced Design System (ADS) delivering an interface towards the microwave circuit simulator. A similar quasi-two-dimensional tool is available from Silvaco (Fast Blaze) [7].

III. Critical Issues of Modeling III-V Devices

This section addresses critical modeling issues for III-V devices based on GaAs, AlAs, InAs, InP, and GaP, their ternary alloys, and non-ideal dielectrics. They are solved in the two-dimensional device simulator MINIMOS-NT [11]. The models are based on experimental or Monte Carlo simulation data and employ analytical functional forms which cover the whole material composition range. The model parameters are checked against several independent HEMT and HBT technologies to obtain one concise set used for all simulations. Reviewing simulation of HBTs and submicron HFETs with gate-lengths down

to 100 nm used for mm-wave devices, solutions of energy transport equations are necessary to account for non-local effects, such as velocity overshoot. A new model for carrier temperature dependent energy relaxation times [12] has been developed as well as a model for lattice temperature dependent saturation velocities [13].

Considering the nature of the simulated devices (including abrupt junctions) heterointerface modeling is a key issue. Thermionic emission and field emission effects critically determine the current transport parallel and perpendicular to the heterointerfaces. Carrier tunneling must be included to describe the current transport from the channel to the contacts in HEMT devices depending on the alloying of the ohmic contacts. For HFET devices the Schottky contact model determines the possibility to calculate realistic gate currents, based on thermionic effects. Another critical issue for recessed HFETs and for HBTs is the description of the semiconductor-insulator interface. Fermi-level pinning prevails especially for typical barrier materials such as AlGaAs or InAlAs, for ledge materials such as InGaP, and insulators such as SiN. General agreement for HFETs demands a non-local description of the impact ionization. Further, when assessing a complete device description, the inclusion of holes and hot hole effects is necessary. Trap modeling, e.g. the inclusion of DX centers, and especially dynamic trap modeling are the most challenging issues for III-V devices since the carrier lifetimes cannot be generalized without deep insight into process technology, e.g. from *1/f* noise measurements. Bandgap narrowing is considered by an analytical model. A distinction between majority and minority carriers is made for the low field mobility based on Monte Carlo simulations. [14] stressed the importance of Auger recombination for InGaAs-base HBTs relative to SRH recombination. Yet, direct recombination is found to be of limited influence in narrow bandgap HBT devices.

III-V materials are known to have a reduced heat conductivity in comparison to Si [15]. Self-heating effects are accounted for by solving the lattice heat flow equation self-consistently with the energy transport equations. Examples are given in the next section for both HEMT and HBT devices. The determination of thermal boundary conditions and the verification of temperature distributions are performed in agreement with three-dimensional thermal chip simulations. The advance of device simulation further allows a precise physics-based small-signal extraction [16]. Measured bias dependent S-parameters serve as a valuable source of information when compared to bias dependent S-parameters simulated from a device simulator, e.g. from MINIMOS-NT. This procedure reflects the full RF-information contained in the S-parameters and allows process control beyond the comparison of DC-quantities, which do not completely account for the RF-properties of interest, e.g. because of the dynamic trap occupation. Ref. [9] demonstrated a software interface between a quasi-two-dimensional device model and the compact Root large signal model within the Microwave Design System (MDS).

The big challenge remaining for III-V device simulation is the improved understanding of processed semiconductors after different manufacturing steps, e.g. etching. Although a variety of simulators have successfully demonstrated the agreement with measurements the understanding of changes of transport and interface parameters remains the ultimate goal of process control.

IV. Selected Results of Industrially Relevant Devices

For HFET performance the very critical issues are process control and inverse modeling of geometrical structures. Fig. 1 shows the simulated and measured output characteristics of an AlGaAs/InGaAs/GaAs HEMT for a substrate temperature of $T_L = 300$ K.

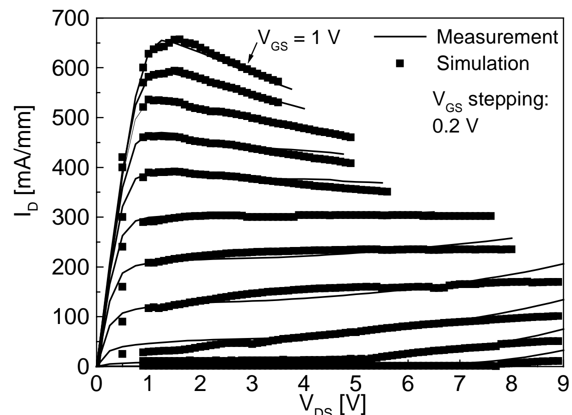

Fig.1: Output characteristics of a pseudomorphic $Al_{0.2}Ga_{0.8}As/In_{0.2}Ga_{0.8}As/GaAs$ high-power HEMT with gate-length $l_g = 300$ nm.

Self-heating effects are accounted for as well as impact ionization. The most critical region of recessed HFETs is the sub gate-contact region. For typical gate-lengths of $l_g = 150$ nm and below the definition of recess structures offers an uncertainty that can be analyzed by device simulation. Fig. 2 shows the sensitivity analysis of the threshold voltage V_{th} towards surface charges and the gate-to-channel separation d_{gc}. Performing such analysis for various recess parameters allows tight control of the device structure during mass production. The measured mean value was $V_{th} = -0.3$ V. Fig. 3 demonstrates a comparison of the simulated and measured S-parameters of a pseudomorphic HEMT at $T_L = 373$ K. No fitting is applied, just the parasitic elements extracted from the measurements are used.

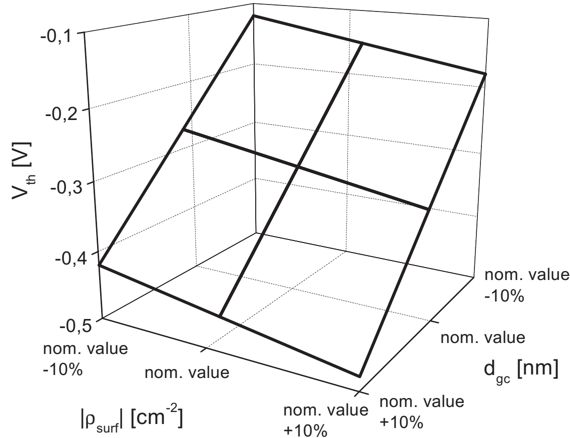

Fig.2: Simulated variations of V_{th} due to variations of gate-to-channel separation d_{gc} and the magnitude of the negative surface charge density ρ_{surf}.

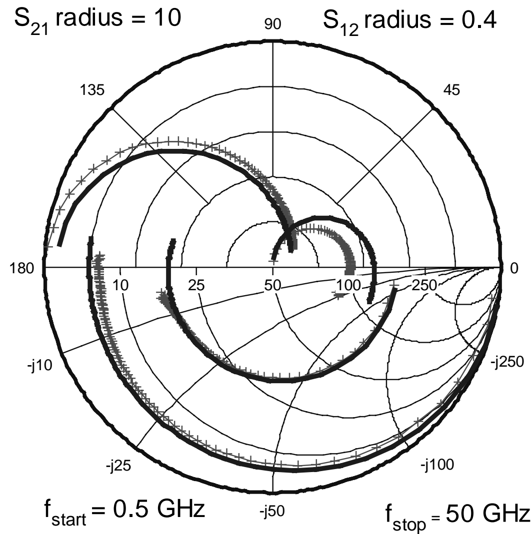

Fig.3: Simulated and measured S-parameters of a l_g= 140 nm HEMT at T_L= 373 K.

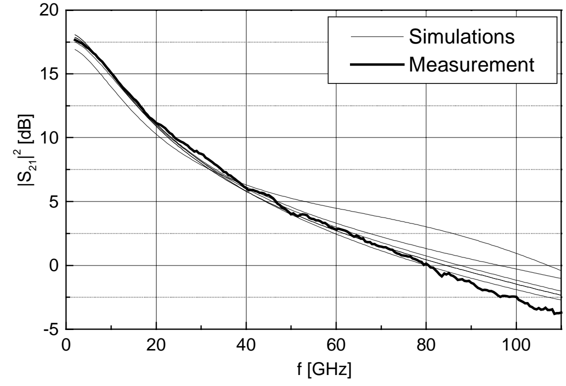

Fig.4: Sensitivity analysis of the magnitude of $|S_{21}|^2$ to d_{gc} variations for a pseudomorphic HEMT.

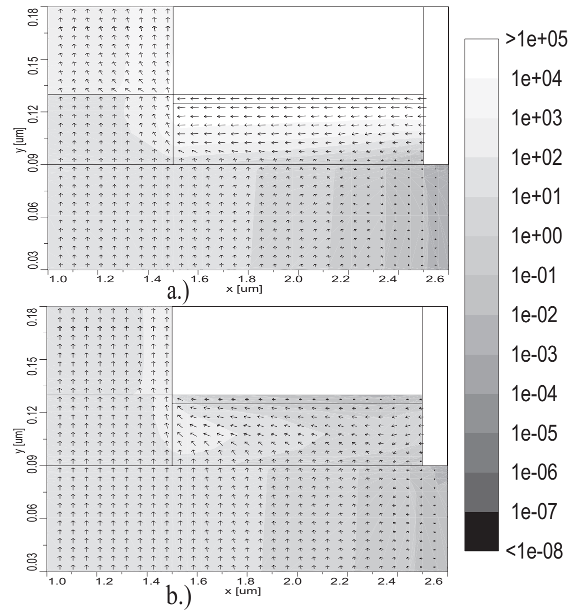

Fig.5: Electron current density [A/cm^2] at V_{BE}=1.2 V. Simulation without surface charges (a) and with a surface charge density of 1×10^{12} cm^{-2} (b).

Fig. 4 shows a sensitivity analysis of the magnitude of $|S_{21}|^2$ to the gate-to-channel separation d_{gc} [17] for l_g =150 nm 2×60 μm HEMT. The effect of the variation for the whole frequency range of operation is visible. The inclusion of temperature changes and self-heating effects allows further analysis since temperature effects are generally not included in nowadays large signal models used for circuit design. In comparison to statistically analyzed wafer mapping results this procedure allows to separate statistical changes from systematic changes during production over a longer time scale.

A typical application for two-dimensional device simulation is the analysis of experimental data, that cannot be explained by simple analytical assumptions, e.g. when several effects compensate. The impact of the ledge [18] thickness and the surface charge density ρ_{surf} is studied for a one-finger InGaP/GaAs HBT with respect to reliability.

We found a value of $\rho_{surf}=10^{12}$ cm^{-2} to be sufficient to get good agreement with the measured Gummel plots at V_{CB}= 0 V. Simulation results for the electron current density at V_{BE} = 1.2 V without (a) and with a surface charge (b) of 10^{12} cm^{-2}, respectively, are shown in Fig. 5. Based on these investigations it is possible to explain the base current degradation (see Fig. 6) of a strongly stressed device by a decrease in the effective negative surface charge density along the interface from 10^{12} cm^{-2} to 4.10^{11} cm^{-2} due to compensation mechanisms [19]. In the case of the output HBT characteristics one meets severe problems to achieve good agreement with measured data, especially for high-power devices. Heat conduction towards possible heat sinks is restricted, so any heat generated e.g. at the heterojunctions leads to significant self-heating and to a change of the electrical device characteristics. Fig. 7 demonstrates

the output characteristics of an AlGaAs/GaAs HBT at constant V_{BE} stepped from 1.4 V to 1.45 V. Note the significant disagreement between simulation without self-heating (SH) and the measured data and the good agreement when self-heating is included in the simulation.

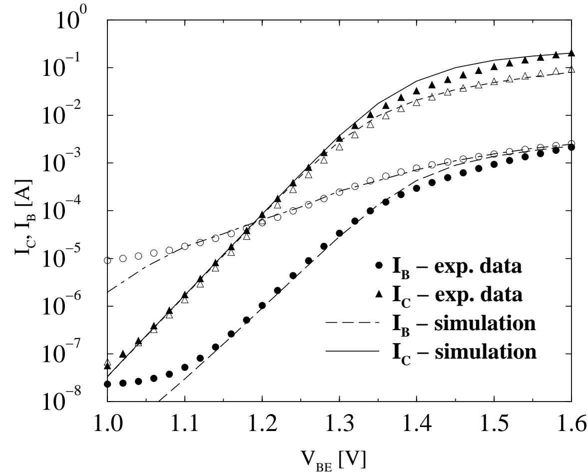

Fig.6: Comparison of measurements (symbols) and simulations (lines) before (filled) and after (open) HBT aging.

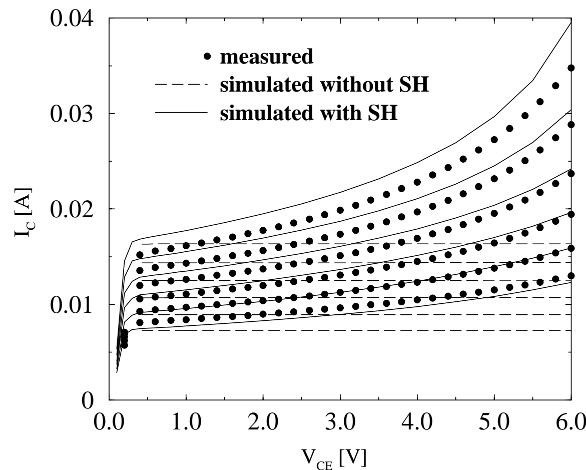

Fig.7: HBT output characteristics. Simulation of with and without self-heating compared to measurement data at constant V_{BE} stepped from 1.4 V to 1.45 V.

V. Conclusion

An overview of the state-of-the-art of simulation tools for heterostructure RF-devices is presented. Simulation results for industrially relevant devices in good agreement with measured data were demonstrated. With an increasing number of stable, reliable heterostructure technologies available, a meaningful comparison between simulation results and statistically analyzed data is possible and delivers on the one hand side model verification, and on the other hand side valuable process information.

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