MOS Capacitor on 4H-SiC as a Nonvolatile Memory Element

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***Abstract* - Nonvolatile-memory characteristics of a metal–oxide–semiconductor (MOS) capacitor are presented, for the first time, in this paper. The MOS capacitors have been fabricated on N-type 4H SiC substrate with nitrided oxide–semiconductor interface. The charge-retention time is in the order of 30,000 years, as determined by thermally activated (200-335°C) transient-capacitance measurements and extrapolation to room temperature. The estimated activation energy of the charge-recombination processes is 1.02 eV.**

I. INTRODUCTION

CURRENTLY, the term *nonvolatile memory* is associated with a variety of so-called *read-only memory* (ROM) elements. These devices can only withstand about 10^6 – 10^7 charging/discharging cycles [1-3], and the charging/discharging times are too long to allow their use for *random-access memory* (RAM) applications. The charge storage in these devices is achieved by trapping the charge in a deep potential well, created by energy-band discontinuity of two materials (typically, semiconductor and oxide). As the energy-band discontinuity does not change with voltage applied, the charging/discharging is based on charge tunneling through very thin material (typically oxide) creating the "walls" of the potential well. This is a slow process and one with limited charging/discharging cycles due to degradation of the oxide physical properties.

In MOS capacitor, the surface band bending due to gate voltage also creates a potential well. This allows the MOS capacitor to be used as a memory element, which is the case in modern RAMs. In silicon, however, the recombination of the stored minority carriers is relatively fast, so the memory has to be refreshed. Silicon carbide is a wide band-gap material, and the recombination rate is orders of magnitude lower. The recombination and generation rates are directly proportional to intrinsic-carrier concentration [4], which is 10^{10} cm^{-3} in silicon and in the order of 10^{-6} cm^{-3} in 4H silicon carbide. Therefore, the minority-carrier lifetime in SiC should be 16 orders of magnitude longer than in Si [5], meaning that a MOS capacitor could operate as a nonvolatile RAM element.

Gardner *et. al.* [6] and Xie *et. al.* [7] proposed a 6H-SiC memory element, where the potential well is created by n–p–n structure. They reported storage time of 10^{14} s (3 x 10^6 years) at room temperature, as extrapolated from high-temperature measurements. They also found that the recombination rate of the stored charge depends very strongly on the quality of the surface passivation at the junction terminations. The reason for that is poor quality of the passivating oxide–SiC interface, in particular, the existence of large density of defects related to carbon accumulation at the interface. As a consequence, the recombination assisted by these defects is so high that no charge retention data have been reported for MOS capacitors on SiC.

Recently, we have shown that the interface carbon can be removed by growing the oxide (or annealing pre-grown oxide) in NO or N_2O ambient [8-10]. In this paper, we report that very long charge-retention times can be achieved with MOS capacitors on 4H SiC with nitrided interface.

II. EXPERIMENT DETAILS

N-type 4H-SiC wafers (manufactured by CREE Research) were used to fabricate the MOS structures. Detail fabrication of nitrided samples has been described elsewhere [10]. The characterization is performed by capacitance transient (C–t) test in the following way. The MOS capacitor is biased in deep-depletion and illuminated by light. The light generates minority carriers, increasing the capacitance to a value well over the equilibrium inversion capacitance. Then, the light is switched off and the change of capacitance is measured by a HP4284A LCR meter. In order to accelerate the recombination of minority carriers, the experiments are performed with capacitors at high temperatures (200 – 335°C).

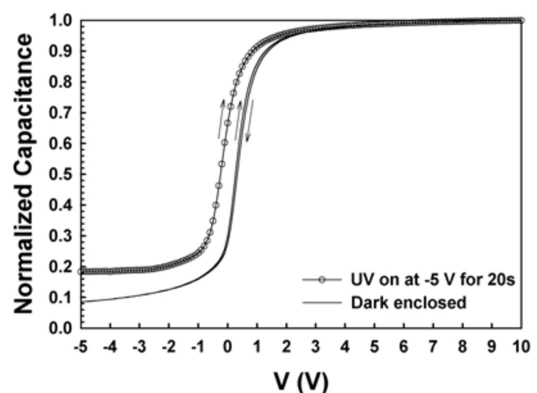

Fig. 1. CV curve for nitrided samples before and after illumination with UV light. Arrows indicate DC sweeping direction.

III. RESULTS AND DISCUSSION

Typical C–V curves of MOS capacitor before and after illumination with UV light are shown in Fig. 1. The C–V curve before illumination is measured by sweeping the voltage from accumulation to deep depletion. Following this, the MOS capacitor is biased in deep depletion (-5V)

and illuminated by UV light, which generates minority carriers in excess of the thermal-equilibrium concentration. Immediately after switching off the light, positive-bias sweep is initiated resulting with a constant capacitance, well above the equilibrium inversion level. This steady-state capacitance level corresponds to "threshold" surface potential of about -0.7V: the reduction of the gate voltage due to the bias sweep does not reduce the surface potential as the excess minority carriers are injected into the substrate. As a result, the depletion-layer width and the measured capacitance are constant. The important conclusion from this observation is that the MOS capacitor could be charged to the theoretical maximum of the minority-carrier density, corresponding to the surface potential of about -0.7V.

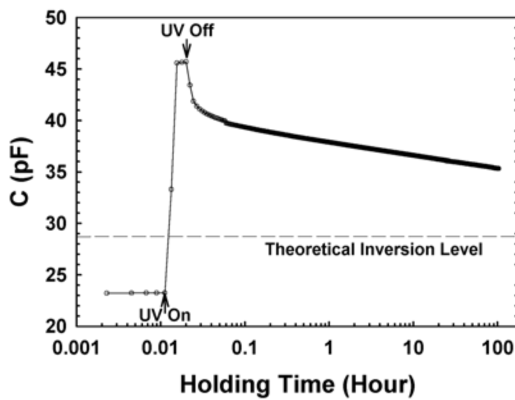

Fig. 2. Transient-capacitance (C-t) plots at room temperature.

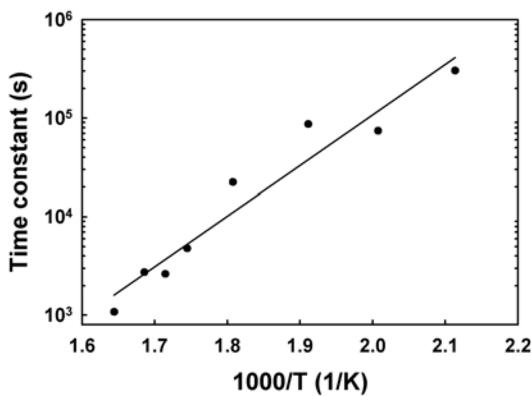

Fig. 3. MOS capacitors time constant at different temperature.

Typical data from the transient-capacitance measurements are presented in Fig. 2. It can be seen that generation-recombination equilibrium is reached under the illumination, causing constant-capacitance in time. When the light is switched off, the generation rate drops to nearly zero, so that the high recombination rate causes relatively fast capacitance decay. However, as the minority carriers recombine, the surface potential shifts from about -0.7V towards the original -5V so that the minority carriers can no longer be injected into the substrate to be recombined with the majority carriers. From that point on, the capacitance change slows down, following exponential decay in time. We define the time constant of this exponential decay as the *storage time.*

The storage times are determined from the slope of the semi-log capacitance–time plots for different ambient temperatures, and the results are presented in Fig. 3. Extrapolation of the storage time to room temperature gives the value of 9.79×10^{11} s (3.11×10^{4} years). This is long enough time to enable the MOS capacitor to be used as a nonvolatile RAM element. However, this time is shorter than the maximum theoretical storage time. The activation energy, determined from the slope, is 1.02 eV. This value is less than half of the energy gap, indicating that defects at the interface are responsible for the faster recombination than the theoretical value for a perfect interface.

IV. CONCLUSIONS

In this letter we have reported the first results on nonvolatile memory characteristic of N-type 4H SiC MOS capacitors with nitrided oxide-SiC interface. The charge-retention time at room temperature and the activation energy are estimated at 9.79×10^{11} s (3.11×10^{4} years) and 1.02 eV, respectively. These results demonstrate that MOS capacitors on SiC enable the development of nonvolatile RAMs.

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