Accurate Estimating Simultaneous Switching Noises by Using Application Specific Device Modeling *

Li Ding and Pinaki Mazumder
Department of Electrical Engineering and Computer Science
The University of Michigan, Ann Arbor, MI 48109.
E-mail: {lding, mazum}@eecs.umich.edu

Abstract

In this paper, we study the simultaneous switching noise problem by using an application-specific modeling method. A simple yet accurate MOSFET model is proposed in order to derive closed-form formulas for simultaneous switching noise voltage waveforms. We first derive a simple formula assuming that the inductances are the only parasitics. And through HSPICE simulation, we show that the new formula is more accurate than previous results based on the same assumption. We then study the effect of the parasitic capacitances of ground bonding wires and pads. We show that the maximum simultaneous switching noise should be calculated using four different formulas depending on the value of the parasitic capacitances and the slope of the input signal. The proposed formulas, modeling both parasitic inductances and capacitances, are within 3% of HSPICE simulation results.

1. Introduction

Simultaneous switching noise (SSN) [1-3], also referred to as ΔI noise or ground/power bounce, is caused by the large instant current, due to the switching of multiple drivers, through the parasitic inductance at the ground (or power) node. SSN causes serious system degradation. It generates glitches on the ground and power-supply wires, decreases the effective driving strength of the circuits, causes output signal distortion, and reduces the overall noise margin of a system. The effect of SSN is getting more significant as a result of the continuous increase in integration level on a single chip and in operating speed. Therefore, it is extremely important to accurately model the SSN and develop SSN-aware design methodologies to ensure the performance and reliability of the current and future VLSI systems.

*This work was partially supported by the MURI (AFOSR) program.

SSN is most evident near the output pads because of the large inductance of the bonding wires and packages as well as the large instant current caused by the simultaneous switching of multiple strong output drivers. Output driver SSN modeling have been studied extensively in the literature [4-8] and many driver design methodologies to reduce the SSN are also reported [9-11]. There are two central issues in any SSN model: the MOSFET model that is employed and the parasitics considered in the model.

Sakurai and Newton's α-power law model [12] for short channel devices is usually employed for SSN modeling in recent years [6-8]. However, equations formulated based on the α-power law model is difficult to solve analytically because of the form of the α-th power function. Different approximation techniques, therefore, had to be used. Vemuru assumed that the derivative of the drain current expression was a constant for submicron processes [6]. Jou *et al.* in [7] used a Taylor expansion of the drain current equation and neglected those second and higher order terms. And in [8], two assumptions were made, i.e., constant derivative of the drain current and linear time dependent SSN voltage. In this paper, we introduce an application-specific device modeling (ASDM) methodology for SSN modeling. In contrast to conventional short channel device models like the α-power law model, the proposed methodology only attempts to model the interested operation region of a MOSFET device in a specific application. By trading off flexibility of a full MOSFET model, ASDM will give a more accurate modeling in the interested region and has a simpler mathematical formulation. Using the proposed model, we have developed new SSN modeling formulations that do not introduce additional approximations in the derivation process.

For the purpose of SSN modeling at I/O pads, previous models only consider the parasitic inductance while the parasitic capacitance and resistance of the wires and pads are neglected, usually without sound justification. For a typical pin grid array (PGA) package, the values of the parasitic inductance, capacitance and resistance are 5 nH, 1 pF, and 1 mΩ, respectively [9]. While it is a very good approximation to neglect the small resistance, the effect of the

Proceedings of the 2002 Design, Automation and Test in Europe Conference and Exhibition (DATE'02)
1530-1591/02 $17.00 © 2002 **IEEE**

IEEE COMPUTER SOCIETY

parasitic capacitance has not been quantitatively evaluated. In this paper, we derive a complete SSN model which considers both parasitic inductance and capacitance and show that the maximum SSN voltage can be obtained using four formulas depending on the operating regions of the system. Through HSPICE simulation, it is observed that the SSN formula without including the capacitance effect is more or less adequate in the over-damped region. However, the proposed new formulation with parasitic capacitance included has to be used in the under-damped regions.

2. MOSFET Modeling for SSN Applications

In this paper, we study the simultaneous switching noise caused by the switching of N identical output drivers. For simplicity of presentation, only the noise at the ground node is discussed. The SSN at the power-supply node can be analyzed similarly. We neglect the small parasitic resistance at the bonding wires and package pins. The pull-down transistors are modeled as a voltage controlled current source. Usually, the load capacitance of the drivers C_L is very large, so one can reasonably assume that the output nodes stay high during the input rising period and the transistors are in the saturation region [4].

According to Sakurai and Newton's α-power law model [12], the drain current of a MOSFET device in the saturation region can be modeled as:

$$I_D = K(V_{GS} - V_T)^{\alpha}, \qquad (1)$$

where V_T is the threshold voltage and α is a fitting parameter which is close to 2 for long channel FETs and is close to 1 for short channel devices. Directly applying Eqn. (1) for analytical study of the SSN, however, turns out to be difficult to obtain closed-form formulas. Previous works either assume $(V_{GS} - V_T)^{\alpha-1}$ is a constant for short-channel devices or use a Taylor expansion and neglect the higher order terms. All these practices may lead to inaccuracy in *addition* to the error introduced in device modeling.

On the other hand, we are only interested in some specific operating regions of a transistor for the SSN application. More specifically, we are interested in the case that the drain terminal of the FET stays high during the input rising period and the source and bulk terminals of the FET have the same voltage. Therefore, the drain current of a FET can be written as a function of two variables, the gate voltage and the source voltage:

$$I_D = f(V_G, V_S). \qquad (2)$$

In Fig. 1, we plot the drain current of a TSMC 0.18μm process n-type transistor ($W = 100\mu m$) with respect to the gate voltage at different source voltage values. The

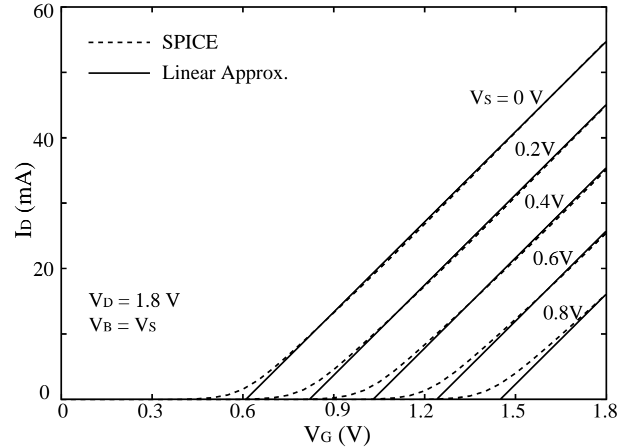

Figure 1. Modeling of MOSFET IV characteristic.

dashed curves are obtained through HSPICE simulation using Level 49 MOSFET model (BSIM3). It is observed that 1) for any given value of V_S, I_D is approximately a linear function of V_G; 2) the group of I_D versus V_G curves are equally spaced with different V_S value, which suggests a linear dependence of I_D on V_S. Therefore, the transistor drain current can be formulated as:

$$I_D = K(V_G - V_0 - \gamma V_S), \qquad (3)$$

where V_0 measures the voltage displacement and γ is a fitting parameter which is always greater than 1 in real processes.

As illustrated in Fig. 1, this simple linear model captures the drain current curves fairly well except the case when the gate voltage is very close to the threshold voltage. The small discrepancy near the threshold region is not an issue for SSN modeling because the current as well as the change in current in this region is insignificant. It is also noted that even the α-power law model is not accurate near this region [12].

The proposed SSN-specific device model looks similar to the α-power law model when α is set to 1. However, it is by no means simply forcing $\alpha = 1$ in the α-power law model. For example, in the α-power law model, V_T is the threshold voltage which is about 0.5V for the 0.18μm NFET. In our model, the value of V_0 is 0.61V which does not have to be the transistor threshold voltage. A general purpose device model, like the α-power law model, tries to achieve good overall matching. In our case, we only need to consider a single case: $V_B = V_S$ and $V_D = V_{DD}$. It is exactly the inflexibility of the ASDM that gives simpler formulation and more accurate result for the targeted application.

IEEE COMPUTER SOCIETY

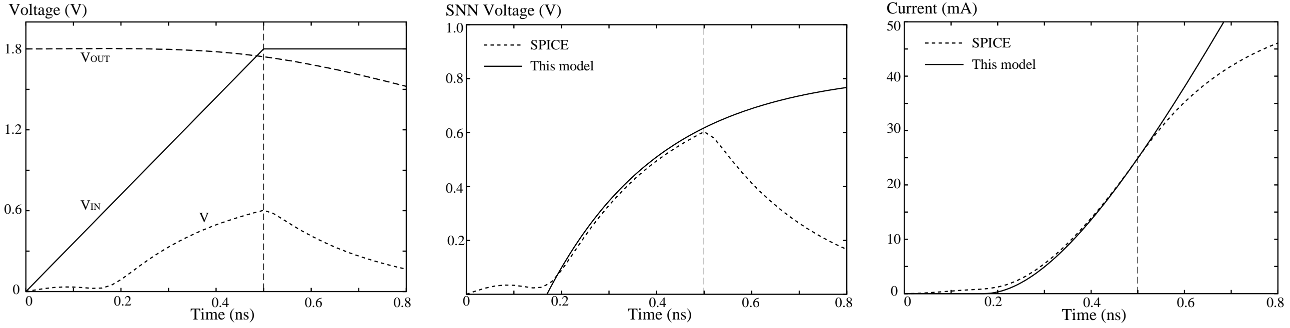

Figure 2. Comparison of SPICE simulation and model results. (a) simulated waveforms; (b) simulated and modeled SSN voltage; (c) simulated and modeled current through the inductor.

3. Simultaneous Switching Noise Calculation

Previous models for the SSN near output drivers only consider the parasitic inductance [6-8]. To make a fair comparison with those models, in this section, we first assume that the effect of the parasitic capacitance can be neglected. The condition when this assumption is valid will be discussed in the next section.

When the parasitic inductance is the only device connecting between the NFETs and the true ground, the simultaneous switching noise due to the discharging current of N identical drivers in the inductor is written as:

$$V = NL\frac{dI_D}{dt}. \tag{4}$$

Inserting Eqn. (3) into the right side of the above equation and noting that in this application V_G and V_S should be replaced by V_{IN} and V, respectively, one obtains:

$$V = NLK\big(\frac{dV_{IN}}{dt} - \gamma\frac{dV}{dt}\big),$$

which can be simplified to:

$$\frac{dV}{dt} + \frac{V}{NLK\gamma} = \frac{s_r}{\gamma}, \tag{5}$$

where s_r is the rising slope of the input signal. Eqn. (5) is a first-order ordinary differential equation. Using the boundary condition that the ground node voltage is zero at the time $t_0 = V_0/s_r$ when the input voltage equals V_0, we get the following time dependent formula for simultaneous switching noise voltage at the ground node:

$$V(t) = NLs_rK\big(1 - e^{-\frac{s_r(t-t_0)}{\gamma NLs_rK}}\big), \quad t_0 \le t \le V_{DD}/s_r. \tag{6}$$

The maximum noise voltage is achieved at the time input signal reaches V_{DD}, which, after simplification, reads:

$$V_m = NLs_rK\big(1 - e^{-\frac{V_{DD}-V_0}{\gamma NLs_rK}}\big). \tag{7}$$

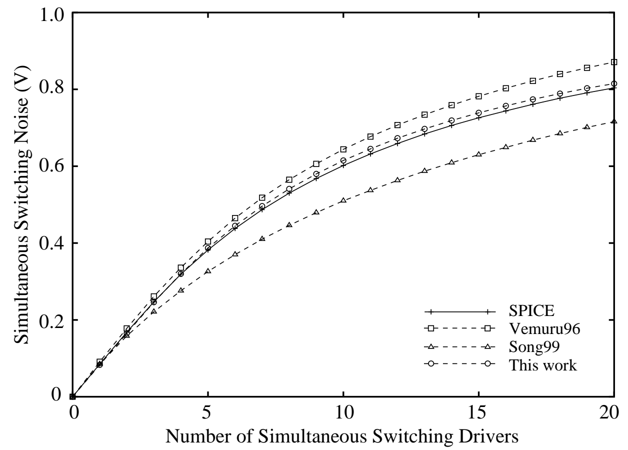

Figure 3. Comparison with previous models.

The time dependent current through the transistor can then be calculated using Eqs. (3) and (6):

$$I_D = K\big(s_rt - V_0 - \gamma NLs_rK(1 - e^{-\frac{s_r(t-t_0)}{\gamma NLs_rK}})\big), \tag{8}$$

in the region $t_0 \le t \le V_{DD}/s_r$.

Fig. 2 compares the results of Eqs. (6) and (8) with SPICE simulation results using typical parameters ($L = 5.0nH$, $W = 100\mu m$, $t_r = 0.5ns$, and $C_L = 10pF$). Note that the formulas are valid only in the range that the input signal is rising, in this case, from 0 to $0.5ns$. It is observed that both the SSN voltage formula and the current formula match the SPICE simulation results very well.

Fig. 3 plots the calculated maximum SSN voltage, obtained using Eqn. (7), together with two previous model calculation results [6],[8] for the TSMC 0.18μ process. The new model is shown to be the most accurate with different number of simultaneously switching drivers. Similar results are also observed using 0.25μm and 0.35μm processes.

Besides being accurate, the formulation of the maximum

IEEE COMPUTER SOCIETY

SSN voltage, Eqn. (7), is very simple. Now let us further look into this equation. Defining a circuit-oriented figure H:

$$H = NLs_r, \tag{9}$$

the maximum SSN voltage formula can be rewritten as:

$$V_m = HK\left(1 - e^{-\frac{V_{DD}-V_0}{\gamma HK}}\right). \tag{10}$$

First, it is observed that the maximum SSN voltage is a function of the circuit-oriented figure H and process-oriented parameters K, V_{DD}, V_0 and γ. The design implication of this observation is that, given a process, H is the only variable that we can use in circuit design to control the simultaneous switching noise.

Second, H is a simple multiplication of three factors: N, L and s_r. This means that changes in each of those three factors will have same effect on the change in SSN. Intuition indicates that the SSNs are caused by the parasitic inductance, therefore we should try to reduce the inductance. In practice, however, given a bonding method and a fixed number of ground pads available, the value of L is more or less a fixed number in a given process. The design implication of the second observation is that we should try to reduce N and/or s_r when reducing L is not feasible and that the effects in SSN controlling are same: 1) instead of reducing the number of output drivers, reducing N in practice means to make the drivers not switching simultaneously; 2) slower switching inputs to the driver will reduce SSN.

4. SSN Modeling with Parasitic Capacitance

In this section, we study the simultaneous switching noise problem considering both parasitic inductance and capacitance. The SSN problem can be formulated as follows:

$$V = L\frac{dI_L}{dt}, \tag{11}$$

$$I_L = NK(s_r t - V_0 - \gamma V) - C\frac{dV}{dt}, \tag{12}$$

where I_L is the current flows through the inductor. Plugging Eqn. (12) into the right side of Eqn. (11), one gets the following second-order ordinary differential equation:

$$C\frac{d^2V}{dt^2} + NK\gamma\frac{dV}{dt} + \frac{1}{L}V = NKs_r. \tag{13}$$

The eigenfunction of the above differential equation is

$$CX^2 - NK\gamma X + 1/L = 0. \tag{14}$$

Denoting

$$\Delta = N^2K^2\gamma^2 - 4C/L, \tag{15}$$

the system is in one of the three operating regions depending on the value of Δ.

Case (1): $\Delta > 0$, (over-damped region).
In this region, Eqn. (14) has two different real roots. Let us denote

$$\lambda_1 = \frac{NK\gamma - \sqrt{N^2K^2\gamma^2 - 4C/L}}{2C}, \tag{16}$$

$$\lambda_2 = \frac{NK\gamma + \sqrt{N^2K^2\gamma^2 - 4C/L}}{2C}, \tag{17}$$

where $\lambda_2 > \lambda_1 > 0$. Using the initial condition that $V(t_0) = 0$ and $dV(t_0)/dt = 0$, the time dependent SSN voltage can be derived as:

$$V(t) = NLKs_r\left(1 - \frac{\lambda_2}{\lambda_2 - \lambda_1}e^{-\lambda_1 t'} + \frac{\lambda_1}{\lambda_2 - \lambda_1}e^{-\lambda_2 t'}\right), \tag{18}$$

where $t' = t - t_0$. To find the maximum noise voltage, one needs to find the local maximas, which is obtained by letting the derivative of the noise voltage to zero, as well as the noise voltages at the boundaries, more specifically to this application, the noise voltage at time t_r. It can be shown that the derivative of the SSN voltage in this case is positive definite during the time period $t_0 < t \le t_r$. Therefore, the approximate maximum SSN voltage is obtained at time t_r.
Case (2): $\Delta = 0$, (critically damped).
In this case, Eqn. (14) has two degenerated real roots. Let us denote

$$\lambda = \lambda_{1,2} = \frac{NK\gamma}{2C}. \tag{19}$$

The SSN voltage can be obtained as:

$$V(t) = NLKs_r\left(1 - (1 + \lambda t')e^{-\lambda t'}\right). \tag{20}$$

The derivative of the SSN voltage in this case is also positive definite during the time period $t_0 < t \le t_r$. Therefore, the approximate maximum SSN voltage is also obtained at time t_r.
Case (3): $\Delta < 0$, (under-damped region).
In this region, Eqn. (14) has two complex roots. Let us denote

$$\lambda = \frac{NK\gamma}{2C}, \quad \varpi \quad \frac{\sqrt{4C/L - N^2K^2\gamma^2}}{2C}. \tag{21}$$

The time dependent simultaneous switching noise voltage can be similarly calculated as:

$$V(t) = NLKs_r\left(1 - e^{-\lambda t'}(cos\omega t' + \frac{\lambda}{\omega}sin\omega t')\right). \tag{22}$$

The derivative of the SSN voltage is

$$V'(t) = NLKs_r\frac{\lambda^2 + \omega^2}{\omega}e^{-\lambda t'}sin\omega t'.$$

Therefore the simultaneous switching noise voltage reaches local maxima/minima when the term $sin\omega t'$ is zero. Using

IEEE COMPUTER SOCIETY

Table 1. Formulas for Maximum SSN Voltage Considering Both Parasitic Inductance and Capacitance.

Case	Condition	Description	Maximum SSN voltage formula
1	$\Delta > 0$	over damped	$NLKs_r(1 - \frac{\lambda_2}{\lambda_2-\lambda_1}e^{-\lambda_1 t_{r,0}} + \frac{\lambda_1}{\lambda_2-\lambda_1}e^{-\lambda_2 t_{r,0}})$,
2	$\Delta = 0$	critically damped	$NLKs_r(1 - (1+\lambda t_{r,0})e^{-\lambda t_{r,0}})$,
3a	$\Delta < 0, t_{r,0} \le \pi/\omega$	under damped	$NLKs_r(1 - e^{-\lambda t_{r,0}}(cos\omega t_{r,0} + \frac{\lambda}{\omega}sin\omega t_{r,0}))$,
3b	$\Delta < 0, t_{r,0} > \pi/\omega$	under damped	$NLKs_r(1 + e^{-\frac{\lambda}{\omega}\pi})$,
where $t_{r,0} = t_r(1 - V_0/V_{DD})$, $\lambda = NK\gamma/(2C)$, $\omega = \sqrt{4C/L - N^2K^2\gamma^2}/(2C)$, $\lambda_1 = (NK\gamma - \sqrt{N^2K^2\gamma^2 - 4C/L})/(2C)$, $\lambda_2 = (NK\gamma + \sqrt{N^2K^2\gamma^2 - 4C/L})/(2C)$.			

the information of the second-order derivative of the SSN voltage, it can be derived that the local maximas occur when

$$t_n = t_0 + (2n-1)\pi/\omega, \quad n = 1, 2, ... \tag{23}$$

with the constraint that $t_n < t_r$. By inserting Eqn. (23) into Eqn. (22), the SSN voltage values at those local maximas is obtained:

$$V_n = NLKs_r\left(1 + e^{-\frac{\lambda}{\omega}(2n-1)\pi}\right),$$

which is a restrict monotonous decrease function with respect to n. Therefore, the maximum SSN voltage among those local maximas is:

$$V_1 = NLKs_r\left(1 + e^{-\frac{\lambda}{\omega}\pi}\right), \tag{24}$$

which is achieved when

$$t = t_1 = t_0 + \pi/\omega. \tag{25}$$

Note that the SSN voltage at the boundary t_r is always smaller than or equal to its proceeding local maxima, which is in turn smaller than the first peak V_1. Therefore, as long as the time to reach the first peak is less than the input signal rising time, i.e.,

$$t_r > t_0 + \pi/\omega, \tag{26}$$

the absolute maximum SSN voltage is the voltage at the first peak as given in Eqn. (24). If, on the contrary, the Inequality (26) does not hold, the maximum SSN voltage is obtained at the boundary, i.e., letting $t = t_r$ in Eqn. (22).

In all, there are four possible cases: i) over damped, ii) critically damped, iii) under damped with fast input signal, and iv) under damped with slow input signal, which have different formulations for the maximum SSN voltage. A complete list of formulas for maximum simultaneous switching noise voltage calculation derived in this section is shown in Table 1.

Fig. 4 compares the formulas with HSPICE simulation results in terms of the maximum simultaneous switching noise voltage. Fig. 4(a) and (c) show a typical case that $L = 5.0nH$ and $C = 1.0pF$ while Fig. 4(b) and (d) assumes that the number of ground pads are doubled, therefore the inductance is halved and the capacitance is doubled. In both cases, it is observed that the simple model without considering the parasitic capacitance performs adequately in the over-damped and critically damped regions. But the error is significant in the under-damped region. On the other hand, the improved model considering both parasitic inductance and capacitance has a relative error of less than 3% in the entire region for both cases.

From the definition of Δ, we can get the value of the critical capacitance, defined as:

$$C_{crit} = \frac{N^2K^2\gamma^2L}{4}. \tag{27}$$

When the parasitic capacitance is greater than C_{crit}, the system is in the under-damped region. Therefore, one should use the more accurate SSN formulas shown in Table 1. Note that C_{crit} is a quadratic function of N, meaning that when N is small C_{crit} will be very small, and vice versa. Therefore, the system is very likely in the under-damped region when N is small and in the over-damped region when N gets large. We have observed this phenomena in Fig. 4.

5. Conclusion

In this paper, we study the increasingly important problem of simultaneous switching noises near chip I/O pads. There are two main contributions of this work. First, we introduced a SSN-specific MOSFET modeling methodology which is shown to be superior than the α-power law model in terms of both accuracy and simplicity for our targeted problem. And second, we quantitatively evaluated the effect of the parasitic capacitance on the simultaneous switching noise for the first time. We showed that the effect of the capacitance is not negligible when the system is in the under-

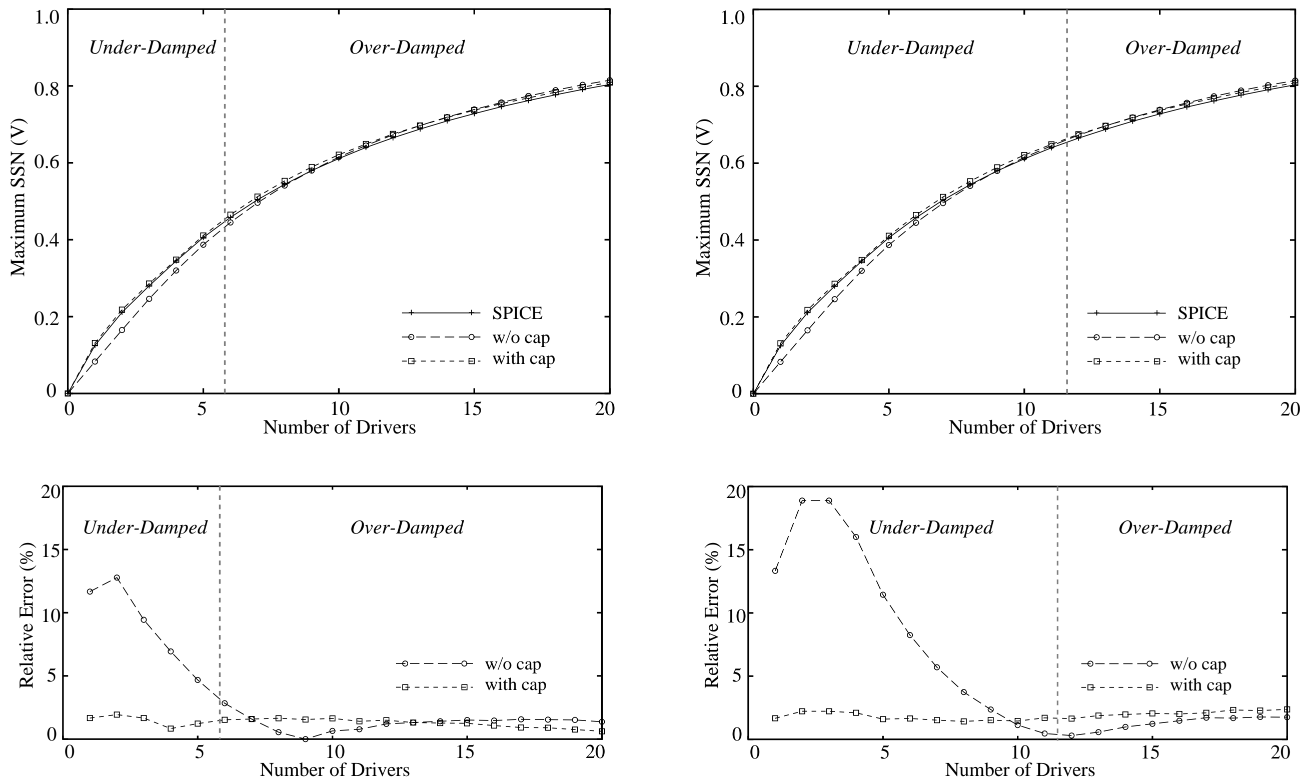

Figure 4. Comparisons of simulated and calculated maximum SSN voltages.

damped region and we derived SSN formulas which model the effects of both parasitic inductance and capacitance.

References

[1] G. A. Katopis, "ΔI Noise Specification for a High-Performance Computing Machine," *Proceedings of the IEEE*, vol. 73, no. 9, pp. 1405-1415, Sep. 1985.

[2] M. Dolle, "Analysis of Simultaneous Switching Noise," *IEEE International Symposium on Circuits and Systems*, vol. 2, pp. 904-907, May 1995.

[3] T. J. Gabara, *et al.*, "Forming Damped LRC Parasitic Circuits in Simultaneously switched CMOS Output Buffers," *IEEE Journal of Solid-State Circuits*, vol. 32, no. 3, pp. 407-418, Mar. 1997.

[4] R. Senthinathan and J. L. Prince, "Simultaneous Switching Ground Noise Calculation for Packaged CMOS Devices," *IEEE Journal of Solid-State Circuits*, vol. 26, no. 11, pp. 1724-1728, Nov. 1991.

[5] A. Vaidyanath, B. Thoroddsen, and J. L. Prince, "Effect of CMOS Driver Loading Conditions on Simultaneous Switching Noise," *IEEE Transactions on Components, Packaging, and Manufactoring Technology - Part B*, vol. 17, no. 4, pp. 480-485, Nov. 1994.

[6] S. R. Vemuru, "Accurate Simultaneous Switching Noise Estimation Including Velocity-Saturation Effects," *IEEE Transactions on Components, Packaging, and Manufacturing Technology - Part B*, vol. 19, no. 2, pp. 344-349, May 1996.

[7] S.-J. Jou, W.-C. Cheng, and Y.-T. Lin, "Simultaneous Switching Noise Analysis and Low Bouncing Buffer Design," *IEEE Custom Integrated Circuits Conference*, pp. 545-548, 1998.

[8] S. W. Song, *et al.*, "Accurate Modeling of Simultaneous Switching Noise in Low Voltage Digital VLSI," *IEEE International Symposium on Circuits and Systems*, vol. VI, pp. 210-213, May 1999.

[9] R. Senthinathan and J. L. Prince, "Application Specific CMOS Output Driver Circuit Design Techniques to Reduce Simultaneous Switching Noise," *IEEE Journal of Solid-State Circuits*, vol. 28, no. 12, pp. 1383-1388, Dec. 1993.

[10] Y. Yang and J. Brews, "Design for Velocity Saturated, Short-Channel CMOS Drivers with Simultaneous Switching Noise and Switching Time Considerations," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 9, pp. 1357-1360, Sep. 1996.

[11] S. R. Vemuru, "Effects of Simultaneous Switching Noise on the Tapered Buffer Design," *IEEE Transactions on VLSI Systems*, vol. 5, no. 3, pp. 290-300, Sep. 1997.

[12] T. Sakurai and A. R. Newton, "Alpha-Power Law MOSFET Model and its Application to CMOS Inverter Delay and Other Formulas," *IEEE Journal of Solid-State Circuits*, vol. 25, no. 2, pp. 584-594, Apr. 1990.

1530-1591/02 $17.00 © 2002 **IEEE**

IEEE COMPUTER SOCIETY