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Review Paper on Power Efficient Hybrid D-Flip Flop

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***ABSTRACT*:** In nanometer CMOS technologies leakage powerhas become a serious concern and is a very important issue in hardware and software VLSI design. The leakage powerincreases as technology is scaled down. Low power flip-flops play a vital role for the design of low-power digital systems. In thispaper several different flip flop topologies are analyzed andpower efficient flip flop method is proposed. This paper presentssurvey on low power hybrid dual dynamic flip flop (DDFF) andembedded logic module (DDFF-ELM) based on DDFF. Thissurvey concludes that ultra low leakage CMOS structure calledas sleepy stack inverter pair method which is efficient in leakagepower reduction for design of low power hybrid flip flop thusproviding circuit designer with new choice to handle leakagepower problem.

KEYWORDS: CMOS, DDFF, DDFF-ELM, sleepy-stack, powerdissipation

I. INTRODUCTION

In nanoscale technology leakage is a serious problem particularly for CMOS circuits. According to the International Technology Roadmap for Semiconductors (ITRS) leakage power consumption may come to dominate total chip power consumption as technology feature size shrinks. With the growing trend towards portable computing and wireless communication the need of low power increases day-by-day. As Flip flop and latches are the major source of power consumption in synchronous system thus studies of low power and high performance flip flop is important.

The industry for low power consumer electronic products is booming with a rapidly expanding market. As Flip-flops are common building blocks and are frequently used in digital VLSI circuits. These are used as starting, intermediate and ending part in the systems. They consumes large amount of power because these are operated at system operating Frequency. Thus a careful design of low power flip flop is important for Low power VLSI system.

Sequential logic circuits such as registers, memory element scounters etc are mostly used in implementation of Very Large Scale Integration (VLSI) Circuits. The CMOS technologies approach has its fundamental physical limits. However, when scaling comes down to submicron level or Nano level many problems occur. As the feature size shrinks, upto 0.09µ and 0.065µ, static power has become a greatchallenge for current and future technologies and if physicalgate length is reduced to below 65nm several device leveleffects such as short channel effect and exponential increasein leakage current. The four main sources of leakage currentin a CMOS transistor are i) Reverse-biased junction leakagecurrent ii) Gate induced drain leakage iii) Gate directtunnellingleakage and iv)Sub-threshold (weak inversion)leakage current. The sub-threshold leakage current being themost leading amongst all the leakage current sources whichbecomes very challenging for research in current and futuresilicon technologies.

The flip-flop is considered to be the most essentialmemory cell in the vast majority of digital circuits. Thus, wedesign a new dual dynamic node hybrid flip-flop (DDFF)and dual dynamic node hybrid flip-flop with embeddedlogic module (DDFF-ELM) by using sleepy stack inverterpair. Thus the sleepy stack inverter pairs are efficient inleakage power reduction and overall power dissipation astechnology scales down to 90nm and below.

Flip flop is widely use in synchronous sequentialcircuits and it can be designed in two logic styles namelystatic and dynamic. Dynamic style exhibits high speed andless area where static design style exhibits less power. Thushere we consider hybrid flip flop which possess advantageof both static and dynamic design style. The dynamic stylepresent at the input side and static style present at the outputside of flip-flop design.

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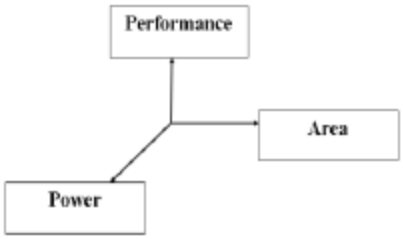

Fig. 1 Design Parameters

The power is rising as the most critical and vital issues in system on chip design today and management of power in every category of design is becoming an urgent problem. In early 1970's, providing high speed operation with minimum area were main aim of design. Many design tools are concentrated to achieve these goals shown in Fig 1

In CMOS VLSI circuits, power dissipation is basically due tothe three important and major components: dynamic, staticand short circuit.

$$P = P_{dynamic} + P_{short\ circuit} + P_{leakage}$$

Dynamic power dissipation is due to switching activityand short circuiting.

$$Pd = f\ C\ Vdd^2$$

Pshort circuit power is caused by the finite rise and fall time ofinput signals, resulting in both the pull up network and pulldown network to be ON for a short while.

$$Ps = I_{leakage}\ Vdd$$

Pleakageis the leakage power. When supply voltage scalingdown, the threshold voltage also decreases to maintainperformance. However, this leads to the exponential growthof the sub threshold leakage current. Sub threshold leakage
is the dominant leakage

$$P_{leakage} = \mathbf{I}_{leakage}\ \mathbf{V}dd$$

II. PREVIOUS WORK DONE

In the design of various sequential circuits, a major challengeis the Design of an efficient low power hybrid D-flip–flop.Thus in many papers different flip flops are proposedovercoming the drawbacks of their presiding designs andanalyze power of different dual dynamic node hybrid flip flop.KalarikkalAbsel have designed low-Power dual dynamicnode pulsed hybrid flip-flop. In this paper first they havecompared and discussed about some existing static anddynamic flip-flop such as Hybrid latch flip-flop (HLFF), semidynamic flip-flop (SDFF) and cross charge controlled flip-flop(XCFF). They studied and designed two different kinds ofpulsed hybrid flip flop which is called as dual dynamic nodeflip flop (DDFF) and a novel embedded logic module (DDFFELM)and both of them eliminate the drawbacks of unwantedtransitions in cross charge controlled flip-flop (XCFF) whendata input is stable at 0. Their design carried out comparison of low power pulsed hybrid flip-flop and gives 29% and 7%reduction in total power dissipation compared to SDFF andXCFF at 50% data activity [1].

MeghanaPelleti has proposed low power and low area dualdynamic node hybrid flip-flop using 120 nm CMOStechnology. In this paper first they have compared anddiscussed about some existing flip-flops such as HLFF, SDFFand XCFF. Drawbacks of this XCFF flip-flop were unwantedtransitions and due to this unwanted transitions powerdissipation problem will occur. Comparison of the dualdynamic node hybrid flip flop (DDFF) showed that it exhibitslower power dissipation along with area [2].

Karthika have designed Power efficient hybrid pulsed flip-flop(HPFF) with embedded logic module (HPFF-ELM) based ontransmission gate scheme. They compared three existingdesigns of dual dynamic node flip-flop such as Conditionaldata mapping flip-flop (CDMFF), cross charge controlled flipflop(XCFF), Dual dynamic flip-flop (DDFF) and DDFF-ELMwith the proposed design of the HPFF and HPFF-ELM. TheHPFF consists of less number of transistors by usingtransmission gate instead of back-to-back inverters in theprevious XCFF and DDFF architectures. Thus the layout areaand delay consumed by the design is reduced. Also thenumber of transistors used by HPFF-ELM is very less whencompared with DDFF-ELM and SDFF-ELM. Thus the layoutarea and the delay are also reduced. The power dissipationproduced after embedding logic functions is decreaseddramatically. A comparison of the proposed

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flip-flop with theconventional flip-flops showed that it exhibits lower powerdissipation along with speed performances. [3].

Varuna RTV have designed Dual Dynamic Edge TriggeredLow Power Flip-Flop Featuring ELM where edge triggering isprovided by the NMOS. The proposed design reduces thepower consumption up to 20% compared to the conventionalflip-flops. Also A high speed ring counter using digital CMOSgate logic components by the DDFF structure is also designedwhich is well suited for modern high performance circuits [4].Omid Sarbishei have proposed An Efficient Implementation ofFlip–Flops with Embedded Logic. This paper presents severalefficient architectures of dynamic/static edge-triggered flip–flops with a compact embedded logic. The overlap-based DFFis proposed in which lookup table is implemented in pull downnetwork (PDN). Also the overlap-based logic cells becomemore efficient when the complexity of their embedded logicfunction increases. The main advantage is that this approachimproves static power consumption due to the reduction of ptypeMOS (pmos) transistors and voltage swing in internalnodes, which makes it even more efficient in below 0.18 mCMOS technologies [5].

R Siva Kumar have designed Low-Power Efficient DoubleEdge Trigger Flip Flop using Tanner EDA tool. In Doubleedgetriggered Flip-Flops data signal changes on both therising and falling clock edges. Thus, results in low clock swingand it leads to lower power consumption. The proposed designsolves the long discharging path problem in conventionalexplicit type pulse-triggered FF (P-FF). In this paper, a newlow power DDFF was proposed. Also 4-b ring counter usingDDFF is designed. There results showed that the proposedDDFF is efficient in terms of power, delay and power delayproduct [6].

Hinamalviya has compared Various Leakage Power Reduction Techniques For CMOS Circuit Design such as sleep mode approach, stack approach, sleepy keeper andsleepy stack method. The sleepy keeper method achievesleakage power reduction equivalent to the sleep and otherapproaches with the advantage of maintaining exact logicstate. But the main disadvantage is that, sleepy keeper causeadditional dynamic power consumption, approximately 15%more than the base case. The sleepy stack well-known lowleakagetechniques which have a combined structure of forcedstack, sleep transistor which achieves ultra-low leakage powerconsumption while retaining state. Their design carried outcomparison of sleepy stack method of 2 input NAND gate thathave achieved dynamic power reduction upto 20.03%, staticpower reduction upto 65.91%, delay increment upto 101.5%and PDP upto 40.20% [7].

Shahriar Jalal Nibir have proposed A New Leakage Reduction Method for Ultra Low Power VLSI Design for PortableDevices. They compared existing designs of Leakage power reduction such as Sleep Transistor Technique, Sleepy StackTechnique, Sleepy Keeper Technique, Dual Sleep Technique, Dual Stack Technique. The comparative analysis showed thatthe stacked sleep transistor offers superior static and dynamicpower reduction [8].

Tripti Mehta have proposed various Low Power Consumption Techniques in a VLSI Circuit such as sleep, stack, sleepykeeper and reverse body bias with sleep and stack. Theirsimulation results of power consumption are done on aTANNER EDA tool at 90 nm technology which showed thatthe proposed XNOR circuit using reverse body with sleep andstack achieves up to 60% less power consumption ascompared to the base case [9].

Jun Cheol Park have proposed Sleepy Stack LeakageReduction. He proposed ultra-low leakage CMOS circuit structure which is call “sleepy stack”. Sleepy stack method isstate-saving technique where circuit state (present value) isretained and thus achieves ultra-low leakage powerconsumption. A state-saving technique has an advantage overa state-destructive technique is that the circuitry canimmediately resume operation at a point much later in timewithout having to somehow regenerate state [10]. SleepyStack approach can achieve more power savings with theadvantage of less delay as compared to the forced stacktechnique.

III. COMPARISON OF LEAKAGE REDUCTIONTECHNIQUES

Leakage current is a major concern for low-power, highperformancedigital CMOS circuits thus various methods areused to reduce leakage current but it limit up to the certainapplication. The Base Case (conventional CMOS) containsonly the PMOS network and the NMOS network and thereforeno reduction in leakage current. It is a state saving techniqueand has a minimum area requirement.The Forced stack technique is Easy to implement and thus usefor Leakage savings but at the same time Propagation delayincreases. Whereas the Sleep transistor method provides goodreduction in leakage power, but it is a state destructivetechnique (current Boolean output value of the circuit mightbe lost). The sleepy stack method is State Saving Techniquealso it has advantage over forced stack technique is that itrequires Less delay compared to forced stacking. In activemode, sleepy stack approach is suitable for faster

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circuitoperation. Sleepy stack approach is use to reduced Leakagepower as well as average power drastically thus useful toenhance power performance.

IV. SLEEPY STACK STRUCTURE

In our proposed approach, Leakage power reductiontechnique name as "sleepy stack." The sleepy stack techniquehas a combined structure of the forced stack technique and thesleep transistor technique. The Sleepy Stack Techniquecombines the Stack & Sleep techniques. In Fig 2 the existingtransistors divided into two half size transistors in the SleepyStack technique like as Stack technique. If dual-Vth values areavailable, high-Vth transistors are used. Between the dividetransistors one of sleep transistor will be added in parallel.

Fig 3 shows stack technique where the existing transistor are Breaking down into two half size transistors. Stacked transistors suppress leakage current while saving state & Sleep transistors are turned off during sleep mode. Thus we reduce the leakage power and overall total power at high speed by replacing the CMOS inverter pair by sleepy stack inverter pair. Leakage power reduction can be classified into two ways.

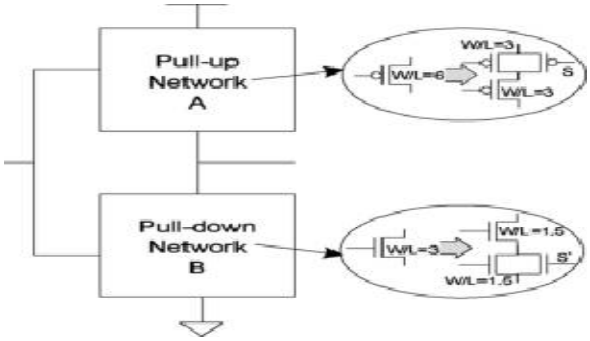

Fig. 2 Sleepy Stack Structure [10]

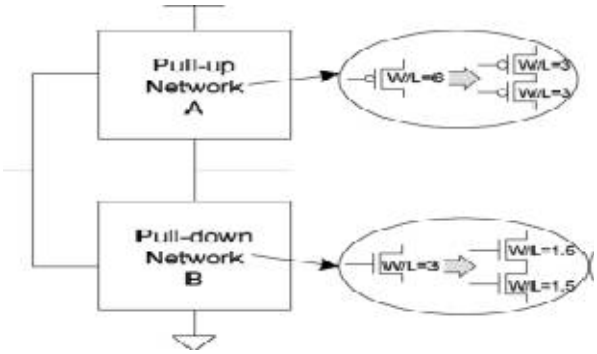

Fig. 3 Forced Stack structure [10]

First is State destructive technique which does not retainexact logic state when the circuit is switched to the othermodes and second is the state saving technique whichretains the exact logic state. State-destructive techniques cutoff transistor (pull-up or pull down or both) networks fromsupply voltage or ground using sleep transistors. These typesof techniques are also called gated-Vdd and gated- Gnd (notethat a gated clock is generally used for dynamic powerreduction) [10].

A state-saving technique has an advantage over a statedestructivetechnique in that with a state-saving technique thecircuitry can instantly resume operation at a point much later1234in time without having to somehow regenerate state. Wecharacterize each low-leakage technique according to thiscriterion [10]. Thus this sleepy stack inverter pair is statesaving technique which is used for leakage power reductionof flip flop in sleep mode and total power is also reduced byrunning the flip flop in active mode.

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V. PROPOSED WORK

In Dual Dynamic Node Hybrid Flip-Flop (DDFF), there aretwo nodes in the circuit among which one is purely dynamicand another is pseudo-dynamic. So, it is called as dualdynamic. Fig. 4 shows schematic of DDFF. As it is havingdynamic frond end and static output, it is hybrid in nature. Theoperation of the flip-flop can be divided into two phases. Firstare evaluation phase, when CLK is high, and the pre-chargephase, when CLK is low. The proposed DDFF architectureacts both as static and dynamic circuits. Thus the operation ofDDFF is based on dynamic logic principles. The flip flop requires two phase to operate based on the clock input to the circuit.

In evaluation phase- The architecture exhibits negative setup time since the short transparency period is defined by the 1-1 overlap CLK and CLK B allows the data to be sampled even after the rising edge of CLK before CLK B falls low. As CLK falls low, the circuit enters in the pre-charge phase and node X1 pulled high through PM0, switching the state of INV1-2. During this period node X2 is not actively driven by any transistor, it stores the charge dynamically. If D is low (prior to the overlap period), node X1 remains high and node X2 pulled low through NM3 as the CLK goes high. Thus, node QB is charged high through PM2 and NM4 is held off. At the end of the evaluation phase, as the CLK falls low, node X1 remains high and X2 stores the charge dynamically [1].

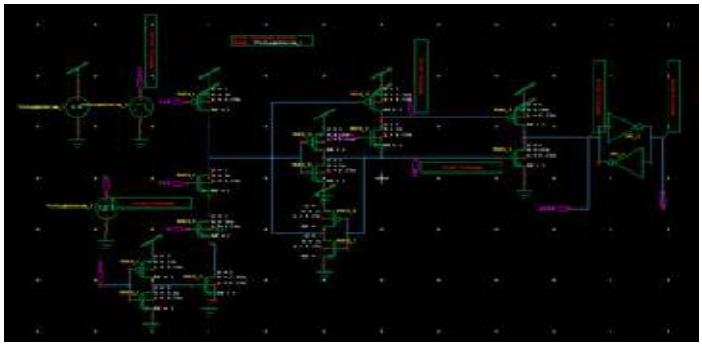

Fig. 4 Proposed DDFF

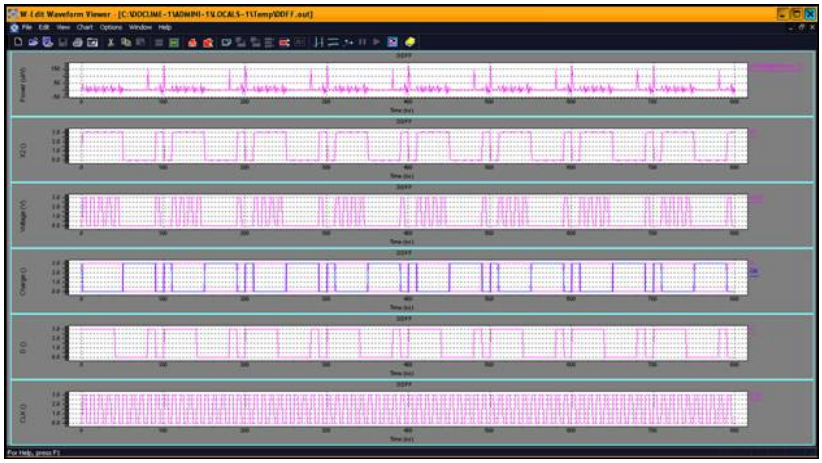

Fig. 5 Waveform of DDFF

Fig. 5 shows waveform of DDFF. The minimum time periodbefore the CLK edge is setup time and the minimum time period after the CLK edge is the hold time, where the datashould be stable so that proper sampling is possible. Heresetup time and hold time depend on the CLK overlap period.

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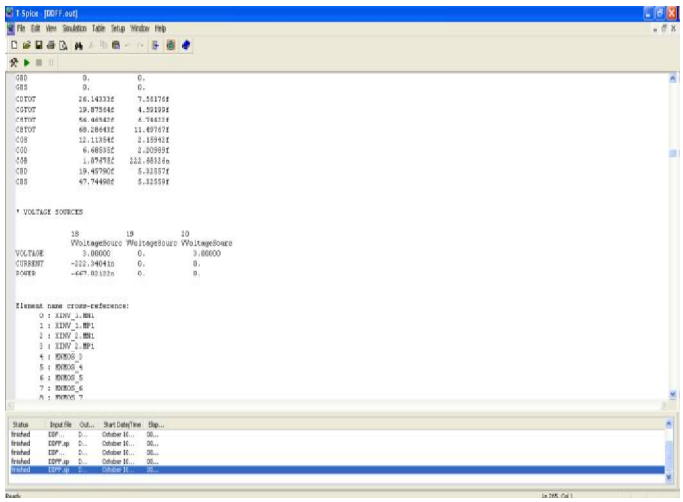

Fig.6 Power Analysis of DDFF

VI. RESULTS

The Power analysis of DDFF design using 90nm CMOStechnology shows that it requires 0.667uW of power. In futureDDFF design using Sleepy Stack method achieving ultra lowleakage power consumption and offers a power reduction upto 45% which can be use for low power efficiency.

VII. CONCLUSION

This paper presents a comparative study of different low power design techniques for dual dynamic node hybrid flipflop (DDFF) and embedded logic module based on DDFF by using sleepy stack technique which can achieve smaller transistor delay than the forced stack technique and use for ultra low leakage power consumption. The main advantage of the sleepy stack approach is the ability to use high- Vth which causes low leakage current and hence results in low leakage power. Vth of sleepy stack method is 69% higher than that of the forced stack. This higher Vth can potentially result in large leakage power reduction. Thus it can be used for future IC'S for low power efficiency. The present study provides a proper choice for leakage power minimization technique for a specific VLSI application. Thus sleepy stack technique is a feasible solution for designer in designing low power CMOSVLSI circuit more efficiently.

REFERENCES

[1] KalarikkalAbsel, Lijo Manuel, and R. K. Kavitha "Low Power DualDynamic Node Pulsed Hybrid Flip-Flop Featuring Efficient EmbeddedLogic " 2013 IEEE Transactions On Very Large Scale Integration (VlSI)Systems, VOL. 21, NO. 9, September 2013.I. S. Jacobs and C. P. Bean,"Fine particles, thin films and exchange anisotropy," in Magnetism, vol.III, G. T. Rado and H. Suhl, Eds. New York: Academic, 1963, pp. 271–350.

[2] Meghana Pelleti1, T. Krishna Murthy2, K. Neelima3 "Low-Power andLow Power Dual Dynamic Node Pulsed Hybrid Flip-Flop FeaturingEfficient Embedded Logic for Low Power CMOS VLSI Circuits Using120nm Technology" International Journal Of Emerging TechnologyAnd Advanced Engineering, Volume 4, Issue 8, AUGUST 2014.

[3] N. Karthika1, S. Jayanthy2 "Design of Hybrid Pulsed Flip-FlopFeaturing Embedded logic" IOSR Journal Of Vlsi And SignalProcessing (IOSR-JVSP, Volume 4, Issue 2, VER. I (MAR-APR. 2014).

[4] Varuna RTV1*, Prabhakaran G2, Marimuthu CN3 "Dual Dynamic EdgeTriggered Low Power Flip-Flop Featuring Elm" ISSN 2348-375XUnique Journal Of Engineering And Advanced Sciences 02 (01), JANMAR2014.

[5] Omid Sarbishei and Mohammad Maymandi - Nejad "A Novel OverlapBased Logic Cell: An Efficient Implementation of Flip Flop WithEmbedded Logic" IEEE Transactions On Very Large Scale Integration(VLSI) Systems, VOL. 18, NO. 2, February 2010,

[6] R Siva Kumar, T SrinivasaPadmaja," Design of a Low-Power EfficientDouble Edge Trigger Flip Flop" International Journal Of EmergingTrends In Engineering Research (IJETER), VOL. 3 NO.6, PAGES :248- 251 (2015).

[7] Hinamalviya and Prof. Murli Manohar Hinnwar "Comparison ofVarious Leakage Power Reduction Techniques for CMOS CircuitDesign" International Journal Of Engineering Research & Technology(IJERT), ISSN: 2278-0181, VOL. 2 Issue 10, October – 2013.

[8] Shahriar Jalal Nibir, Md. RifatAlam Siddique and Asif JahangirChowdhury "A New Leakage Reduction Method for Ultra Low PowerVLSI Design for Portable Devices" 2nd International Conference OnPower, Control And Embedded Systems IEEE-2012.

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[9] Shahriar Jalal Nibir, Md. RifatAlam Siddique and Asif JahangirChowdhury "A New Leakage Reduction Method for Ultra Low PowerVLSI Design for Portable Devices" 2nd International Conference OnPower, Control And Embedded Systems IEEE-2012.
[10] Jun Cheol Park and Vincent J. Mooney III, IEEE. "Sleepy StackLeakage Reduction", IEEE Transactions On Very Large ScaleIntegration (VLSI) Systems, VOL. 14, NO. 11, November 2006
[11] N. Waste and K. Eshraghian, Principle of CMOS VLSI Design: ASystem Prospective, 2nd ed. New York: Addison –Wesley, 1993.