Silicon Electronic Photonic Integrated Circuits for High Speed Analog to Digital Conversion

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Abstract: Integrated optical components on the silicon platform and optically enhanced electronic sampling circuits are demonstrated that enable the fabrication of a variety of electronic-photonic A/D converter chips surpassing currently available technology in sampling speed and resolution.

INTRODUCTION

The goal of this program is to leverage the low jitter properties of mode-locked lasers to develop an electronic-photonic integrated circuit (EPIC) that facilitates high speed analog-to-digital conversion (ADC) beyond the bottleneck set by electronic jitter. Several photonic ADC techniques have been investigated in recent years [1,2]. The photonic ADC architecture pursued here in the form of an EPIC is known as time-interleaved optical sampling using wavelength-division multiplexing (WDM) [3] techniques.

OPTOELECTRONIC ADC-CHIP

The envisioned EPIC is shown in Figure 1. A chirped optical clock signal from a mode-locked laser is channelized in time using precisely-tuned WDM filters to create time-interleaved optical sampling signals, each

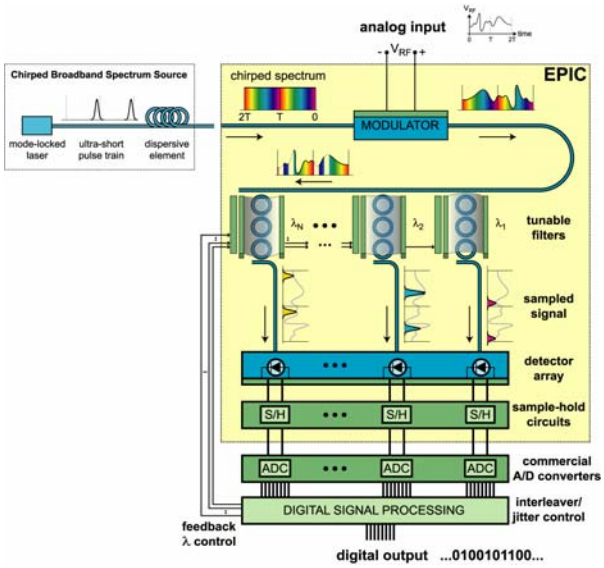

Figure 1: Schematic layout of EPIC for high-speed ADC.

operating at the rate of the mode-locked laser. The total sampling rate is then the optical clock rate times the number of WDM channels. However, in order to realize the high resolution, the sampling times of the interleaved channels must be uniform, the converter gains from each channel must be closely matched, and the sample memory effects must be minimal. These characteristics require monitoring and very tight feedback control of the WDM filters which is most easily possible with an EPIC. The ADC chip requires the development of a number of devices: WDM filter banks with large FSR and precise control of relative resonance frequencies, wideband optical modulators, Ge- photodetectors, and low jitter femtosecond lasers, potentially also integrated. All these devices and techniques must be integrated on a CMOS compatible technology platform. In the following we discuss progress made towards some of the key components for this optoelectronic sampling technology.

HIGH INDEX CONTRAST FILTER BANK

The proposed ADC chip requires filters with large free spectral range (FSR) and low loss. These two key requirements call for microring filters fabricated in a high-index contrast (HIC) material system.

The microring resonator filter designs used for fabrication of the filter banks presented here are based on to the design described in [3]. By utilizing this design with the HIC materials of silicon-rich silicon nitride (n =2.2 @ 1550 nm) forming the core, and silicon dioxide (n =1.455 @ 1550nm) or air cladding a very wide FSR of 20 nm is realized. The filter design was fine tuned to achieve the objective of a 3 dB bandwidth of 50 GHz and less than 30 dB adjacent channel crosstalk for 150 GHz spaced channels. The critical feature size of the gap between the bus and ring waveguides is 160 nm for these filters (Figure 2a).

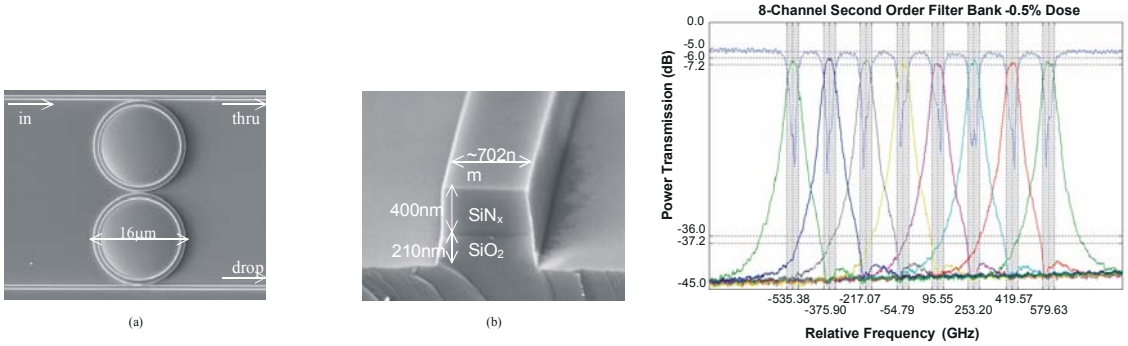

Figure 2: (a) Top view of second order microring resonator filter. (b) Cross-section view of bus waveguide showing smooth vertical sidewalls. (c) Through- and drop-port characteristics of filter bank with second order single stage filters and 159 GHz channel spacing. Frequencies are all relative to 1540 nm.

Direct-write scanning electron beam lithography (SEBL) was used due to its combination of high resolution and high level of dimensional control. The basic fabrication process used is similar to that described in [4].

Controlling the resonant frequency of HIC microring resonator filters requires an extremely high level of dimensional control. To overcome the discretization in e-beam step size, e-beam dose modulation is used. This technique combined with changing the radius was used to make 8-channel second, order filter banks with average channel spacings of about 159±6 GHz, thereby addressing and demonstrating accurate channel spacing and control. The filter showed a channel bandwidth of 46.5GHz, a drop loss averaged over 40 filters of 1.5±0.5 dB and a adjacent channel crosstalk of less than -30 dB,.(Figure 2(b)). Fine tuning of filters to an exact frequency grid by thermal means (heaters) is in progress.

HIGH SPEED SILICON MODULATORS

For a high speed electro-optical modulator the well known plasma dispersion effect in silicon is exploited [5]. Mach-Zehnder modulators with figure of merit (FOM)= $V_\pi L$= 0.2, 50% modulation up to 5GHz have been demonstrated [6].

GE PHOTODETECTORS

It has been demonstrated in Ultra High Vacuum Chemical Vapor Deposition (UHVCVD) systems that depositing a low temperature Ge layer (seed layer), followed by the deposition of a high temperature layer (cap layer) with subsequent annealing, can create a smooth, planar Ge film on a (100) silicon substrate with threading dislocation density on the order of 10^7 cm^{-2} [7]. This two-step deposition process has been successfully adapted to an LPCVD system (Applied Materials Epitaxial Reactor). Thus, integrating Ge

films onto silicon (Ge/Si) substrates into a CMOS-compatible process is an attractive goal for making arrays of on-chip detectors that can be used in an electronic-photonic ADC chip.

Approximately 2 µm-thick intrinsic Ge films were deposited on p+ (100) Si substrates, and capped with a 0.2 µm N+ polysilicon layer to create a vertical *pin*-photodiode (Figure 3(a) inset). The IV characteristics of the photodiodes fabricated with the blanket Ge films are shown in Figure 3(a).

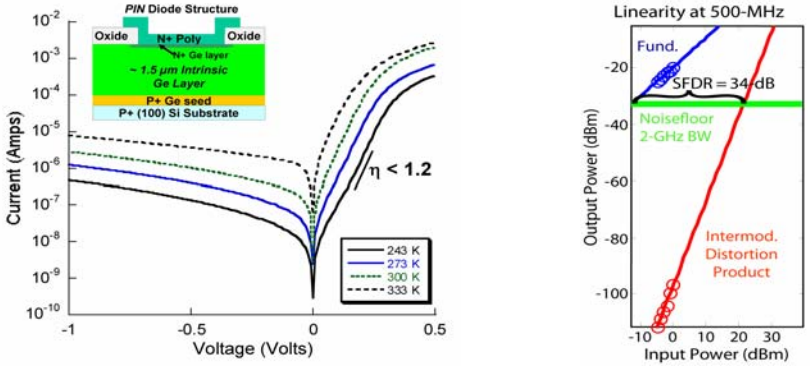

Figure 3: (a) IV characteristics of a 100x100 µm diode as a function of temperature. (b) Spur-free dynamic range measurement on a 100x100µm Ge photodiode. The diode was biased at -3V

At 1.55 µm wavelength, the Ge film has a responsivity of 0.5 A/W. The frequency response of a 20 µm x 100 µm photodiode at a wavelength of 1.04 µm and reverse biased with5 volt is measured to have a 3dB frequency of 1.4 GHz. For the ADC application it is important that the detector is highly linear for the dynamic range requested. To characterize the linearity, we measured the spur-free dynamic range (SFDR), shown in Figure 3(b). For the current devices the SFDR is 34-dB which would allow for 5.6 effective bits if it was the limiting factor in the system's performance.

CONCLUSIONS

Integration of HIC optical devices on the Si-technology platform together with electronics may lead to advanced signal processing capabilities in the near future. Here in brief, we discussed only two of the key components of such a system – filter banks and detectors. The presentation will in addition report progress made towards the other necessary components such as modulators and on-chip modelocked lasers, novel sampling techniques, as well as integration of these devices in a CMOS compatible fabrication process.

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