A Novel Nanometric Fault Tolerant Reversible Subtractor Circuit

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Abstract: Reversibility plays an important role when energy efficient computations are considered. Reversible logic circuits have received significant attention in quantum computing, low power CMOS design, optical information processing and nanotechnology in the recent years. This study proposes a new fault tolerant reversible half-subtractor and a new fault tolerant reversible full-subtractor circuit with nanometric scales. Also in this paper we demonstrate how the well-known and important, PERES gate and TR gate can be synthesized from parity preserving reversible gates. All the designs have nanometric scales.

Keywords: Fault tolerant, nanometric circuits, nanotechnology, quantum computing, reversible logic, subtractor

INTRODUCTION

Reversible circuits are composed of reversible gates. In this circuits information don't be lost. Reversible circuits can produce unique output from each input and vice versa, hence, there is a one-to-one correspondence between input and output vectors (Thapliyal and Srinivas, 2006). So a reversible logic gate has an equal number of inputs and outputs (k ×k) (Babu and Chowdhury, 2005).

In ideal conditions, a reversible circuit has zero internal power dissipation because, it does not lose information. Under R. Landauer's research in the early 1960s, the amount of energy dissipated for every irreversible bit operation is given by KTLn2 joules, where K = $1.3806505 \times 10^{-23}$ J/K is the Boltzmann's constant and T is the absolute temperature at which operation is performed. But in 1973, Bennett showed that KTLn2 joules of energy can be saved from a system as long as the system permits the regeneration of the inputs from produced outputs (Haghparast et al., 2009; Haghparast and Navi, 2008a; Thapliyal and Gupta, 2006).

A reversible gate with n-inputs and n-outputs is called a n × n reversible gate (Sastry et al., 2006). In a n × n reversible function, there are 2^n input rows and 2^n output rows in its truth table. In fact the output rows are a permutation of the input rows in the truth table (Kerntopf, 2002; Hung et al., 2006). Direct fan-outs from the reversible gate and feedbacks from a gate output directly to its inputs are not allowed (Sastry et al., 2006). Classical logic gates are called irreversible since they cannot uniquely reconstruct the input vector states from the output vector states.

Synthesis and designing of a reversible gate is different from traditional logic gates (Haghparast and Sheikh, 2011). Therefore, constructing a fault tolerant reversible circuit is much more difficult than a conventional logic circuit (Parhami, 2006). In this paper, we propose a fault detection method based on parity preserving reversible logic gates.

PRIMARY DEFINITIONS

Some of the main measures in synthesis a reversible logic circuit are: Number of reversible logic gates, Number of garbage outputs, Number of constant inputs, Total quantum cost, and total logical calculations (Haghparast et al., 2009).

Garbage outputs: One of the most important parameters in designing a reversible circuit is its garbage outputs (Hasan et al., 2004). In a reversible logic gate number of inputs and outputs is equal but all the outputs are not expected. The number of outputs added to make an n-input k-output function reversible is named garbage outputs. In fact they are needed to maintain reversibility. A heavy price is paid for every garbage output (Parhami, 2006).

So, one of the major challenges in reversible logic synthesis is to minimize the garbage outputs (Hasan et al., 2004; Thapliyal et al., 2009).

Quantum cost: The quantum cost of a reversible gate is the number of 2×2 reversible gates or quantum logic gates required in designing it. The quantum cost of all

reversible 2×2 gates is taken as 1 and the cost of all the1×1 reversible gates such as NOT gate is assumed to be zero. Thus, any reversible gate is performed by using 1×1 NOT gates and 2×2 reversible gates (Thapliyal and Ranganathan, 2009).

Constant inputs: The inputs that are added to a n × k function to make it reversible are called constant inputs (Haghparast *et al*., 2009).

Reversible logic gates:
NOT gate: NOT gate is a 1×1 gate represented as shown in Fig. 1. Since it is a 1×1gate, its quantum cost is zero (Thapliyal and Ranganathan, 2009; Rangaraju *et al*., 2010).
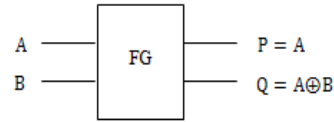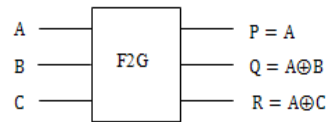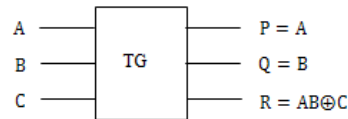
Feynman Gate (FG): Among the exist 4! = 24 2×2 reversible gates, Feynman gate which is shown in Fig. 2 is the most important gate. It can be represented as $I_v = (A, B)$ $O_v = (P = A, Q = A \oplus B)$, where, I_v and O_v are input and output vectors. Since it is a 2×2 gate, it has a quantum cost of 1 Thapliyal and Ranganathan (2009) and Saiful (2010).

Feynman double Gate (F2G): Feynman double gate as a 3×3 reversible gate is shown in Fig. 3. It can be showed as:

$$I_v = (A, B, C) , O_v = (P = A, Q = A \oplus B, R = A \oplus C)$$

where, I_v nd O_v are input and output vectors respectively. F2G gate is a Feynman gate with one more input and one more output which the control input 'A' defines a second controlled NOT operation (Haghparast and Navi, 2008b). It has the quantum cost of 2.
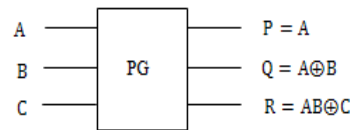
Toffoli Gate (TG): Toffoli gate is a 3×3 two-through reversible gate as shown in Fig. 4. It means that two of its outputs are same as the inputs. This gate can be represented as:

$$I_v = (A, B, C) , O_v = (P = A, Q = B, R = AB \oplus C)$$

where, I_v and O_v are input and output vectors respectively. Toffoli gate is one of the most popular reversible gates and it has quantum cost of 5 (Thapliyal and Ranganathan, 2009; Chung and Wang, 2007).
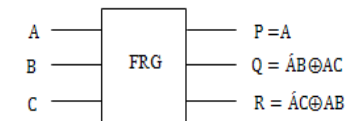
Peres Gate (PG): Peres gate also known as New Toffoli Gate (NTG) is a 3×3 reversible logic gate. It can be described as:

$$I_v = (A, B, C) , O_v = (P = A, Q = A \oplus B, R = AB \oplus C)$$

where, I_v and O_v are input and output vectors respectively. This gate is constructed by a Toffoli gate that followed by

Fig. 1: NOT gate

Fig. 2: Feynman gate

Fig. 3: Feynman double gate

Fig. 4: Toffoli gate

Fig. 5: Peres gate
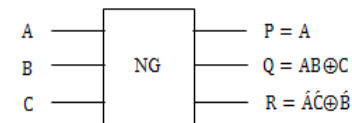

Fig. 6: Fredkin gate

Fig. 7: New gate

a Feynman gate. It is shown in Fig. 5. Its quantum cost is 4 which is less than quantum cost of a Toffoli gate (Haghparast *et al*., 2009).

Fredkin Gate (FRG): Fredkin gate is shown in Fig. 6. It can be described as:

$$I_v = (A, B, C) , O_v = (P = A, Q = \acute{A}B \oplus AC, R = \acute{A}C \oplus AB)$$

where, I_v and O_v are input and output vectors, respectively. It is known as swap gate. If control input
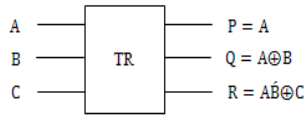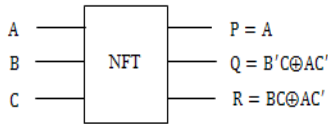
Fig. 8: TR gate

Fig. 9: New fault tolerant gate

A = '0' then inputs B and C are showed clearly in outputs, else if A = '1' then inputs B and C are swapped and showed in outputs. It has quantum cost of 5 (Haghparast and Sheikh, 2011; Saiful, 2010).

New gate (NG): Another one of the interesting gate is New gate which is represented in Fig. 7. The advantage of selecting the New gate is that, this gate can produce all the basic gates. It has the quantum cost of 7 (Hasan *et al.*, 2003; Haghparast and Navi, 2007).

TR gate: TR gate is a 3×3 reversible gate and it has mapping between its inputs and outputs as:

$$I_v = (A, B, C), O_v = (P = A, Q = A \oplus B, R = AB' \oplus C)$$

where, I_v and O_v are input and output vectors, respectively. It is shown in Fig. 8. The quantum cost of this gate is 6. TR gate can work singly as a half-subtractor circuit furthermore, with two TR gates we can design a reversible full-subtractor (Thapliyal and Ranganathan, 2009).

New Fault Tolerant (NFT):
NFT gate can be defined as:

$$I_v = (A, B, C), O_v = (P = A \oplus B, Q = B'C \oplus AC',$$
$$R = BC \oplus AC')$$

where, I_v and O_v are input and output vectors, respectively. This gate is shown in Fig. 9 and its quantum cost is 5. It can implement all Boolean functions (Haghparast and Navi, 2008b).

Parity preserving reversible gates: Parity preserving is one of the error detection methods in digital logic systems. Using error detection methods in reversible logic circuits is together with some problems because in these circuits, fan-out and loops are not permitted.

Table 1: Truth table of the parity preserving F2G gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	0	0

Table 2: Truth table of the parity preserving FRG gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

Table 3: Truth table of the parity preserving NFT gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	1	0	0
0	1	1	1	0	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	0	1	1
1	1	1	0	0	1

Consequently using these ways may increase the number of gates and number of garbage outputs (Haghparast and Navi, 2008b).

For parity preserving a reversible circuit, each gate must be parity preserving. So for constructing parity preserving reversible circuits we need to parity preserving reversible gates. Simply we can verify that which gate is parity preserving by comparing the input parity to the output parity. In the other words, these gates satisfy the equation:

$A \oplus B \oplus C = P \oplus Q \oplus R$. (Haghparast and Navi, 2008 a,b; Parhami, 2006).

Among the discussed reversible gates, only the gates F2G, FRG and NFT are parity preserving gates. Which means that triple of them satisfy the relation $A \oplus B \oplus C = P \oplus Q \oplus R$.

Truth tables of F2G, FRG and NFT gates are presented in Table 1, 2 and 3, respectively (Haghparast and Navi, 2008 a,b).

RESULTS ANALYSIS

New design of parity preserving reversible subtractor circuits: Half-subtractor circuit executes $A - B$ operation if A and B be input variables thus, the equations of the borrow and difference are as follows: *Diff* = $A \oplus B$, Borr = $A'B$. Similarly, Full-ubtractor circuit performs
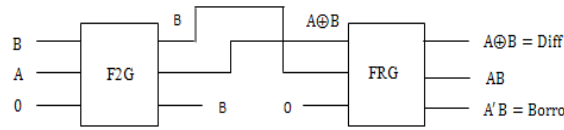
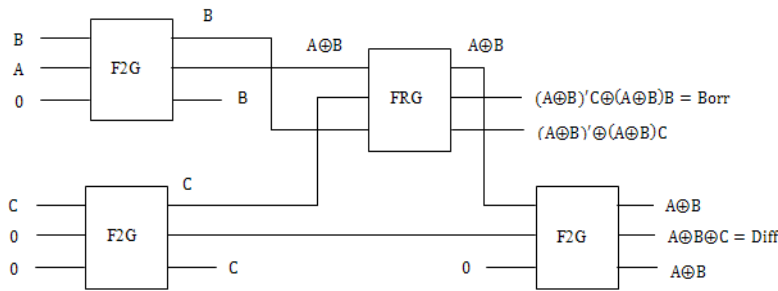Fig. 10: Proposed parity preserving reversible half-subtractor circuit

Fig. 11: Proposed parity preserving reversible full-subtractor circuit
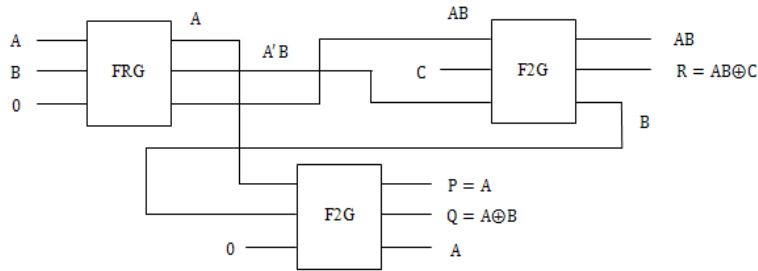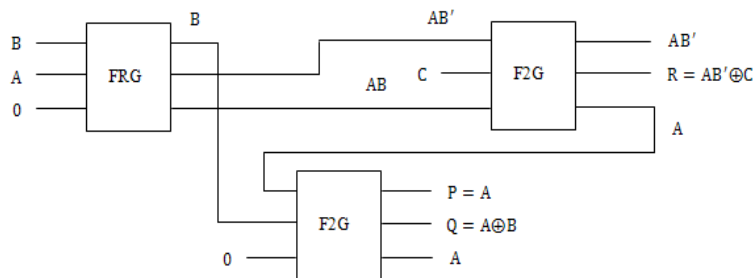

Fig. 12: Proposed parity preserving PERES gate

Fig. 13: Proposed parity preserving TR gate

A‒B‒C operation if A, B and C be input vectors so, the equations of borrow and difference are as follows:

$$Diff = A \oplus B \oplus C, Borr = A'B \oplus A'C \oplus BC$$

(Thapliyal *et al.*, 2005)

Although there are some works on reversible subtractor circuits but so far haven't reported any acts on reversible subtractor circuits with parity preserving. In this section, we show our new proposed design of parity preserving reversible half-subtractor circuit and parity preserving reversible full-subtractor circuit. The circuit shows how F2G gate and FRG gate can be used to design a parity preserving reversible half-subtractor and parity preserving reversible full-subtractor.

Parity preserving reversible half-subtractor circuit:
The proposed parity preserving half-subtractor circuit is shown in Fig. 10. As you see, this circuit is composed of two gates F2G and FRG. Since the quantum cost of F2G

and FRG are 2 and 5, respectively so, the quantum cost of this circuit is 7. The proposed circuit requires two constant inputs and produces two garbage outputs.

Our proposed parity preserving half-subtractor circuit can be used in constructing fault tolerant reversible circuits.

Parity preserving reversible full-subtractor circuit: The suggested reversible parity preserving full-subtractor can be built using these gates of F2G gate and one FRG gate. This circuit can be implemented as shown in Fig. 11 thus, the proposed circuit uses 4 reversible parity preserving gates. It produces 4 garbage outputs and requires only one constant input. Constructing the proposed circuit has been resulted in generation of the quantum cost of 11.

Our proposed parity preserving full-subtractor circuit can be used for designing fault tolerant reversible systems which is the necessary requirement of nanotechnology based systems.

New design of parity preserving Peres gate: In this part we demonstrate how Peres gate can be realized by using three parity preserving reversible gates, which is shown in Fig. 12. Thus, this circuit requires three gates (two F2G gates and one FRG gate) and produces 2 garbage outputs. The proposed parity preserving PG gate uses two constant inputs and it has the quantum cost of 9.

New design of parity preserving TR gate: In this section we show how FRG gate and F2G gate can be used to implement the TR gate. Our proposed design is depicted in Fig. 13. The proposed reversible parity preserving circuit needs three reversible gates (one FRG gate and two F2G gates) and it produces two garbage outputs. Also, it has the quantum cost of 9.

CONCLUSION

In this study, we proposed a novel parity preserving reversible half-subtractor circuit and a novel parity preserving reversible full-subtractor circuit. We also designed parity preserving PG implementation using two kinds of parity preserving gates. Furthermore we showed the parity preserving TR gate implementation. All the scales are in the nanometric area.

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