Leakage Power Reduction for Deeply-Scaled FinFET Circuits Operating in Multiple Voltage Regimes Using Fine-Grained Gate-Length Biasing Technique

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***Abstract*—With the aggressive downscaling of the process technologies and importance of battery-powered systems, reducing leakage power consumption has become one of the most crucial design challenges for IC designers. This paper presents a device-circuit cross-layer framework to utilize fine-grained gate-length biased FinFETs for circuit leakage power reduction in the near- and super-threshold operation regimes. The impacts of Gate-Length Biasing (GLB) on circuit speed and leakage power are first studied using one of the most advanced technology nodes – a 7nm FinFET technology. Then multiple standard cell libraries using different leakage reduction techniques, such as GLB and Dual-V_T, are built in multiple operating regimes at this technology node. It is demonstrated that, compared to Dual-V_T, GLB is a more suitable technique for the advanced 7nm FinFET technology due to its capability of delivering a finer-grained trade-off between the leakage power and circuit speed, not to mention the lower manufacturing cost. The circuit synthesis results of a variety of ISCAS benchmark circuits using the presented GLB 7nm FinFET cell libraries show up to 70% leakage improvement with zero degradation in circuit speed in the near- and super-threshold regimes, respectively, compared to the standard 7nm FinFET cell library.**

I. Introduction

With the severe restrictions placed by cooling and battery life constraints today, power efficiency has become the key to sustaining a continued performance enhancement in future VLSI circuits, since it directly affects the thermal margin, circuit performance and reliability [1][2][3]. To reduce power consumption of ICs, *Ultra-Low Voltage* (ULV) CMOS operations, where the supply voltage is scaled down to near or below the threshold voltage (V_T) of transistors, have been shown effective with 5-20X energy savings [4]. The ULV operations can achieve the minimal energy consumption and benefit performance-relaxed and energy-constrained applications such as portable wireless devices, implantable medical devices, and sensor network nodes [5].

However, it is well known that the steady down-scaling of the feature size of bulk CMOS technology has resulted in *Short-Channel Effects* (SCE), such as *Drain Induced Barrier Lowering* (DIBL) and V_T roll-off [6]. The SCEs limit the bulk CMOS transistor scaling in deep-submicron regions [7][8], which inevitably erodes the expected power efficiency achieved by applying the ULV operations in CMOS technology. The multi-gate or tri-gate transistor structures such as FinFETs are proposed to rejuvenate the chip industry by rescuing it from the SCEs [8]. The improved electrostatic integrity of FinFET devices can alleviate SCEs and further lower supply voltages to improve the power efficiency, making such devices especially advantageous for near- and super-V_T operations [1]. It has been reported that FinFET devices are estimated to be up to 37% faster while consuming less than half the dynamic power or cut static leakage current by as much as 90% compared to the bulk CMOS devices [8]. Besides, the low (or absence of) channel doping in FinFETs may eliminate the random dopant fluctuation, which is a major source of process-induced variations in conventional CMOS technology [1]. Therefore, FinFETs are promising device candidates for bulk CMOS at the 22-nm technology node and beyond [8]. In addition to the SCEs, the down-scaling has also resulted in an explosive increase in leakage current in recent generations [6]. Many circuit-level techniques, such as gate sizing [9], *Gate-Length Biasing* (GLB) [3][10], sleep mode approach [2], stack mode approach [2], multi-V_{dd} [11] and Dual-V_T [2][9], have been commonly leveraged to overcome the issue of high leakage power in conventional CMOS technology.

However, there lacks a throughout investigation of those power saving techniques aforementioned for the deep-scaled FinFET circuits operating in near- and super-V_T voltage regimes. In this paper, we conduct a detailed investigation by developing a device-circuit cross-layer framework comprising four steps: (i) we first design and optimize deeply-scaled FinFET devices using the Synopsys TCAD suite [12]; (ii) we build equivalent circuit models of FinFET devices and extract parameters in a Verilog-A format that is compatible to HSPICE for fast simulations in circuit level [13][14]; (iii) based on the device models, we generate Liberty-formatted standard cell libraries that support leakage power saving techniques, such as GLB and Dual-V_T techniques in two different operation regimes, namely, the near-V_T and super-V_T regimes; (iv) using the libraries, we synthesize various benchmarks and evaluate the effectiveness of the leakage power saving techniques.

The contributions of this work are threefold. First, we carry out a detailed analysis on a fine-grained GLB technique. Circuit simulation results show a significant leakage power reduction of about 70% in both near- and super-V_T regimes. Meanwhile, the fine-grained GLB technique also introduces 27% and 13% penalties in circuit speed, and 3% of area overhead in these two regimes, respectively. Therefore, the GLB technique can be generally applied to reduce leakage power consumption for both near- and super-V_T regimes with relatively minor impact on speed and area. Second, we create standard cell libraries by using the fine-grained GLB technique and a Dual-V_T technique and use them to synthesize ISCAS benchmark circuits, in order to compare the GLB with the Dual-V_T technique. Synthesis results demonstrate that i) the GLB technique is able to deliver a fine-grained trade-off curve between leakage power savings and circuit speed degradation; and ii) the GLB technique is much more effective compared with Dual-V_T technique in the near-V_T regime because its tradeoff curve is less sensitive to the supply voltage. Additional benefits of using the GLB technique include a less expensive fabrication cost as it requires no additional manufacturing steps and masks, and an improved immunity against the ling-edge roughness effect. We investigate the leakage power saving capability of the GLB technique versus the granularity of the biased gate length. Experimental results show a diminishing return effect that provides insights of further optimizing the GLB cell library – a small number of cells can be used to achieve the majority of leakage power savings. Finally, we illustrate that the total power consumptions (comprised of both dynamic and leakage power consumptions) of the presented GLB technique can also be significantly reduced.

II. The 7nm FinFET Technology

A. FinFET Device Model

Due to the lack of publicly accessible industrial data for deeply-

scaled FinFETs, we derived our FinFET device models by using Synopsys Sentaurus Device [13] that is included in the TCAD tool suite [12]. For this paper, a 7nm FinFET process with lambda-based layout design rules is developed [15][16][17].

B. Leakage Power Saving Techniques

Gate-Length Biasing: We consider GLB with increased gate lengths up to 9nm. The reason to choose 9nm as the upper bound is that significantly larger gate lengths are not layout swappable with nominal versions and it can result in substantial Engineering Change Order (ECO) overheads during layout [3]. The small gate-length biases for FinFET devices can be achieved by slight modification to the layout.

Dual-V_T Technique: We engineer the work-function of gate materials to increase the V_T of the FinFET devices [17]. The V_T of the standard FinFET devices is 0.235V, and the V_T of the high-V_T version is 0.335V. Note that fabricating the FinFET circuits with the Dual-V_T technique incurs additional costs in gate work-function engineering.

In summary, we generate standard FinFET devices with 0.235V threshold voltage and 7nm gate length using Synopsys TCAD tool suite. We also generate a set of FinFET devices with biased (increased) gate lengths up to 9nm and standard V_T value, as well as high-V_T FinFET devices with 7nm gate length and an increased V_T equal to 0.335V. The naming conventions for the generated FinFET devices are concluded in Table I. We can also name the logic cells made up with such FinFET devices, e.g., the cell name for a 1X inverter using standard FinFET devices is INV1X_STD.

C. FinFET Standard Cell Library

In this paper, the deeply-scaled FinFET standard cell libraries in this paper are built in .lib format [18]. The 7nm FinFET device models aforementioned are specified by look-up-tables (LUTs) which can be simulated in HSPICE through a Verilog-A interface. A hierarchical manner is adopted to build the standard cell libraries: (i) in the library-level, the information of process, supply voltage level, units, LUTs of the FinFET device model, thresholds for timing parameters as well as operating corners are provided; (ii) in the cell-level, the cell name, area, leakage power, I/O, and various capacitances are specified and measured; (iii) in the pin-level, the timing parameters including rise/fall output slews, as well as rise/fall propagation delays, and internal rise/fall power parameters are stored in a certain number of 2-D LUTs. The timing and power parameters of each logic cell in the 7nm FinFET standard library are obtained through HSPICE simulations based on the Verilog-A based 7nm FinFET device model.

To evaluate the performance of the presented GLB technique, we designed a few standard cell libraries as listed in Table II. The GLB libraries (NT_GLB and ST_GLB), in which each type of logic cells have five versions: one with nominal gate length and four with different biased gate lengths, are used to test the effectiveness of (fine-grained) GLB in leakage power minimization. Dual-V_T libraries (NT_DVT and ST_DVT), which consist of standard cells with two different threshold voltages – nominal V_T and high V_T, are used to test the effectiveness of Dual-V_T technique on circuit benchmarks. Standard libraries[1] (NT_STD and ST_STD) are reference libraries where no leakage power saving technique is applied. Note that the STD libraries and GLB-based libraries are comprised of logic cells with nominal V_T, and all cell libraries have two versions as we characterize them in near-V_T and super-V_T voltage regimes separately. We also reduce the number of gate length bias values to form GLBra, GLBrb and GLBrc libraries, which has four, three and two gate lengths, respectively, to explore the opportunities of optimizing the GLB library and reducing the library complexity.

III. Impacts of the Gate-Length Biasing Technique

A. Impact on Leakage Power and Circuit Speed

[1] Please note that here standard library STD means cell library based on standard FinFET devices with nominal 7nm gate length and V_T = 0.235V.

TABLE I. 7NM FINFET DEVICES NAMING CONVENTIONS

Device Name	V_T	Gate-Length
STD	0.235V	7.0nm
HVT	0.335V	7.0nm
GL05	0.235V	7.5nm
GL10	0.235V	8.0nm
GL15	0.235V	8.5nm
GL20	0.235V	9.0nm

TABLE II. NAMING CONVENTIONS FOR LIBRARIES IN DIFFERENT REGIMES

Library Name	Operation Regimes	Device Types
NT_STD	Near-V_T ($V_{dd} = 0.30V$)	STD
NT_DVT		STD, HVT
NT_GLB		STD, GL05, GL10, GL15, GL20
NT_GLBra		STD, GL05, GL15, GL20
NT_GLBrb		STD, GL10, GL20
NT_GLBrc		STD, GL20
ST_STD	Super-V_T ($V_{dd} = 0.45V$)	STD
ST_DVT		STD, HVT
ST_GLB		STD, GL05, GL10, GL15, GL20
ST_GLBra		STD, GL05, GL15, GL20
ST_GLBrb		STD, GL10, GL20
ST_GLBrc		STD, GL20

In this subsection, we investigate the advantages and limitations of GLB technique for FinFET logic circuits operating in near- and super-V_T regimes. As shown in Figure 1, a 20-stage FO4 FinFET inverter chain made up with 2nm gate-length biased NFET and PFET (i.e., 9nm gate length) achieves up to 69% and 68% leakage power reductions in near- and super-V_T regimes, respectively, compared to the leakage power results at the nominal 7nm gate length. The reduction of leakage power comes at the cost of degradation of circuit speed. One can observe in Figure 1 that the propagation delay, which is measured at 50%-50%, increases by 27% and 13% in the near- and super-V_T regimes, respectively. Therefore, observations in Figure 1 strongly justify our methodology that leverages FinFET devices with slightly biased L_G to achieve significant amount of leakage power reduction at the cost of relatively minor performance degradation.

Compared to previous work utilizing the GLB technique [3][10], the GLB technique is more effective for deeply-scaled FinFET circuits in the sense that more leakage power savings are achieved at the same amount degradation of circuit speed. For instance, measurement results for a single NMOS transistor at 130nm shows an 18% leakage power reduction at the cost of 15% delay degradation after biasing its gate length to 150nm. The reason that more leakage power is saved is that the deeply-scaled FinFET technology is heavily affected by the SCEs, including the V_T roll-off effect and DIBL effect. Both the V_T roll-off effect and the DIBL effect will result in an increase of V_T when the gate length increases (in which the DIBL effect specifies that V_T is a linear function of V_{DS} [19], and the linear coefficient depends on the gate length [20]).

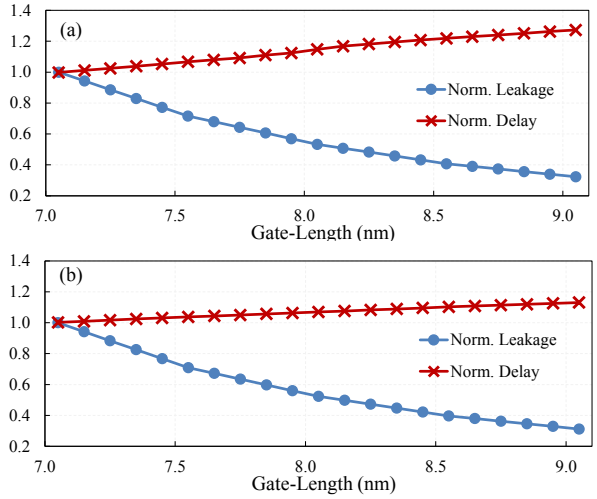

Figure 1. (a) Evaluating normalized leakage and delay of a 20-stage FO4 inverter chain in near-V_T regime and (b) super-V_T regime with different gate lengths.

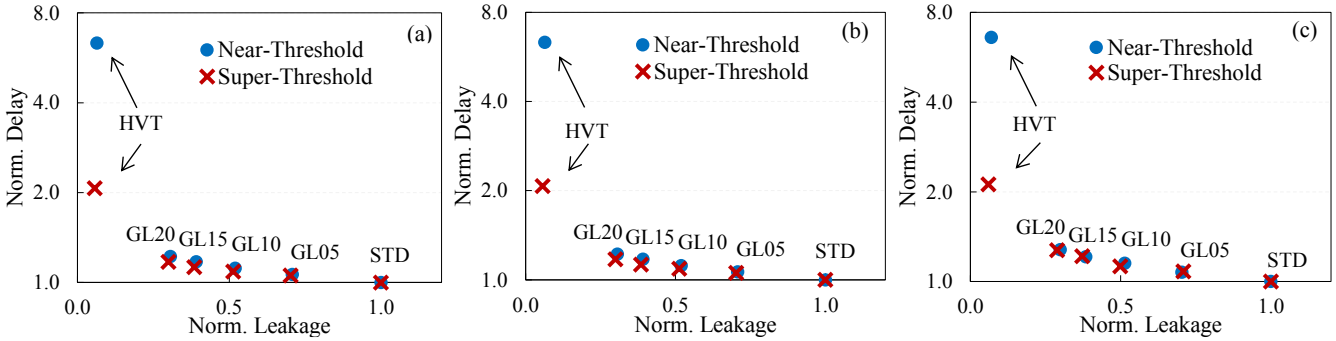

Figure 2. Comparisons of normalized delay and leakage of cells with different gate lengths and V_T at near- and super-V_T regimes. Cells from left to right are inverter (a), NAND2 (b), and NOR2 (c).

Therefore, the GLB technique that biases the gate length alleviates the impact of the V_T roll-off and DIBL effects and in return results in a higher V_T. The higher V_T is the major factor responsible for the significant leakage power reduction in the deeply-scaled FinFET technology. In contrast, SCEs are negligible for 130nm technology node.

Another important observation is that under the same GLB, the normalized leakage reduction is very close in near- and super-V_T regions, while the normalized delay penalty in near-V_T regime is as twice as super-V_T regime (i.e., 27% and 13% normalized delay increase at $L_G = 9nm$ in the near- and super-V_T regimes, respectively). There are two factors that the biased gate length affects the circuit speed: i) longer gate length reduces the driving strength; and ii) the V_T roll-off and DIBL effects result in slightly higher V_T. The former factor equivalently impacts circuits operating in the near- and super-V_T regimes. However, the latter one degrades the circuit speed in a polynomial manner (according to the α-power law) in the super-V_T regime and more significantly in the near-V_T regime. Therefore, longer normalized delays are observed in Figure 1 (a), compared to Figure 1 (b).

B. *Area Overhead*

The GLB technique also leads to an area overhead. The investigation of layouts of cells shows that the area overheads for GLB cells are approximately 1~4%, depending on the sizing and the degree of gate-length bias. We synthesize ISCAS benchmark circuits using i) a library that only applies the nominal gate length (NT_STD); and ii) a library that contains logic cells with 7nm, 7.5nm, 8nm, 8.5nm and 9nm gate lengths (NT_GLB). Then we compare netlists generated using these libraries and estimate the total circuits areas. As an example, the area overhead of c3540 is approximately 3.31%, which is totally acceptable, given a significant leakage power saving of 43% achieved by the GLB technique.

IV. Comparisons Between the Gate-Length Biasing and the Dual-V_T Tehcnqiue

A. *Basic Cells Analysis*

We compare the cell speed and leakage power of different runtime leakage power saving techniques, namely, the GLB technique and Dual-V_T technique. Figure 2 (a), (b), and (c) compare normalized delay and leakage power results for some basic cells such as 1X inverter, 1X 2-input NAND gate, and 1X 2-input NOR gate, respectively, at near- and super-V_T voltage regimes. Results in Figure 2 show that, although using a high V_T can reduce the leakage power significantly, it results in a huge delay penalty. In addition, due to the limitation of fabrication technology, it is not practical to continuously modify the gate work-functions and generate fine-grained threshold voltages. In contrast, the GLB technique provides a solution to produce fine-grained trade-offs between the leakage power reduction and the circuit speed degradation.

Another important observation from Figure 2 is that the Dual-V_T technique and the GLB technique result in distinct impacts on circuit speed in different voltage regimes. When operating in the super-V_T regime, the Dual-V_T technique achieves more than 90% leakage power reduction with 2X delay penalty. However, the delay penalty increases to 6~8X when the supply voltage is reduced to the near-V_T regime. Compared to the Dual-V_T technique, the GLB technique is more robust to the supply voltage in the sense that the trade-off points are less dependent on the supply voltage. This is because of the following two reasons: (i) The GLB technique mitigates the DIBL effect which reduces the V_T value at $V_{dd} = 0.45V$ compared with $V_{dd} = 0.30V$, and (ii) The V_T value of HVT device is 0.335V and is higher than the supply voltage $V_{dd} = 0.30V$ in the near-V_T regime, which makes gate delay exponentially dependent on the supply voltage.

The robustness property makes the GLB technique to be more effective in the low supply voltage regime. For example, considering a non-critical path whose delay is half of the critical path delay, when operating in the super-V_T regime, most cells along this path can be replaced by high-V_T cells to reduce the leakage power consumption. However, if the supply voltage drops into the near-V_T regime, this non-critical path becomes the actual critical-path and may cause a timing violation because delays of all high-V_T cells are increased by 6~8X. Therefore, the Dual-V_T technique becomes not practical for circuits operating in the near-V_T regime or multiple voltage regimes. In contrast, the GLB is still effective because the relative delay penalties of GLB cells are more robust to the change of the supply voltage. The non-critical paths in the super-V_T regime are more likely to remain non-critical when operating in the near-V_T regime.

B. *ISCAS 85 Benchmark Results*

We synthesize ISCAS 85 benchmark circuits based on the generated standard cell libraries by using the Synopsys Design Compiler. The leakage power results are reported by the Design Compiler. We first compare results of leakage power reductions

Table III. Leakage Power Consumption Comparison among STD, DVT and GLB in Near-V_T Regime without Delay Penalty

Circuits	NT_STD	NT_DVT		NT_GLB	
	Leakage (nW)	Leakage (nW)	Leakage Reduction	Leakage (nW)	Leakage Reduction
c432	133.4	131.2	1.7%	49.1	63.2%
c1908	350.9	298.7	14.9%	200.7	42.8%
c2670	487.3	456.2	6.4%	208.1	57.3%
c3540	865.3	836.5	3.3%	612.2	29.3%
c6288	2107.0	1895.7	11.1%	1394.4	33.8%
average	788.78	723.7	7.5%	492.9	45.3%

Table IV. Leakage Power Consumption Comparison among STD, DVT and GLB in Super-V_T Regime without Delay Penalty

Circuits	ST_STD	ST_DVT		ST_GLB	
	Leakage (nW)	Leakage (nW)	Leakage Reduction	Leakage (nW)	Leakage Reduction
c432	248.5	50.4	79.7%	85.9	65.4%
c1908	579.6	248.4	57.1%	308.5	46.8%
c2670	851.0	118.6	86.1%	288.9	66.1%
c3540	1454.7	632.0	56.6%	828.5	43.0%
c6288	3216.0	503.0	84.4%	1081.0	66.4%
average	1210.0	310.5	72.8%	518.6	57.5%

achieved by the presented GLB technique and the Dual-V_T technique in different voltage regimes. Table III lists leakage power consumptions after synthesizing various benchmark circuits with NT_STD, NT_DVT, and NT_GLB libraries with the same delay constraint. One can observe that the presented GLB technique is able to reduce the leakage power consumption by up to 63.2% without any delay penalty, compared to the results when no leakage power saving technique is applied. An average leakage power reduction of 45.3% is achieved for all benchmark circuits tested. In contrast, results in Table III show that the Dual-V_T technique only achieves 7.5% leakage power reduction on average. The presented GLB technique significantly improves the leakage power saving capability by 6X on average in the near-V_T regime, against the Dual-V_T technique. This is because of the GLB's robustness as analyzed in Section IV.A.

Table IV compares leakage power consumptions and leakage power reductions of these two techniques in the super-V_T regime. One can observe that Dual-V_T technique (slightly) outperforms the presented technique in this condition. This is because that the relative delay penalty of the Dual-V_T technique is much smaller in the super-V_T regime and a large number of cells in non-critical paths can be replaced by high-V_T cells. The results in Table IV agree with our observations in Figure 2 and analysis in Section IV.A. However, the leakage power saving capability of the presented GLB technique is still comparable to that of the Dual-V_T technique in the super-V_T regime.

V. Optimizing the GLB Cell Library

We test GLB, GLBra, GLBrb, GLBrc, which are comprised of four, three, two, one gate-length biased cells and the nominal cell, respectively, under the same delay constraint in the near-V_T regime. Figure 3 shows leakage power consumptions normalized to results of NT_STD cell library of a few ISCAS 85 benchmarks. One can observe that the library that has more gate-length biases is able to achieve better leakage power performance since it delivers a finer-grained trade-off between (cell) leakage and delay. Another important observation is that the library with 2 gate-lengths significantly improves the leakage performance, compared to STD, but adding more gate-length biases can only marginally reduce the leakage consumption, which shows a diminishing return effect. Therefore, if the cell library is being designed with limited resources and efforts, two gate lengths are good enough to achieve a satisfactory leakage performance. This diminishing return effect provides us insights of how to design the GLB cell library with an acceptable size, while the majority of the power saving capability is claimed.

VI. Total Power Consumptions

We also investigate the impact of presented fine-grained GLB technique on the total (averaged over time) power consumption of benchmark circuits in both regimes and show results in Figure 4. The total (averaged) power consumption is comprised of both dynamic power and leakage power consumptions. One can see that FinFET circuits synthesized using GLB libraries achieve total power savings over all different delay constraints in both regimes. In particular, we observe a small amount of total power savings when the delay constraint is tight because the leakage power consumption plays a

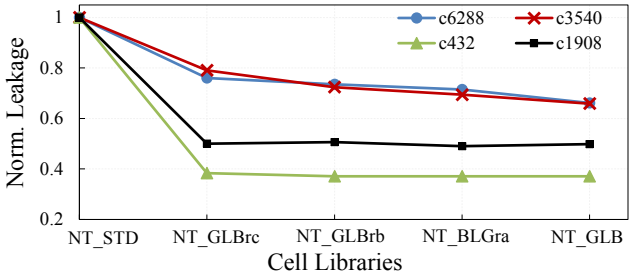

Figure 3. Normalized leakage consumptions of ISCAS benchmark circuits synthesized using different gate-length biased libraries in the near-V_T regime.

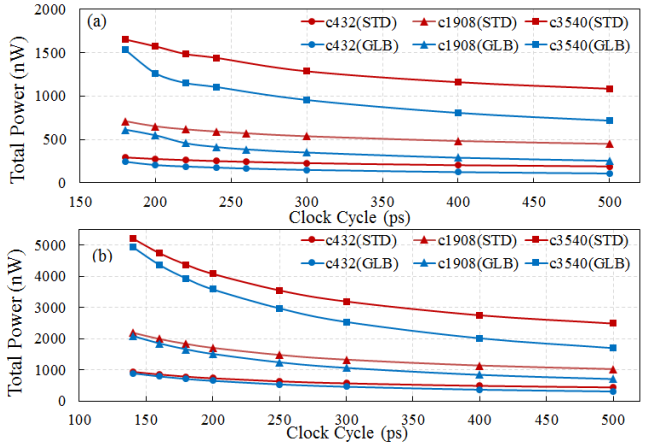

Figure 4. Total power consumptions of some ISCAS benchmark circuits synthesized using STD and GLB library in the (a) near-V_T and (b) super-V_T regime.

less important role compared with dynamic power consumption in this case. However, for applications with relaxed delay constraints, significant total power reductions of up to 52% in the near-V_T regime and up to 31% in the super-V_T regime are observed. Therefore, although the presented fine-grained GLB technique consumes slight additional dynamic energy consumption, it still results in significant savings in total power consumptions without any timing performance penalty. This is mainly because the GLB technique is very effective in reducing the leakage power consumption, which has become very important in deep-scaled technology node, in multiple voltage regimes.

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