50-nm Gate Schottky Source/Drain p-MOSFETs With a SiGe Channel

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***Abstract*—We propose new SiGe channel p-MOSFETs with germano–silicide Schottky source/drains (S/Ds). The Schottky barrier-height (SBH) for SiGe is expected to be low enough to improve the injection of carriers into the SiGe channel and, as a result, current drivability is also expected to improve.**

In this letter, we demonstrate the proposed Schottky S/D p-MOSFETs down to a 50-nm gate-length. The drain current and transconductance are −339 μA/μm and 285 μS/μm at $V_{GS} = V_{DS} = -1.5$ V, respectively. By increasing the Ge content in the SiGe channel from 30% to 35%, the drive current and transconductance can be improved up to 23% and 18%, respectively. This is partly due to the lower barrier-height for strained $Si_{0.65}Ge_{0.35}$ channel than those for strained $Si_{0.7}Ge_{0.3}$ channel device and partly due to the lower effective mass of the holes.

***Index Terms*—Germano–silicide, heterostructure, MOSFET, Schottky source/drain, SiGe, silicide, silicon–germanium-on-insulator (SGOI).**

I. Introduction

SCHOTTKY SOURCE/DRAIN MOSFETs (SSD-MOSFETs) are an attractive choice for scaling down into the sub-100-nm gate regime, because it can be with implantless and low-temperature process. Furthermore, the SSD-MOSFETs are one of the most promising ballistic-MOSFETs because high-energy carrier injection into the channel from the metal-source is possible [1]–[10]. However, this type of MOSFET cannot achieve the high-drive current because the current is limited by relatively high-potential barrier (Schottky barrier) at the source. To improve the current drivability of SSD-MOSFETs, we propose a new SiGe-channel p-MOSFET that consists of a silicide and a germano–silicide Schottky junction S/D. The Schottky barrier-height (SBH) at the PtGeSi/SiGe channel interface can be controlled by the Ge content in the SiGe channel because SBH is lowered and almost completely determined by the SiGe band gap [11]. Thus, the current drivability improvement could be expected by this barrier lowering at the PtGeSi/SiGe interface.

Strained SiGe channel p-MOSFETs have also received a great deal of attention, due to their high-drive current, which is increased by the strain- or band-structure-induced mobility improvements [12]–[14] to minimize the asymmetric operation of MOSFETs in CMOS applications. However, conventional SiGe-channel p-MOSFETs require carefully considered channel design and doping profiles to prevent the parallel conductions at the SiO_2/Si parasitic channel.

On the other hand, in the SiGe channel SSD-MOSFETs, the hole-injection into the Si channel might be effectively suppressed by a higher Schottky barrier at the PtSi/Si interface than that at the PtGeSi/SiGe interface and most of the holes being injected into the SiGe channel. Then, parallel conductions at the SiO_2/Si parasitic channel would be strongly suppressed by selective carrier injection, which had been confirmed by two-dimensional (2-D) drift-diffusion device simulations [15]. Thus, the current drivability could be also improved expected by the lower effective mass of the holes in the SiGe channel.

In this letter, we demonstrate first ever SiGe channel SSD-MOSFETs with gate lengths down to 50 nm, accomplishing high current drivability.

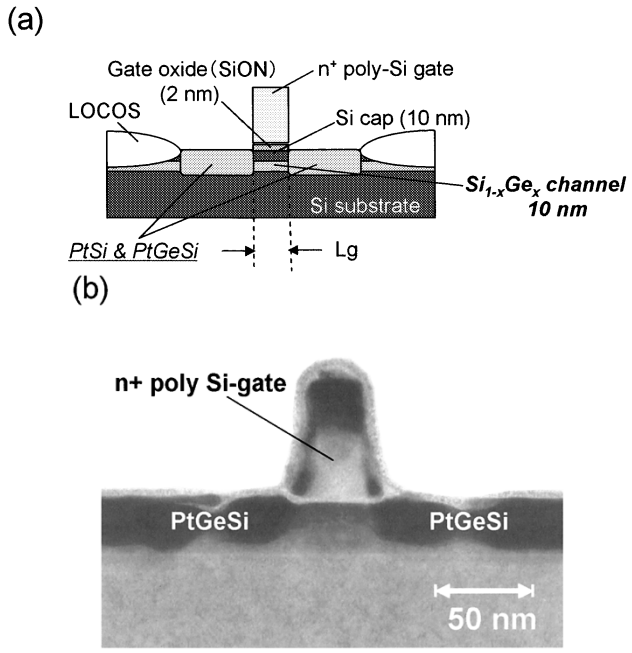

Fig. 1. (a) Schematic view of the proposed SiGe channel SSD-MOSFET. (b) TEM micrograph of a fabricated 50-nm device. The S/D junction-depth is about 25 nm and the epitaxial SiGe and Si layers in the S/D region were completely silicided.

II. Device Fabrication

Fig. 1(a) is a schematic view of the structure of the proposed device. A strained 10-nm thick SiGe channel (p-type: $< 3 \times 10^{12}$ cm^{-3}) and a relaxed 10-nm thick Si cap (p-type: $< 3 \times$

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10^{12} cm^{-3}) were grown by UHV-CVD on an n-type ($\sim 1.6 \times 10^{16}$ cm^{-3}) and 5 Ωcm substrate. Wafers with two different Ge contents ($x = 0.30$ and 0.35) in the SiGe channel were prepared for comparison purposes.

After conventional LOCOS-isolation processes, a 2-nm thick nitrided gate oxide was grown by rapid thermal oxidation and nitridation of the Si-capping layer. Then, a 150-nm thick, *in-situ*-doped n-type polysilicon gate was grown by LPCVD. We used electron-beam lithography to form the gate pattern. After forming the gate, a 10-nm sidewall-spacer was formed. Prior to S/D-metal evaporation, cleaning was done with a diluted-HF solution. 10-nm Pt evaporated by electron-beam evaporator and then silicided at 400 °C in an N_2 ambient. Nonreacted Pt was removed in a diluted aqua-regia solution. Fig. 1(b) is a TEM micrograph of the 50-nm gate device that we fabricated. The source and drain junction-depth were about 25 nm and the epitaxial SiGe and Si layers in the S/D region were completely silicided. The process temperature was suppressed under 800 °C and strain of epitaxial SiGe channel was maintained.

III. Results and Discussion

Fig. 2 compares the drain current curves of 70-nm gate-length devices with different Ge content ($x = 0.30$ and 0.35). A 23% improvement in the current drive can be observed at $V_{\rm DS} = V_{\rm GS} = -1.5$ V in the $Si_{0.65}Ge_{0.35}$ channel SSD-MOSFET, compared to the device with the $Si_{0.7}Ge_{0.3}$ channel. An 18% improvement in the saturation transconductance can also be observed at $V_{\rm DS} = V_{\rm GS} = -1.5$ V.

This is partly due to the lower barrier-height for the strained $Si_{0.65}Ge_{0.35}$ channel than that for the strained $Si_{0.7}Ge_{0.3}$ channel device and partly due to the lower effective mass of holes in the $Si_{0.65}Ge_{0.35}$ with a greater biaxial compressive strain. The biaxial compressive strain in the SiGe channel lifts the degeneracy of the light-hole (LH) and heavy-hole (HH) bands at the Γ points, leading to an even lower in-plane effective mass for the topmost HH band [14].

Fig. 3 shows the drain current curves of a 50-nm gate-length device with a $Si_{0.7}Ge_{0.3}$ channel. High-drive current (~ -339 μA/μm) and high transconductance (~ 285 μS/μm) were achieved at $V_{\rm DS} = V_{\rm GS} = -1.5$ V. The drive current is about 60% compared with scaled pn-junction p-MOSFETs [16]. To improve the drive current, the Si cap layer must be thinned to increase the gate capacitance.

The sublinear behavior at drain voltages of less than ~ 0.2 V that has recently been reported for SSD-MOSFETs [8] caused by the forward-biased Schottky barrier at the drain end of the channel were vanished and almost linear behavior was achieved. This behavior was probably caused by the relatively low barrier-height at the drain end "forward-biased" PtSiGe/SiGe Schottky junction.

Fig. 4 has the subthreshold curves for SiGe channel SSD-MOSFETs. The linear threshold voltage was 0.28 V for 50-nm gate device and threshold voltage shift ΔVth was about 0.3 V. The large off-state leakage observed at $V_{\rm DS} = -1$ V is due to thermionic and tunneling emissions over the 1ow ($\sim <$ 0.2 eV) source potential barrier which occurs along the entire edge of the

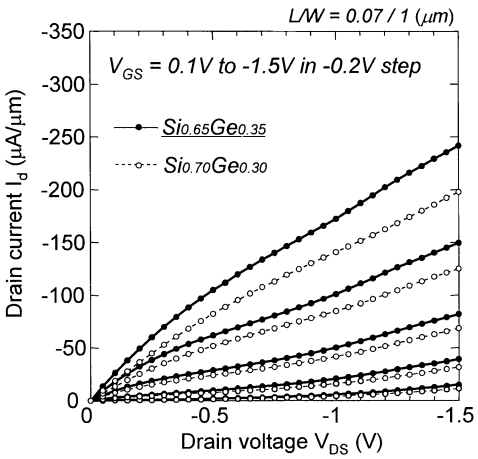

Fig. 2. Drain current curves of 70-nm gate-length devices with different Ge content. The solid and broken curves are for $Si_{0.65}Ge_{0.35}$ and $Si_{0.7}Ge_{0.3}$ channels, respectively. A 23% improvement in the current drive can be observed at $V_{\rm DS} = V_{\rm GS} = -1.5$ V in the $Si_{0.65}Ge_{0.35}$ channel SSD-MOSFET compared with the $Si_{0.7}Ge_{0.3}$ channel device. An 18% improvement in saturation transconductance can also be observed at $V_{\rm DS} = V_{\rm GS} = -1.5$ V.

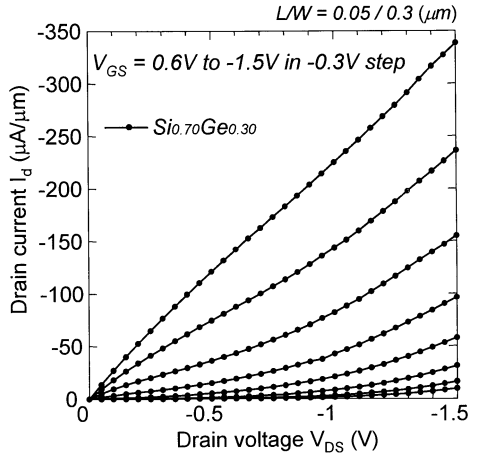

Fig. 3. Drain current curves for a 50-nm gate-length device with a $Si_{0.7}Ge_{0.3}$ channel. The high-drive current (~ -339 μA/μm) and high transconductance (~ 285 μS/μm) were achieved at $V_{\rm DS} = V_{\rm GS} = -1.5$ V.

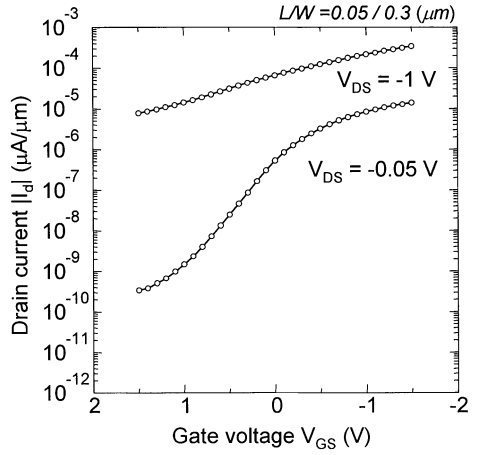

Fig. 4. Subthreshold curves of a 50-nm gate-length device with a $Si_{0.7}Ge_{0.3}$ channel. Off-state leakage under bias conditions is caused by the thermionic and tunneling emissions that occurred along the entire edge of the source.

source. This phenomenon has recently been reported for SSD-MOSFETs with bulk-Si substrates [10]. However, these leakage currents, especially the thermionic emission along the entire edge of the source, can potentially be suppressed by using ultrathin silicon–germanium-on-insulator (SGOI) substrates [17] and complete silicidation down to the buried oxide layer in the S/D region.

IV. Conclusions

We demonstrated first ever SiGe channel SSD-MOSFETs with gate-lengths down to 50 nm. The drain current and transconductance were $-339\ \mu\mathrm{A}/\mu\mathrm{m}$ and $285\ \mu\mathrm{S}/\mu\mathrm{m}$, respectively, at $V_{\mathrm{DS}} = V_{\mathrm{GS}} = -1.5$ V for a 50-nm long channel device. The large leakage current could be reduced and the subthreshold characteristics improved by using a thin-body SGOI structure and complete silicidation of the S/D region.

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