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FABRICATION OF NANO-ELECTROMECHANICAL STRUCTURES DOWN TO 20 NM BY SPACER TECHNOLOGY

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ABSTRACT

Spacer technology has been developed to fabricate nanostructures for NEMS application. It provides a parallel nanofabrication method with double or quadplex device density at a certain lithography node. By controlling the deposited film thickness, the feature size of the SiO₂ spacer hard mask is reduced down to 35 nm. After the spacer pattern is transferred to Si, a precise thermal oxidation is performed to improve the profile and reduce the plasma damage. Finally, sublimation or HF vapor phase etching is introduced to release the nanostructures according to different structure dimensions. As a result, with better surface morphology, suspended Si nanobeams with a width of 20 nm are obtained. Actuated by mechanical vibration and electrostatic forces, vibrations of the obtained cantilever beams and fixed-fixed beams are observed in SEM. In addition, a metallic nano-nozzle with a diameter of 140 nm is established by electroless plating around the suspended Si nano-beam served as a mold.

As a development of the spacer technology, nano-needle array is demonstrated at the cross points of crossed SiO_2 spacers by anisotropic etching. The diameters of the hybridized nano-needles are 300 nm so far and can be further reduced by smaller spacer dimension.

Keywords: NEMS, spacer technology, suspended nano-beam, nano-nozzle, nano-needle array

1. INTRODUCTION

Nano-electromechanical systems (NEMS), characterized by dimensions in nanometers, will surely take a revolution in mass detection, medical diagnostics, data storages and mechanical miniaturization [1-4]. It also provides a new platform to take further research in fundamental physics [5-7]. NEMS devices can be fabricated by either top-down or bottomup method. Conventional top-down method is based on different kinds of "lithography" technologies such as extreme ultraviolet and electron beam lithography. They are always involved with either expensive complex commercial apparatus or low fabrication efficiency. Bottom-up method, usually in a chemical synthesis way [8], however, still has great challenges on controllable construction. Both of the two methods are promoting the development of NEMS nowadays.

Spacer technology has been demonstrated in integrated circuit industry for decades. Defined by the deposited film thickness, the minimum feature size of the spacer has been demonstrated to be 20 nm, or even further smaller [9]. In addition, it also provides a double or quadplex device density for a given lithography node [10]. Based on this spacer technology, Choi et al. has obtained Si nanowire array [9] and applied it to produce novel electronic devices with sub-40 nm gate length recently [10, 11].

In this paper a parallel fabrication method for NEMS manufacture is proposed by using spacer technology. SiO_2 spacer hard mask of 35 nm is fabricated and Si structure of 20

nm is obtained combined with a precise thermal oxidization. Sublimation release or HF vapor phase etching is introduced to guarantee high yield of suspended nano-structures. Vibrations of the obtained cantilever beams and fixed-fixed beams are then observed in scanning electron microscope (SEM), under external actuations. By developing the spacer technology, some other nano-electromechanical structures such as nano-nozzle and nano-needle array are also demonstrated.

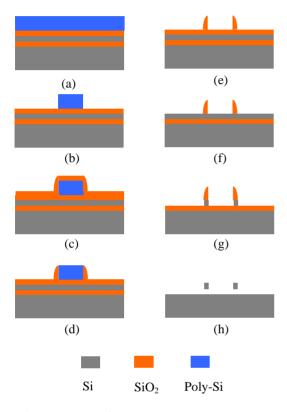


Fig. 1. Schematics of Si nano-structure fabrication process based on spacer technology

2. SPACER TECHNOLOGY FOR SUSPENDED NANO-BEAM

2-1. Spacer Technology

Fig. 1 shows the fabrication process of Si nano-structures by spacer technology. After the film deposition (Fig. 1(a)), poly-Si is patterned by photolithography (Fig. 1(b)). Then a LPCVD SiO₂ is conformally deposited at the wafer surface (Fig. 1(c)) and anisotropically etched by RIE (Fig. 1(d)). We remove the exposed poly-Si (Fig. 1(e)) and etch the SiO₂, leaving the spacers only (Fig. 1(f)). Then the spacer hard mask pattern is transferred to Si combined with traditional photoresist masks by anisotropic ICP etching (Fig. 1(g)). Finally release the structures by etching SiO₂ (Fig. 1(h)).

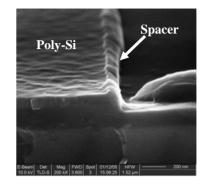
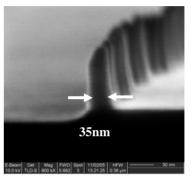
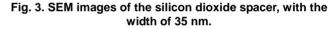


Fig. 2. SEM image of spacer corresponding to Fig. 1 (d)





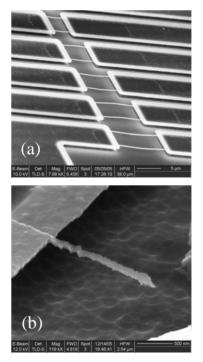


Fig. 4. Different nano-structures after release. (a) released by sublimation method; (b) released by HF vapor phase etching method.

As illustrated above, the feature size of the spacer hard mask is defined by the deposited film thickness in Fig. 1 (c). It can be precisely controlled at nanometer scale by traditional microelectronics process. So it is convenient to obtain nanostructures at the whole wafer. Meanwhile, for a given lithography node, it can provide a double or even quadplex device density, with feature size beyond the lithography limit simultaneously.

Fig. 2 shows the SEM image of the SiO_2 spacer before remove the poly-Si, corresponding to the Fig. 1 (d). By controlling the deposited film thickness, a spacer with dimension of 35 nm is obtained in Fig. 3, which is corresponding to Fig. 1 (f). Combined with these hard masks and photo-resist masks, Si structures can be patterned and etched then (see Fig. 4).

Usually there are some variations in the lateral surfaces of Si nano-structures fabricated by spacer technology. From Fig. 4 (b) we can see variations about 50 nm for the Si nano-beam. These variations will significantly limit the applications and the extent to reduce the structure width. Thus a precise thermal oxidization is performed before final release. This will not only improve the surface profile, but also reduce the dimension and plasma damage. As a result, with better surface morphology, the feature size is finally reduced down to 20 nm (see Fig. 5).

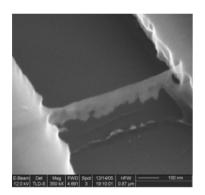


Fig. 5. 20 nm Si nano-beam after precise thermal oxidation and HF vapor phase release.

2-2. Sacrificial Layer Release

Two sacrificial release methods for different structure dimensions are introduced to obtain suspended nano-structures in the last step. For structures with width above 40 nm, we use HF solution to wetly etch the surrounding SiO_2 . Then cyclohexane is used to replace the HF solution for sublimation release. For structures with width below 40 nm, HF vapor phase etching is proposed to prevent the fluid-induced fracture as well as surface-tension-induced collapse during the final release step.

The results of the two methods mentioned above are shown in Fig. 4 (corresponding to Fig. 1(h)). The sublimation method is well established by different kinds of structures up to 16 μ m-long and above 40 nm-wide. By using the dry release

method, 20 nm-wide Si suspended beam is released successfully (see Fig. 5). As a proof, vibrations of the cantilever beams and fixed-fixed beams are observed in SEM, actuated by mechanical vibration and electrostatic forces, respectively (see Fig. 6). The two release methods applied according to the structure dimensions guarantee high yield of suspended nano-structures in the release step.

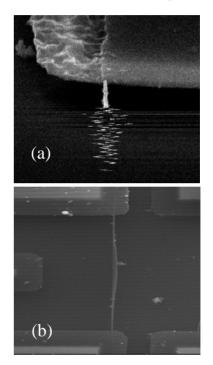


Fig. 6. Vibrations of (a) cantilever beams and (b) fixed-fixed beams are observed in SEM under external actuations.

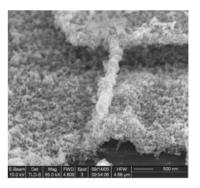


Fig. 7. Metal nano-nozzle fabricated by spacer technology and electroless copper plating.

2-3. Other Nano-electromechanical Structures

Based on the spacer technology, some other nanoelectromechanical structures can also be parallel fabricated. Used as a mold, the Si nano-beams can be conformally encapsulated by other materials and then selectively etched to form nano-nozzle and nano-channel structures. Here we use electroless copper plating to encapsulate the Si after the structures are suspended. Copper will only be plated on Si nano-beams while the SiO_2 is immune [12]. Then we use FIB to cut the fixed-fixed beam to expose the Si and selective remove the Si core by KOH etching. Finally a nano-nozzle with a diameter of 140 nm is successfully obtained (see Fig. 7).

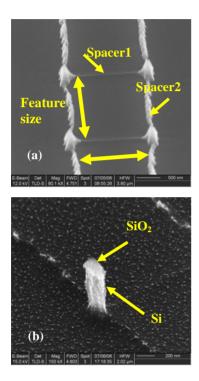


Fig. 8. (a) SiO_2 nano-needle array by crossed spacers, with quadplex density for the given lithography node. (b) Hybridized nano-needle with a diameter of 300 nm.

3. DEVELOPMENT OF THE SPACER TECHNOLOGY

By developing the spacer technology, two layers of SiO_2 spacers are used to fabricate nano-needle array. At the cross points, the thickness of the spacer is doubled. After anisotropic dry etching, only SiO_2 nano-needles are left at the cross points, with the height of a single spacer. The SEM image of SiO_2 nano-needle array is shown in Fig. 8 (a), with quadplex density compared with lithography density. In Fig. 8 (a), the second spacer hasn't finished etching while the first spacer has been completely removed. The needles are generally with a tip radius of 37 nm. This top-down method also enables good controllability of the needle dimensions and locations beyond the photolithography limit.

Then we take the SiO_2 needle as a mask to etch the Si below by ICP. Hybridized nano-needles with higher aspect ratio are then obtained, with a diameter of 300 nm, as shown in Fig. 8 (b). As SiO_2 is hydrophilic and Si is hydrophobic, this nano-needle array is sure to have great prospect in bio-medical field.

4. CONCLUSIONS

The application of spacer technology for NEMS structure fabrication has been successfully demonstrated. Combined with traditional microelectronics process, the feature size of the spacer is reduced to 35 nm, which is far beyond the limitation of the lithography we used. The two release methods we proposed greatly improve the yield of suspended nano-beams. By using a precise thermal oxidization, Si nano-structures with good profile and smaller dimension are fabricated. As a result, we obtain suspended nano-beam as small as 20 nm successfully. We also observe the vibrations of the cantilever beam and fixed-fixed beam under SEM, which can be used in some device applications.

Other nano-electromechanical structures are also demonstrated based on the spacer technology. Both a nano-nozzle of 140 nm diameter and nano-needle of 37 nm tip radius are established, which have potential applications in fluidic and bio-medical field.

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REFERENCES

[1] Dohn, S., Sandberg R., Svendsen W., and Boisen A., 2005, "Enhanced Functionality of Cantilever Based Mass Sensor using Higher Modes and Functionalized Particles", Proc. Transducers'05, Seoul, Korea, pp. 636-639.

[2] Shekhawat G., Tark S., and Dravid V. P., 2006, "MOSFET-Embedded Microcantilevers for Measuring Deflection in Biomolecular Sensors", science, 311, pp. 1592-1595.

[3] Drechsler U., Burer N., Despont M., Durig U., Gotsmann B., Robin F., and Vettiger P., 2003, "Cantilevers with nanoheaters for thermomechanical storage application", Microelectronic Engineering, 67–68, pp. 397–404.

[4] Fennimore A. M., Yuzvinsky T. D., Han W. Q., Fuhrer M. S., Cumings J., and Zettl A., 2003, "Rotational actuators based on carbon nanotubes", nature, 424, pp. 408-410.

[5] Bolle C. A., Aksyuk V., Pardo F., Gammel P. L., Zeldov E., Bucher E., Boie R., Bishop D. J. and Nelson D. R., 1999, "Observation of mesoscopic vortex physics using micromechanical oscillators", nature, 399, pp. 43-46.

[6] Naik A., Buu O., LaHaye M. D., Armour A. D., Clerk A. A., Blencowe M. P., and Schwab K. C., 2006, "Cooling a nanomechanical resonator with quantum back-action", nature, 443, pp. 193-196.

[7] Cleland A. N., and Roukes M. L., 1998, "A nanometre-scale mechanical electrometer", nature, 392, pp. 160-162.

[8] Koehne J., Chen H., Li J., Cassell A.M., Ye Q., Ng H. T., Han J., and Meyyappan M., 2003, "Ultrasensitive label-free DNA analysis using an electronic chip based on carbon nanotube nanoelectrode arrays", Nanotechnology, 14, pp.1239-1245.

[9] Choi Y. K., Zhu J., Grunes J., Bokor J., and Somorjai G. A., 2003, "Fabrication of Sub-10-nm Silicon Nanowire Arrays by Size Reduction Lithography", J. Phys. Chem. B, 107, pp. 3340-3343.

[10] Choi Y. K., King T. J., and Hu C., 2002, "A Spacer Patterning Technology for Nanoscale CMOS", IEEE Trans. Electron. Devices, 49, pp. 436-441.

[11] Choi Y. K., King T. J., Hu C., 2002, "Nanoscale CMOS spacer FinFET for the terabit era", IEEE Electron. Device Lett., 23, pp. 25-27.

[12] Han X., Li Y., Wu W. G., Yan G. Z., and HaoY. L., 2005, "Electroless Copper and Nickel Plating on Single-crystal Silicon for MEMS Applications", Chinese Journal of Semiconductor, 5, (26), pp. 1059-1064