Analogue-to-digital interface technique for digital controllers in DC-DC converters

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A digital controller for a DC-DC converter is implemented with an efficient analogue-to-digital interface scheme. Conventional digital controllers require flash-type ADCs, which need large analogue circuits and thus significantly diminish the advantage of digital implementation. The presented delta-sigma modulated single-bit interface effectively reduces the analogue circuit area, while it achieves good voltage regulations. A silicon chip is implemented and measured to prove the successful operation of the controller.

Introduction: Traditionally, controllers for DC-DC converters have been implemented in pure analogue circuits. However, recent research showed the possibility of digital implementation of controllers [1–3]. Compared to analogue implementations, digital controllers have several advantages such as inherently low sensitivity to process variations, low sensitivity to noise, low-voltage operation, and ease of integration with other digital blocks such as microprocessors. Also, the digital controllers can be designed using a hardware description language (HDL), and can be ported to new processes without long redesign and simulation time of analogue circuits. Even for the digital controllers, however, an essential analogue block is an analogue-to-digital converter (ADC), which interfaces the DC-DC converted analogue output voltage with the digital controller. In this Letter, we demonstrate an efficient interface technique to reduce the complexity of conventional ADCs.

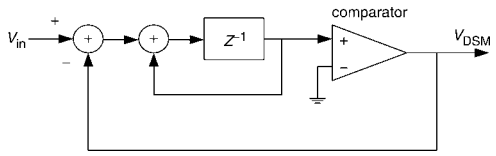

Fig. 1 *First-order delta-sigma modulator*

Delta-sigma modulated DC-DC converter: The design of an ADC could be a major bottleneck in controller development since analogue circuit design heavily depends on circuit designers while digital design is highly automated. The delta-sigma modulator (DSM) [4] has been used widely in high-resolution ADC circuits. Fig. 1 shows the block diagram of a DSM. It is a first-order modulator with an integrator. If multiple integrators are implemented, high-order modulators can be designed at the cost of more power, larger area, and longer design time. The simple first-order modulator is sufficient for our implementation as it is proven in the measurement results later. The hardware complexity of a first-order modulator is significantly less than that of the flash ADCs used in conventional digital controllers. The analysis of a delta-sigma modulator is straightforward [4], and is summarised below:

$$STF(z) = \frac{V_{DSM}}{V_{in}} = z^{-1} \tag{1}$$

$$NTF(z) = \frac{V_{DSM}}{V_e} = 1 - z^{-1} \tag{2}$$

Equation (1) is called a signal transfer function (STF), and it shows that the output of the modulator is the same as the input signal except for a delay. Since the output of the DSM is generated by a comparator, the output has only two levels. In other words, the output of the DSM is a crude representation of input analogue voltage with large quantisation noise V_e. However, the feedback control forces the quantisation noise to be attenuated significantly. The noise transfer function (NTF) in (2) can be evaluated in frequency domain by setting $z = e^{j2\pi f/f_s}$, where f_s is the sampling frequency. This gives [4]

$$NTF(f) \simeq 2\sin\left(\frac{\pi f}{f_s}\right) \tag{3}$$

The quantisation noise will be noise-shaped by $NTF(f)$, so in low frequency band, significant attenuation of quantisation noise can be achieved. The DSM is implemented in place of an ADC block in Fig. 2. The control law of the digital controller in our implementation is an integral controller as in [2], so the details of digital blocks are similar to those in [2].

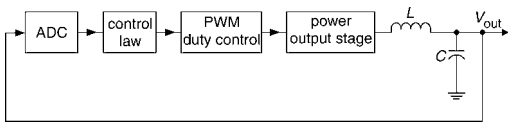

Fig. 2 *Digital DC-DC converter*

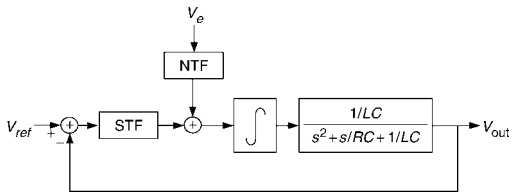

Fig. 3 *Feedback model of DC-DC converter*

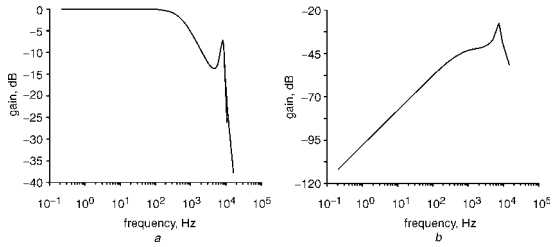

Fig. 4 *Frequency responses of H_1 and H_2*
a H_1 b H_2

Fig. 3 shows a mathematical model of a digitally controlled DC-DC converter. The ADC in Fig. 2 is replaced by STF and NTF blocks, and the digital blocks are replaced by an integrator. The L and C in Fig. 2 are combined with a load resistor R and shown as a second-order RLC block in Fig. 3. The feedback system analysis shows that the transfer function for V_{ref} is:

$$H_1 = \frac{V_{out}}{V_{ref}} = \frac{STF \times K(s) \times RLC(s)}{1 + STF \times K(s) \times RLC(s)} \tag{4}$$

The $K(s)$ is a model of a digital integrator in analogue domain as [2]

$$K(s) = \frac{K}{s} \tag{5}$$

The gain K of the integrator is

$$K = \frac{\Delta d}{T_{cnt}} \tag{6}$$

where Δd is the duty cycle resolution of the PWM generator and T_{cnt} is the period of the digital integrator clock. Similarly, the transfer function for the quantisation noise V_e is:

$$H_2 = \frac{V_{out}}{V_e} = \frac{NTF \times K(s) \times RLC(s)}{1 + STF \times K(s) \times RLC(s)} \tag{7}$$

Since the DC-DC converter in Fig. 2 is a mixture of continuous-time functions and discrete-time functions, we applied bilinear transformation to convert the discrete-time functions into analogue representations. Once the discrete-time functions are converted to continuous-time functions, the complete feedback loop can be analysed. The frequency characteristics of (4) and (7) are shown in Figs. 4*a* and *b*, respectively. They show that the DC-DC output voltage will be equal to the DC reference voltage V_{ref}, and that the quantisation noise V_e of the first-order modulator will be significantly attenuated especially at low frequencies. Because of the quantisation noise attenuation, the one bit interface of the DSM can be used as an accurate analogue-to-digital interface circuit.

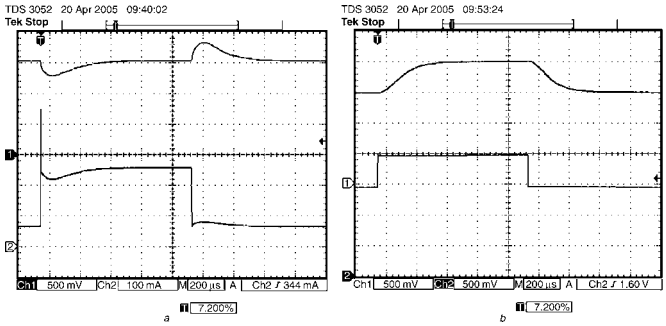

Fig. 5 *Output responses for load current change and V_{ref} change*

a Load current change
b V_{ref} change

Measurement results: To verify the operation of a delta-sigma modulated digital controller, a silicon controller chip was fabricated in 0.35 µm CMOS process and measured at 500 kHz DC-DC switching frequency. The digital logic of the controller was designed and synthesised by Verilog HDL. The analogue DSM block was implemented in a switched-capacitor circuit, which is a common technique in circuit design [4].

Fig. 5*a* shows the DC-DC output voltage regulation when load current, which is the lower trace, changes from 75 to 275 mA and back to 75 mA. The upper trace shows that the output voltage recovers in about 300 µs for the step load current change. Also, Fig. 5*b* shows the output voltage when reference voltage V_{ref} changes from 1.5 to 2.0 V and back to 1.5 V. The output voltage closely follows the reference voltage in 300 µs. These results prove the stable operation of the controller with good voltage regulation.

Conclusion: An efficient analogue-to-digital interface technique has been implemented for digital controllers. Instead of conventional flash-type ADCs, the 1-bit delta-sigma modulator effectively converts the analogue voltage level into digital value for the digital controllers. The silicon implementation shows good voltage regulation performance.

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