

Subband Engineering in n-Type Silicon Nanowires using Strain and Confinement

Z. Stanojević, V. Sverdlov, O. Baumgartner, and H. Kosina

Institute for Microelectronics, TU Wien
Gußhausstraße 27-29/E360, 1040 Wien, Austria

1 Abstract

We present a model based on $\mathbf{k} \cdot \mathbf{p}$ theory which is able to capture the subband structure effects present in ultra-thin strained nanowires. The effective mass and valley minima are calculated for different crystal orientations thicknesses and strains. The results show that transport enhancement can be achieved by both confinement and strain which is in agreement with recent experimental findings.

2 Motivation

Nanowire based gate-all-around transistors offer a perspective for further device size reduction in microelectronics. Apart from the enhancement of electrostatic control over the channel due to a high surface to volume ratio, nanowires exhibit transport properties which deviate significantly from what is observed in bulk silicon or inversion layers. In a recent experimental study [1] nanowires with gate-all-around structure as thin as 3 nm were successfully fabricated using a top down structuring process [2]. The produced nanowires had a [110] oriented axis and (1 $\bar{1}$ 0) and (001) oriented walls.

3 Modeling

To understand the transport properties in wires below 10 nm one must carefully take quantization effects into account. A simple treatment using effective masses fails to satisfactorily describe the subband structure of such thin devices. This is due to the energy of the lowest subband already being of the order of 100 meV where non-parabolicity effects become noticeable.

In this work we investigate the effects of both two-dimensional confinement and strain using a two band $\mathbf{k} \cdot \mathbf{p}$ model for the conduction band [3, 4]. The model is valid for the conduction band and includes a first-order treatment of uniaxial and shear strain. The model Hamiltonian describing a pair of adjacent Δ -valleys reads as follows:

$$\mathbf{H} = \left(\frac{\hbar^2(k_{t1}^2 + k_{t2}^2)}{2m_t} + \frac{\hbar^2 k_t^2}{2m_l} + \Xi_u \varepsilon_{t-1} + V \right) \mathbf{I} \\ + \frac{\hbar^2 k_0 k_1}{m_l} \sigma_z - \left(\frac{\hbar^2 k_{t1} k_{t2}}{M} - 2\Xi_{u'} \varepsilon_{t1-t2} \right) \sigma_x.$$

V denotes the conduction band edge; $m_l = 0.91m_e$ are the longitudinal and $m_t = 0.19m_e$ the transversal effective

mass and $\frac{1}{M} \approx \frac{1}{m_t} - \frac{1}{m_e}$; $k_0 = 0.15 \frac{2\pi}{a}$ amounts to the distance between a X point and the nearest Δ valleys; ε_{t-1} and ε_{t1-t2} are uniaxial and shear strain components and Ξ_u and $\Xi_{u'}$ the deformation potentials; $\sigma_{x,z}$ denote the Pauli matrices and \mathbf{I} the identity matrix. The Hamiltonian is rotated according to the nanowire axis and quantized in the cross section plane to obtain the subband structure.

4 Results and Conclusions

We predict a significant change of the effective mass with respect to its bulk value due to confinement and strain, as shown in Fig. 1 and 2. The trend of the change depends on the crystal orientation of the wire; while for a [111] wire the mass generally increases with confinement and strain, the situation is different for [110] wires. Here, the transport properties can be significantly enhanced using a combination of confinement and strain. We also show that the minima of the heavy unprimed valleys shift to higher energies with increasing strain (Fig. 6) and confinement (Fig. 3), while the opposite trend is observed for the unprimed valley (Fig. 4). This shift leads to a repopulation of the carriers towards the light unprimed valley and further improves the transport properties.

A strain induced current enhancement of up to 30% was shown in [1], which is in qualitative accordance with the results obtained from our calculations, where we found that tensile strain along the axis is beneficial in terms of effective mass for [110] oriented wires. This leads us to believe that transistors based on strained [110] nanowires with diameters below 10 nm are promising candidates for future digital integrated circuits where fast switching and low power consumption are important.

Acknowledgment

This work has been supported by the Austrian Science Fund, special research program F2509.

References

- [1] S. Bangsaruntip *et al.*, *VLSI Technology (VLSIT), 2010 Symposium on* (2010), pp. 21–22.
- [2] S. Bangsaruntip *et al.*, *Electron Devices Meeting (IEDM), 2009 IEEE International* (2009), pp. 1–4.
- [3] J. C. Hensel *et al.*, *Phys. Rev.* **138**, A225 (1965).
- [4] V. Sverdlov *et al.*, *Solid-State Electronics* **52**, 1563 (2008).

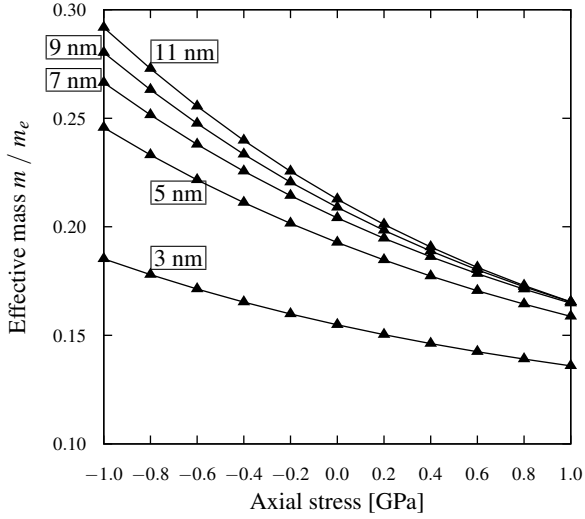


Fig. 1: Stress dependence of the effective mass in the unprimed (Γ) valley for [110] nanowires of different thicknesses

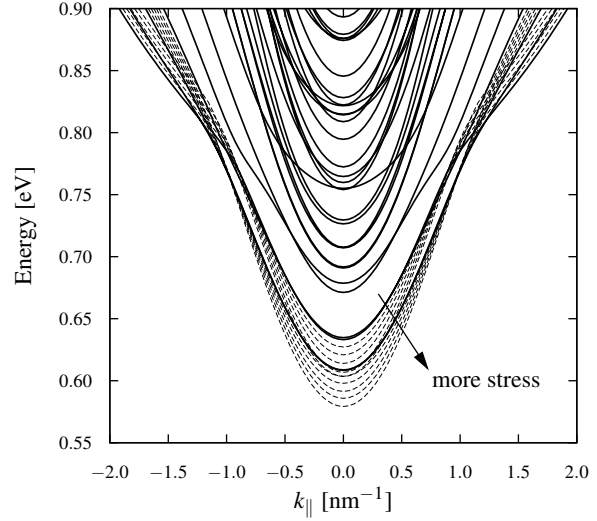


Fig. 4: Unprimed subbands in a [110] nanowire; solid line—unstrained, dashed lines—tensile axial stresses up to 1 GPa (shown for the four lowest subbands only)

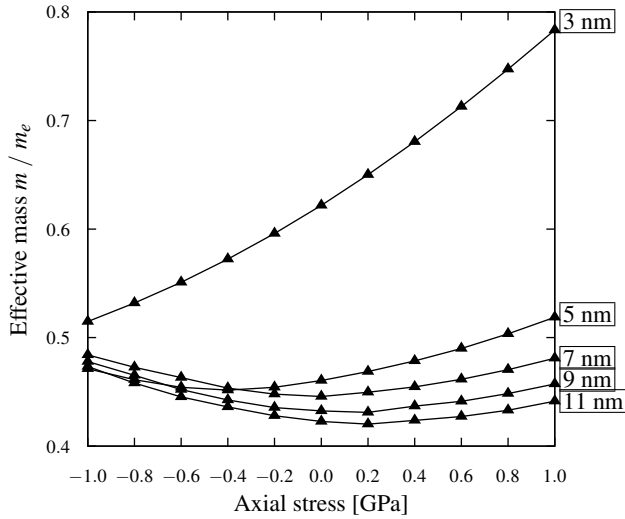


Fig. 2: Stress dependence of the effective mass for [111] nanowires of different thicknesses

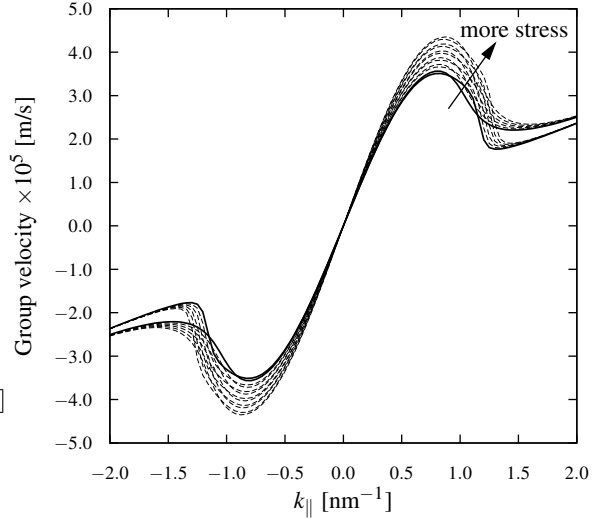


Fig. 5: Group velocities of the two lowest subbands in a [110] nanowire; solid line—unstrained, dashed lines—tensile axial stresses up to 1 GPa

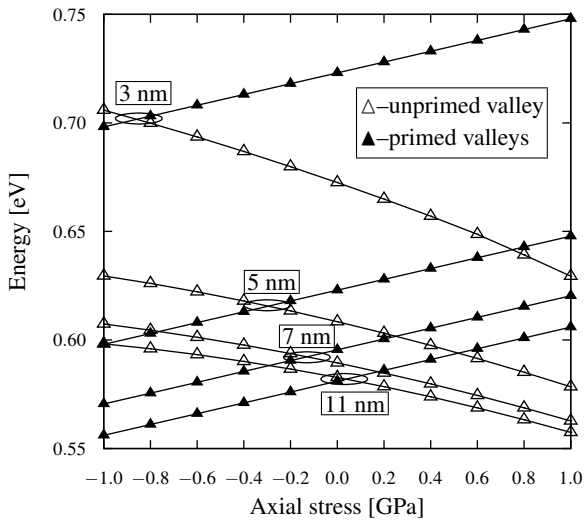


Fig. 3: Energy of valley minima for varying axial stress and different thicknesses of [110] nanowires

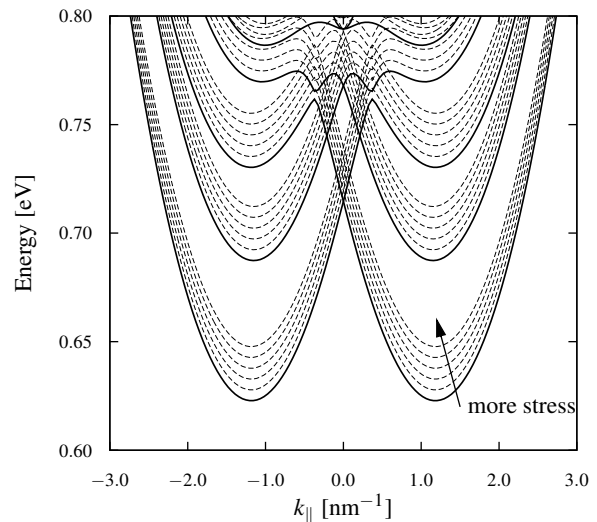


Fig. 6: Primed subbands in a [110] nanowire; solid line—unstrained, dashed lines—tensile axial stresses up to 1 GPa; plot is centered around the edge of the Brillouin zone.