Characteristics of P-Channel Polysilicon Conductivity Modulated Thin-Film Transistors

Chunxiang Zhu, *Student Member, IEEE*, Johnny K. O. Sin, *Senior Member, IEEE*, and Wai Tung Ng, *Member, IEEE*

***Abstract*—A p-channel polysilicon conductivity modulated thin-film transistor (CMTFT) is demonstrated and experimentally characterized. The transistor uses the concept of conductivity modulation in the offset region to obtain a significant reduction in on-state resistance. The conductivity modulation is achieved by injecting minority carriers (electrons) into the offset region through a diode added to the drain. Experimental results show that the conductivity modulation in the p-channel device is as effective as that in the n-channel device. This structure can provide 1.5 to 2 orders of magnitude higher on-state current than that of the conventional offset drainthin-film transistor (TFT) at drain voltage ranging from -15 V to -5 V while still maintaining low leakage current and simplicity in device operation. The p-channel CMTFT can be combined with the n-channel CMTFT to form CMOS high-voltage drivers, which is very suitable for use in fully integrated large-area electronic applications.**

***Index Terms*— Conductivity modulation, low temperature, polysilicon, thin-film transistor.**

I. Introduction

LOW-TEMPERATURE polysilicon thin-film transistor (TFT) appears to be one of the most promising technologies for the ultimate goal of building large-area electronic systems on glass substrate [1]. In flat panel liquid crystal, electroluminescent, and plasma displays, as well as other applications such as high-speed printers and page width optical scanners, etc., both efficient high-voltage drivers and control circuits have to be implemented on the same glass substrate for system integration [2]–[6]. For high-voltage drivers, conventional offset drain TFT is commonly used [7]. In this structure, the drain region is offset from the channel region in order to provide high breakdown voltage. However, the offset region adds to the structure a large series resistance, which leads to a severe current pinching problem. To alleviate this problem, a lightly doped offset region was used. However, the required implant charge density for a reproducible offset region is extremely difficult to determine [8]. An alternative way to solve the current pinching problem is to use a field-plated high-voltage TFT [9]. In this structure, an addition metal field plate to enhance the conductivity of the offset region is used. However, this approach results in a complicated device structure and biasing scheme. Recently, an n-channel conductivity modulated TFT (CMTFT) is proposed to solve the current pinching problem [10]. The device uses the concept of conductivity modulation in the offset region. Experimental results showed that it can provide orders of magnitude higher on-state current compared to the conventional offset drain TFT while still maintaining low leakage current. To further minimize the power dissipation and to facilitate circuit design, CMOS high-voltage drivers should be used. Thus, a high-performance p-channel CMTFT is needed.

In this paper, a p-channel poly-Si CMTFT is demonstrated and experimentally characterized. Results show that conductivity modulation in the p-channel CMTFT device is as effective as that in the n-channel device. Fabrication process, on-state/off-state current–voltage (I–V) characteristics, and breakdown voltage performance of the p-channel CMTFT will also be discussed.

Manuscript received November 12, 1998; revised February 1, 1999. This work was supported by the UGC Research Infrastructure Grant, Hong Kong SAR Government, Grant RI 95/96.EG24. The review of this paper was arranged by Editor C. Y. Yang.

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Publisher Item Identifier S 0018-9383(99)05095-9.

II. Device Structure and Operation

Schematic cross section of the p-channel conventional offset drain TFT and CMTFT are shown in Fig. 1(a) and (b). Channel region of the devices is lightly doped to n-type to make sure the device can be operated in the inversion mode with low leakage current and adjustable threshold voltage. The conventional offset drain TFT is a majority carrier device and with a lightly doped offset region placed between the channel region and the drain region for low leakage current and high breakdown voltage. The offset region adds a large parasitic resistance to the device especially for higher breakdown voltage devices. On the other hand, the CMTFT is a mixed carrier device. It uses the concept of conductivity modulation in the offset region by incorporating an n^+ drain instead of a p^+ drain used in the conventional p-channel offset drain TFT. The drain and offset regions can be viewed as a series combination of a diode with a drift resistance as shown in Fig. 1(c). When the gate voltage is above the threshold voltage and the drain-to-source voltage is high enough, the drain diode is turned on, and electrons are injected into the offset region from the n^+ drain. The injected electrons recombine with the traps associated with the grain boundaries and facilitate the flow of holes in the offset region. The high concentration of injected electrons modulates the resistivity of the offset region and reduces the on-state resistance dramatically compared to that of the conventional offset drain TFT. In order to prevent minority carrier (electron) accumulation in the channel region, it is necessary to connect the channel region of the device to the source. A segmented

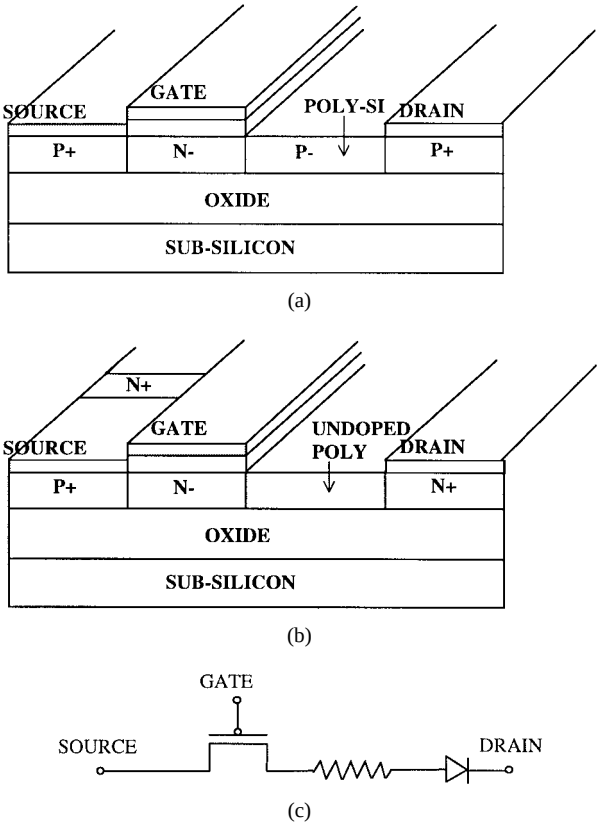

Fig. 1. Schematic cross section of (a) the p-channel conventional offset drain TFT, (b) the CMTFT, and (c) the equivalent circuit of the p-channel CMTFT.

source structure with 10 : 1 segmentation ratio (p^+ to n^+) is used as shown in Fig. 1(b).

In contrast to the conventional offset drain TFT in which a lightly doped offset region is used, the CMTFT uses an undoped offset region. The breakdown voltage of the CMTFT is therefore dependent on the channel length and the undoped offset region length. At zero gate voltage, the large drain voltage is blocked by the reverse biased junction formed by the intrinsic offset region and the channel region.

III. Device Fabrication

To demonstrate the performance of the p-channel CMTFT, both the p-channel conventional offset drain TFT and CMTFT have been fabricated on the same substrate using low-temperature (600 °C) process. The major fabrication steps of the p-channel CMTFT are shown in Fig. 2. Silicon wafers with a layer of thermally grown oxide (5000 Å) are used as starting substrate. A layer of amorphous silicon (2000 Å) is first deposited on the oxide at 550 °C using LPCVD. It is then recrystallized to polycrystalline silicon by furnace annealing at 600 °C in nitrogen ambient for 20 h. Afterwards, the device islands are defined by plasma dry etching. Channel region of the devices is then doped with phosphorus of an implant dose of 1×10^{12} cm^{-2}. In the case of the conventional offset drain TFT, boron implant with dose of 1×10^{12} cm^{-2} is used to dope the offset region. After that, a 1000 Å layer of oxide is deposited as gate oxide using APCVD. The gate polysilicon layer is then deposited at 600 °C using LPCVD

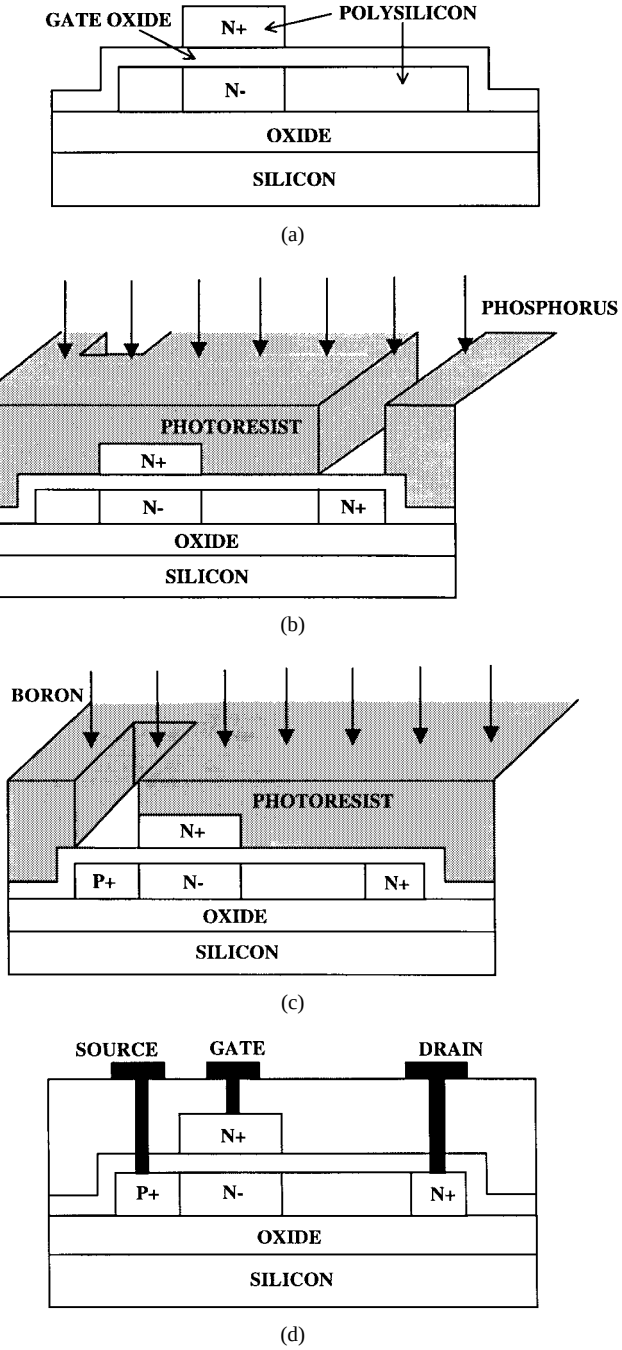

Fig. 2. Major fabrication steps of the p-channel CMTFT.

with a thickness of 2500 Å. After that, it is doped by a 40 keV phosphorus implant with a dose of 4×10^{15} cm^{-2} and patterned. The source region is doped by a 33 keV boron implant with a dose of 4×10^{15} cm^{-2}, and the drain region is doped by a 40 keV phosphorus implant with a dose of 5×10^{15} cm^{-2}. In the case of the conventional offset drain TFT, no phosphorus implant at the drain is needed. Instead, the drain will be doped using the same source implant. After the source/drain implantation, 3500 Å of LTO is deposited and densified at 600 °C in oxygen ambient for 10 h and in nitrogen ambient for 2 h. The dopants are activated during the LTO densification. Contact holes on the LTO layer are opened using dry etching. A layer of Al is then deposited

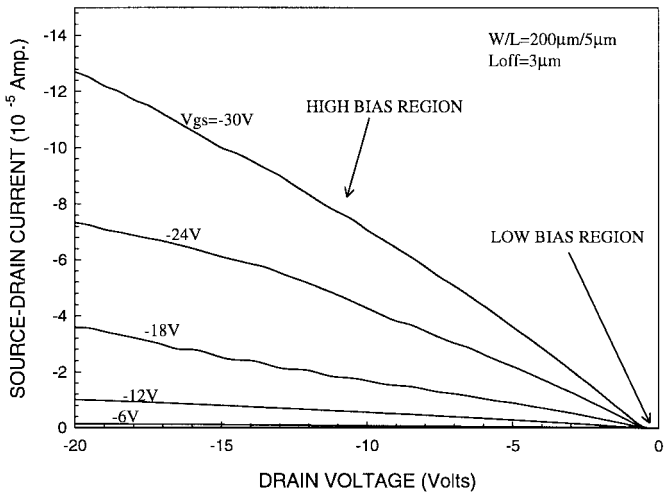

Fig. 3. Experimental $I-V$ characteristics of the p-channel CMTFT.

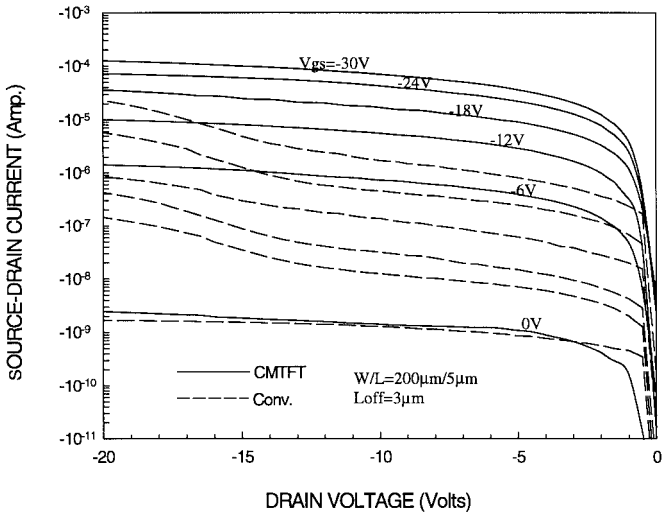

Fig. 4. Forward conduction characteristics of the p-channel CMTFT and conventional offset drain TFT.

using sputtering method with a thickness of 1 μm. After metal patterning, forming gas annealing is performed at 400 °C for 30 min. Finally, the devices are hydrogenated in r.f. hydrogen plasma for 2 h.

IV. Results and Discussion

Our results reported here represent majority of the device performance and are taken as the average value of over ten devices in the different regions of the wafer. Fig. 3 shows the experimental $I-V$ characteristics of the p-channel CMTFT. The $I-V$ characteristics exhibit a low bias region and a high bias region. The transition voltage between the two regions is at approximately -0.5 V, which is in fact the turn-on voltage of the drain diode. At the drain voltage less than the turn-on voltage, the drain diode is off, and the device is basically off. As the drain voltage is increased and above the diode turn-on voltage, the drain diode is turned on, and the device is operated in the high bias region. In this region of operation, minority carriers (electrons) are injected into the offset region and modulate the offset region resistance for significant increase in drain current.

Fig. 4 shows the forward conduction characteristics of the conventional offset drain TFT and CMTFT. Both devices have the same offset length of 3 μm and W/L ratio of 200 μm/5 μm. It is shown that the conventional offset drain TFT experiences severe current pinching due to the high resistance in the lightly doped offset region. For the device at low forward-bias, most of the voltage is dropped across the offset region, and the hole carriers flowing in from the channel fill the traps at the grain boundaries in the offset region. Therefore the current is rather low. When the drain voltage is increased, the potential barrier formed by grain boundaries is overcome, and the drain current becomes higher. In the case of the CMTFT, also shown in Fig. 4, the current pinching problem is minimized. This can be explained as follows. As the gate voltage is above the threshold voltage and the drain voltage is below the turn-on voltage of the drain diode, the drain diode is off, and no electrons are injected from the drain. The device is in the off-state. When the drain voltage is increased beyond the turn-on voltage, the drain diode is turned on; electrons are then injected into the offset region. Existence of the electrons in the offset region reduces the barrier height formed between the grain boundaries and enhances the flow of both electrons and holes in the offset region. Thus, the conductivity in the offset region is modulated, and the on-state resistance is reduced dramatically, resulting in a significant increase in on-state current. From Fig. 4, the on-state current of the CMTFT is 1.5 to 2 orders of magnitude higher than that of the conventional offset drain TFT at a gate voltage of -24 V and drain voltages ranging from -15 V to -5 V.

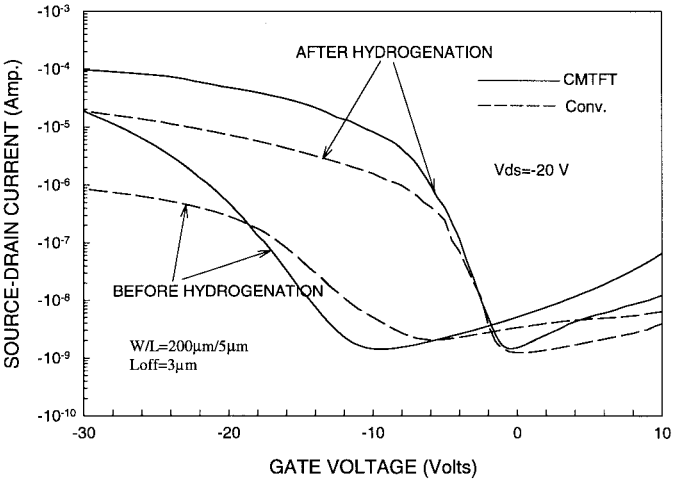

Fig. 5. Gate transfer characteristics of the p-channel CMTFT and conventional offset drain TFT.

Fig. 5 shows the gate transfer characteristics of the p-channel conventional offset drain TFT and CMTFT before and after hydrogenation. Both devices have the same dimensions as those stated in Fig. 4. The threshold voltage, subthreshold slope, and leakage current are all improved after hydrogenation for both devices. The leakage current of the CMTFT is comparable with that of the conventional offset drain TFT. At a drain voltage and gate voltage of -20 and -24 V, the

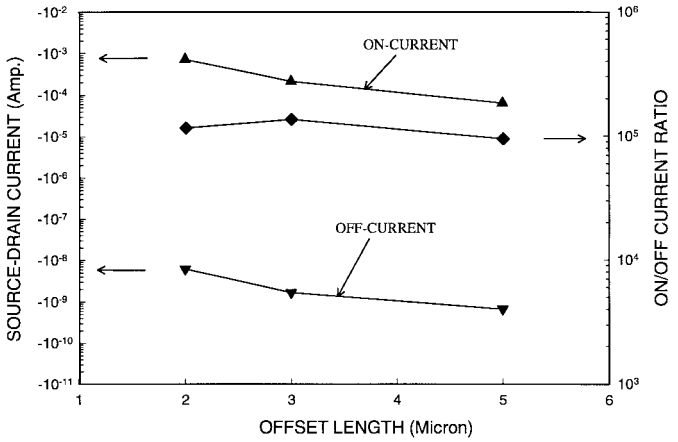

Fig. 6. On-current and off-current versus offset length for the p-channel CMTFT.

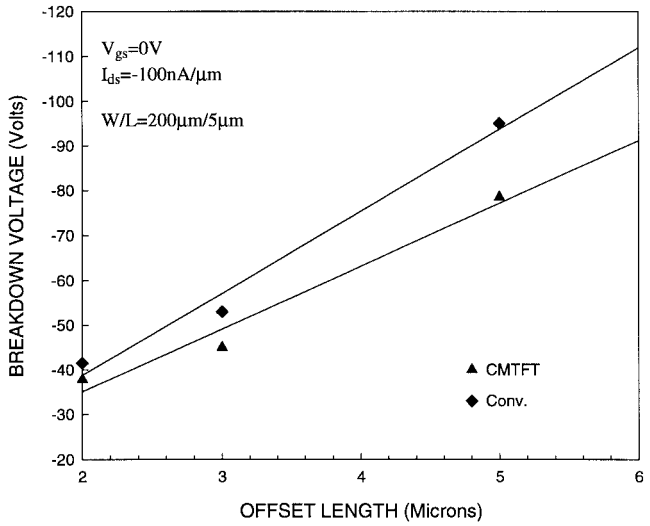

Fig. 7. Breakdown voltage versus offset length for the p-channel CMTFT and conventional offset drain TFT.

on/off current ratio of the CMTFT is six times larger than that of the conventional offset drain TFT.

The on-current and off-current of the CMTFT as a function of offset length are shown in Fig. 6 with a W/L ratio of 200 μm/5 μm. The on-current is measured at a drain bias of -20 V and a gate bias of -24 V. As expected, the on-current of the CMTFT decreases with the increase in offset length. As the offset length increases, the on-state resistance increases, which leads to a reduction on the on-current of the device. The off-current is measured at a drain bias of -20 V and a gate bias of 0 V. The off-current also decreases with the increase in offset length. As the offset length increases, the lateral electric field at the drain region decreases, which results in a corresponding reduction on the off-current. Since both the on-current and off-current are reduced at longer offset length, a relatively constant on/off current ratio is obtained. The on/off current ratio as a function of offset length is also shown in Fig. 6.

Fig. 7 shows the breakdown voltage of the p-channel CMTFT as a function of offset length. The devices are with a W/L ratio of 200 μm/5 μm. The breakdown voltage is measured at a drain current of -100 nA/μm. It is shown that the breakdown voltage increases fairly linearly with the increase in offset length. This is due to the reduction of electric field at the channel/offset junction as the offset length is increased, which lowers the impact ionization and in turn causes the breakdown to occur at a higher voltage. The breakdown voltage of the conventional offset drain TFT as a function of offset length is also plotted in Fig. 7 for comparison. The CMTFT's have approximately 9–17% lower breakdown voltages compared to those of the conventional offset drain TFT's for offset length from 2 to 5 μm. For the CMTFT, the large drain voltage is supported by the n^+ (segmented) $n/^-/i/n^+$ parasitic resistor structure. However, in the case of the conventional offset drain TFT, the breakdown voltage can be considered as the BV_{CEO} of the $p^+/n^-/p^-/p^+$ parasitic bipolar structure. Figs. 6 and 7 show that higher breakdown voltage p-channel CMTFT can be obtained with high on/off current ratio.

Since the p-channel CMTFT has involved minority carriers (electrons) in the conduction mechanism, the switching speed of the device might be affected by the minority carrier (electron) storage effect. However, due to the high trap density in polysilicon film, the minority carrier (electron) lifetime is very short [11]. Therefore, the transient behavior of the device should not be degraded compared to the conventional offset drain TFT. The switching characteristics of the p-channel CMTFT and conventional offset drain TFT are measured by using a resistive load connected between the drain and power supply with the source grounded. To compare the switching performance, both devices (W/L $=$ 200 μm/5 μm, $L_{\text{off}} = 3$ μm) are biased at the same drain to source and gate to source voltage of -20 V and -17 V, respectively. The identical drain to source voltage for both devices are obtained by adjusting the load resistance. The turn-off times of the CMTFT and conventional offset drain TFT are 51.2 and 84.5 μs, respectively. The improvement in turn-off time of the CMTFT is due to its higher current sourcing capability. The turn-on times of the CMTFT and conventional offset drain TFT are 27 and 41.3 μs, respectively. The reduction in turn-on time of the CMTFT is due to its much smaller on-state resistance which discharges the parasitic capacitance of the system[1] faster.

V. Conclusion

A p-channel poly-Si CMTFT is demonstrated and experimentally characterized. Results showed that the concept of conductivity modulation in the p-channel device is as effective as that in the n-channel device. With the increase in offset length, higher breakdown CMTFT driver devices can be obtained. The p-channel CMTFT, together with the n-channel counterpart, can be used to implement CMOS high-voltage drivers for a variety of fully integrated large-area electronic applications which require high-voltage driving capability.

[1] It is important to note that the relatively slow switching speed measured for both structures is due to the large RC time constant of the parasitic capacitance inherent in the measurement system. However, as far as comparison is concerned, the measurement can still serve the purpose.

ACKNOWLEDGMENT

The authors would like to thank Vitelic Ltd. , Hong Kong, for providing the APCVD and ion implantation processes, and the fabrication staffs at the HKUST for their constant support.

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