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Using Theory CMOS Active Inductors in Low Noise Amplifier

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ABSTRACT

In this paper we present LNA with active inductor circuits are employed to assess their suitability for providing a tuning function in HEMT circuits. Comparisonof measurement and simulation ofan active inductor shows the high quality factor. Simulations ofthe low noise amplifier show the advantages of active inductorswith similar performance even in regard to the noise figure**..** The design and simulation of the circuits employs a low-cost commercially available low pinch-off HEMT process.

Keywords: *Active inductors, HEMT, LNA, ADS*

1. INTRODUCTION

With decreasing channel length and thereby increasing transit frequency HEMT technology becomes more attractive for RF components in mobile communication products. One of the key circuits in the RF front end is the low noise amplifier (LNA), which requires inductors for the impedance and noise matching. On-chip passive inductors exhibit poor quality-factor and require large silicon die area.

2. DESIGNAMPLIFIER

The single-stage amplifier circuit topology selected for this work is shown in Figure 1. This circuit configuration and the design procedure are well established. The amplifier specifications could of course be achieved with other circuit topologies but the one selected serves as a good vehicle for illustrating some of the limitations of the use of active inductors. Of the devices available in the F20 process library, the six-finger 150 mm gate width=finger (900 mm total gate-width) low pinch off (V_P¼_1V) component element was selected as being the most suitable for the amplifier. Biased for maximum efficiency at 20% of the maximum current and a drain-source voltage (V_{DS}) of 3V. With these bias conditions the input and output matching components were optimized to satisfy the specifications at 2.5GHz. With the bias conditions to the device and the capacitor values kept constant, the tuning range was then explored by adjusting the inductance values.

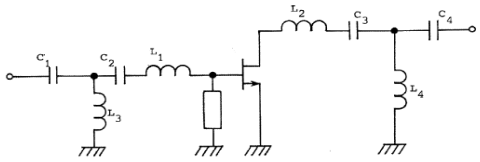

Fig 1: Amplifier Circuit Topology

This showed that the amplifier could be tuned over a wide frequency range and still meets the same specifications at different frequencies. the matching element values at 2 GHz with the device biased as stated above. For the center frequency specified, the stability criteria were met by employing a 500Ohmshunt resistance as shown in Figure 9. Although the results shown in figure 10and11 do not take into account interconnect effects, it nevertheless gives a good indication of the inductance range required from the active inductors. Such a broad frequency tuning range especially the lower frequency area, whilst useful, may however be unnecessary in the case of the mobile handset market where the trend seems to be for higher frequency of operation

3. THEORY CMOS ACTIVE INDUCTORS

3.1. Design Shunt Active Inductor

To alleviate the limitations imposed on the chip area and the quality (Q) factors of the spiral inductors, active designswere proposed to implement the required on-chip inductance.

For RF applications, the regulated cascade topology is commonly used in the design of CMOS active inductors.
Fig. 2 shows the schematic of the active inductor. As the input voltage applies to the gate terminal of the common-source transistorM1 , the transconductance gm1 converts the voltage to adrain current charging the capacitance Cgs2 of transistor M2 .The voltage established across Cgs2 is then converted to theinput current by the transconductance of M2, emulating the current–voltage characteristics of a shunt inductance. Note that thetransistor M3 is used as the gain-boosting stage to enhance the Q factor of the active inductor, while the required bias currentsfor M1 andM2 are provided by the current mirrors .From the small-signal analysis, the nodal voltages andcan be expressed as M4-M7 From the small-signal analysis.

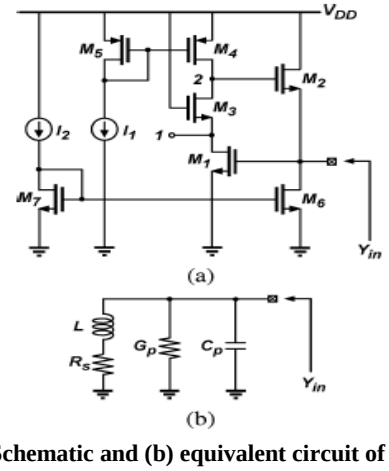

Fig. 2:(a) Schematic and (b) equivalent circuit of the regulated cascade active inductor.

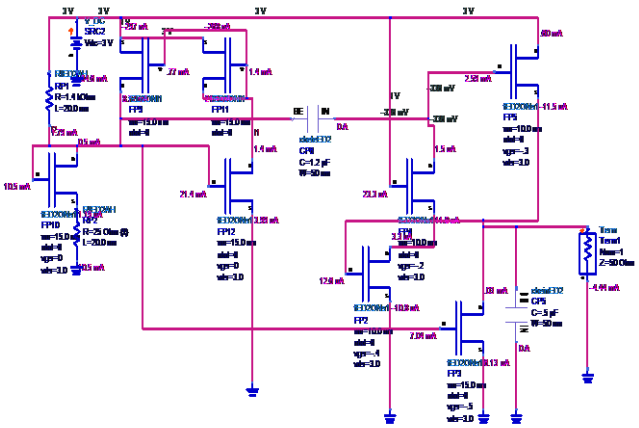

Fig 3: Schematic Active Inductor for this work

3.2 Design Series Active Inductor

Fig.4 shows the characteristics of aconventional spiral inductor and active inductorsmentioned above. The resonant frequency, which is the maximum inductor operating frequency, iscompared to the inductance value at lGHz**,** where lines show the calculated characteristics and dotsshow the measured data for active inductor. **As**shown in Fig.3, the operating frequency range ofactive inductor is higher than that of a spiralinductor especially in the high inductance region.The difference between the calculated and measureddata for the active inductors is due to uncountedconnecting lines and parasitic capacitance in theinductor chips.

A photograph of a fabricated CGF-feedback activeinductors and a circuit configuration are shown inFig.5. Four 0.5um*100umsingle-gate implantedFETsare employed, where one FET is used for Dcbiasing. This circuit configuration is availablefor both series and shunt inductors. In theactive inductor itself, dc power consumption is about 70mV**.** The measured and predicted impedance of the active inductor are shown in Fig.5, wherethe port 2 is grounded. The ***Q*** value is about **2**at 3GHz**. A** higher **Q** value can be obtained byusing a FET with a wider gate as cascade FET.

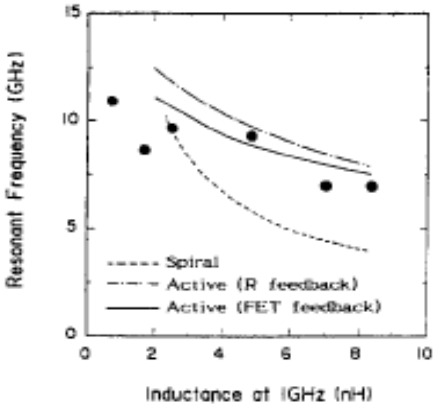

Fig.4: Resonant-Frequency Comparison of the Activeinductors and the Conventional Spiral Inductor

Chain-dotted and solid lines representingresistor feedback and *CGF* feedback active inductors,respectively, and dashed line representingspiral inductor are calculated at 1GHz**.** Dotsrepresent measured data for active inductors.

A schematic of common-gate cascadeFET feedbackactive inductor is shown in Fig.6. **A** shuntresistor, with the same magnitude as theequivalent negative resistance shown in Table **1,**is connected to obtain a lossless inductor. Theloss of this active inductor can be much lowerthan that of any other active inductors, andfurthermore, the inductance value can be varied bychanging the voltage, V, of the second gate ofthe feedback cascadeFET**.** Fig.7 shows themeasured impedance of the cascade FET feedbackactive inductor, where the impedance is represented by series resistance and inductance. Themaximum ***Q*** factor of 65 is obtained at about **8GHz,**where the shunt resistor value is selected to makethe active inductor stable at all frequencies.

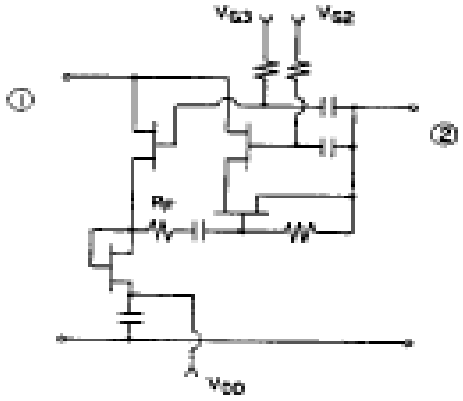

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Fig.4: Schematics of Circuit Configuration the Active Inductor

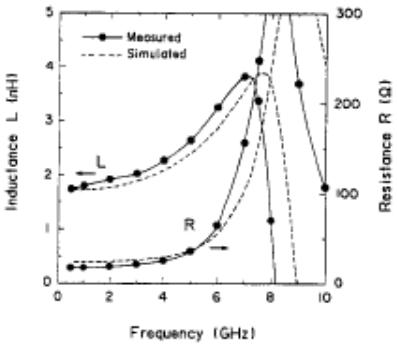

Fig.5: Impedance-frequency characteristics of the CGF feedback active inductor. Impedance is represented by series resistance and inductance

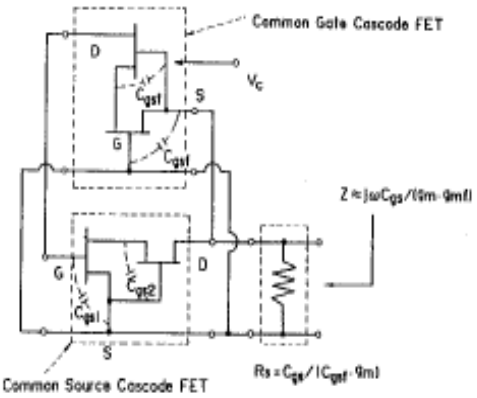

Fig.6:Circuit configuration of the cascade FET feedback active inductor with a shunt resistor.

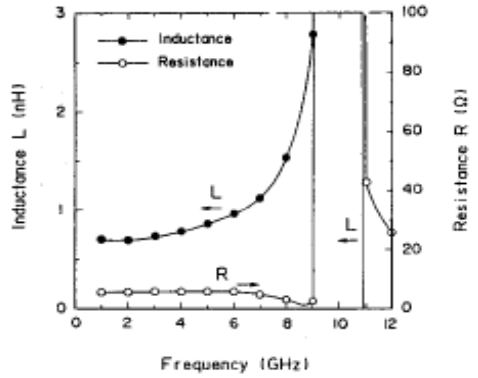

Fig.7:Impedance-frequency characteristics of the cascadeFFll feedback active inductor. Impedance is represented by series resistance and inductance

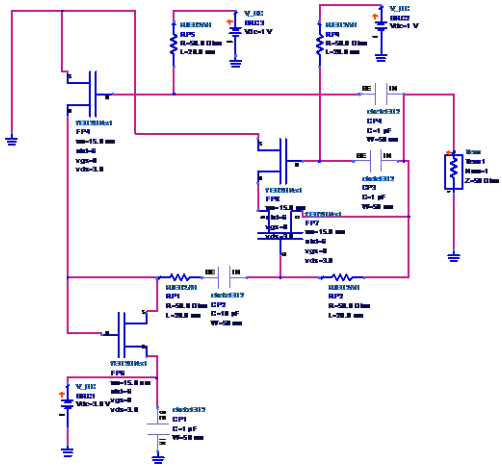

Fig 8: SchematicSeries active inductor for this work

4. DESIGNLOW NOISE AMPLIFIERWITH COMPO-NENT ELEMENT ADS

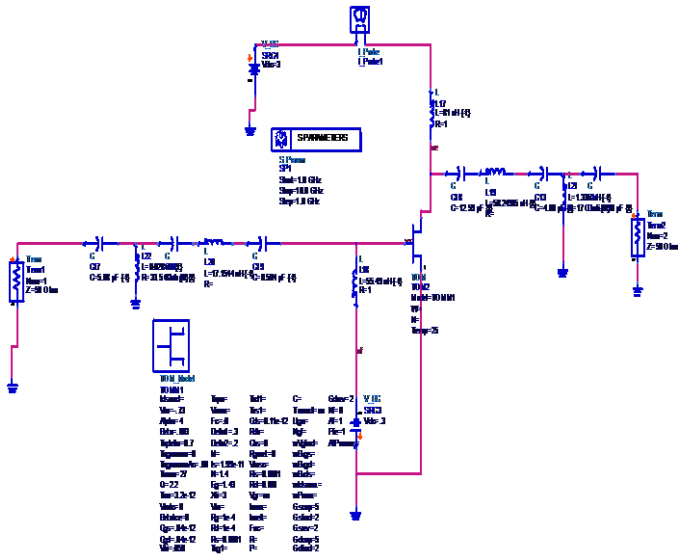

Fig 9: Schematic Design of component element ADS

Fig10And11 Showsthe Result ofLow noise Amplifier with Component Element ADS in 2GHz center frequency.

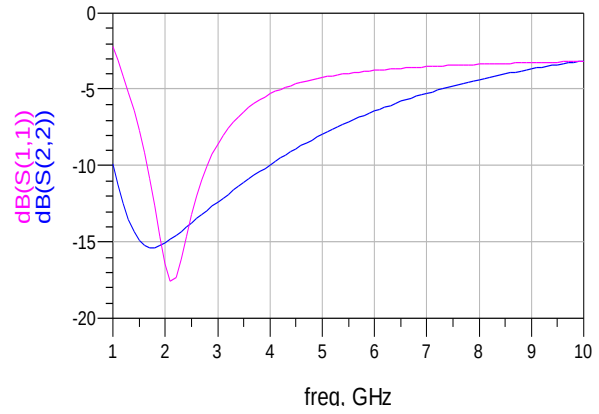

Fig 10:Impedance Matching Low Noise AmplifierWith Component Element ADS

Fig 11.dB(S21)Low Noise Amplifier With Component Element ADS

5. DESIGN OF LOW NOISE AMPLIFIER ACTIVEINDUCTOR WITH ED02AH TECHNOLOGY

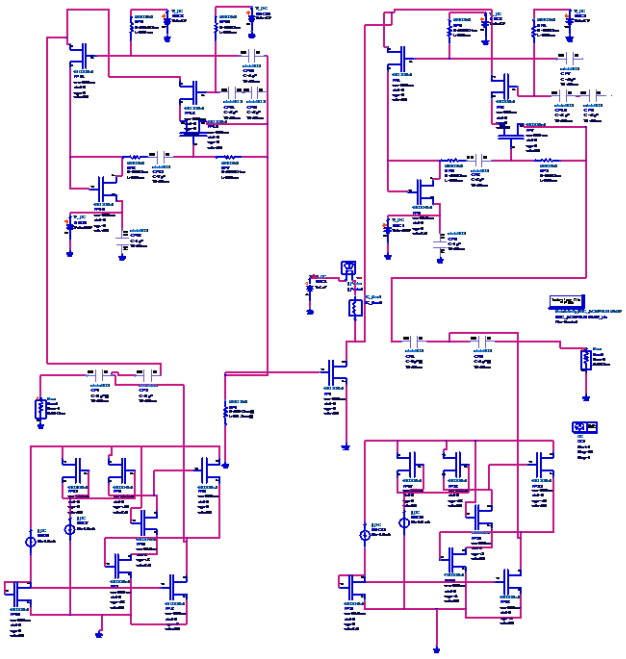

Fig 12:Schematic of Low Noise Amplifier active inductor with ED02AH technology

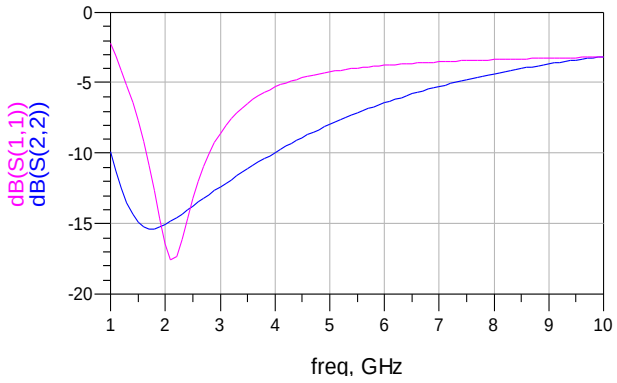

Fig 13.dB(S22) and dB(S11) of Low Noise Amplifier active inductor with ED02AH technology

Fig 14.dB(S21) of Low Noise Amplifier active inductor with ED02AH technology

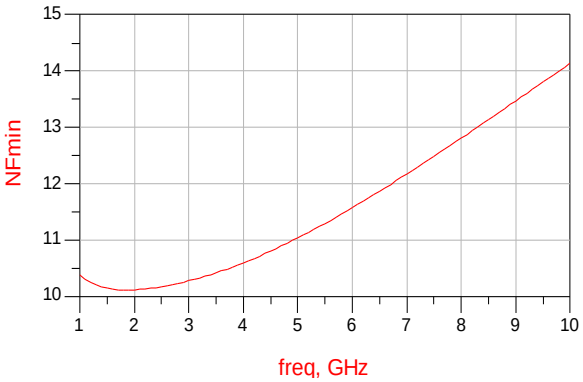

Fig 15.NF of Low Noise Amplifier active inductor with ED02AH technology

6. CONCLUSION

In this work we present Design with technology ED02AH .Simulations of the low noise amplifier show the advantages of active inductors with similar performance even in regard to the noise figure.

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