

Comparative Analysis of Self-Controllable Voltage Level (SVL) and Stacking Power Gating Leakage Reduction Techniques Using in Sequential Logic Circuit at 45Nanometer Regime

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Abstract

Today leakage power has become an increasingly major issue in low power VLSI design. With the most important element of leakage, the sub-threshold current, exponentially increasing with decreasing device dimension, leakage commands associate ever increasing share in the processor power consumption. In this paper two techniques such as transistor stacking and self controllable voltage-level (SVL) circuit for reducing leakage power in sequential circuits are proposed. This work analysis the power and delay of three different types of D Flip-flops using pass transistors logic, transmission gates and gate diffusion input (GDI) cmos design style. All the circuit parameters are simulated with and without the application of leakage reduction techniques. All these proposed circuits are simulated with and without the application of leakage reduction techniques. The circuits are simulated using Cadence Virtuoso tool at 45nm technology for various parameters

Keywords: Pass Transistors Logic, Transmission Gate, GDI, Self-Controllable Voltage Level (SVL) technique, Stacking Power Gating.

I. INTRODUCTION

CMOS technology has been scaling down to meet the performance, production cost and power requirements of the industry [1]. With the rapid growth of transportable electronic devices, low power design is crucial in the design of electronics. Therefore, the main focus of the industry has modified from high performance designs to low power designs to meet the demands of the transportable electronics. Since the battery period is a key factor for a portable device, both the electronic industry and the battery industry have been attempting to address this need [3] [4]. However, power reduction is also an issue in high performance computers where heat dissipation has become a major bottle neck in keeping the processors at proper operating temperatures [5]. This is due to the growing power per unit area as a result of the reduction in the minimum feature size of the process technology, which allows a designer

integration of transistor with higher speeds in each chip. During this paper we design and analysis of various style approach D flip-flop circuits using with Stacking power gating and SVL leakage reduction techniques.

This paper is organized as follows: in Section 2 describes self controllable voltage-level (SVL) and stacking power gating leakage reduction techniques that are applied to the proposed designs. Section 3 presents three different designs of D flip-flops using pass transistor logic, transmission gates and Gate-Diffusion Input (GDI) gates. Section 4 presents the simulation and results of the flip-flops and section 5 gives the conclusion.

II. CMOS IMPLEMENTAATION OF D FLIP-FLOP CIRCUITS

The flip-flops are basic memory storage element in digital circuits that store one bit information [9]. This section presents the three

different design style of CMOS technology which is used to implement the D flip-flops circuits. These proposed circuits are combined pair of master and slave D latch circuit. The wide use of sequential logic and memory storage systems in modern electronics results in the implementation of low power and high speed design of basic memory elements. One of the most important basic memory elements is the D flip-flop (DFF). Three different designs of D flip-flops in CMOS logic are presented in this section. The D flip-flop combines a pair of master and slave D latch. Design –I uses pass transistors logic (PTL) and inverters for the master-slave latches [10] as shown in Fig. 1. The two chained inverters are in memory state when the PMOS loop transistor is on, that is when $clk = 0$. Other two chain inverters on the right hand side acts in the opposite way.

The flip-flop changes its state during the falling edge of the clock. Fig 2 shows the design – II that uses transmission gates (TG) and inverters [11]. Transmission gate is an important structure implemented using CMOS integrated circuit that sustains switch function, efficient layout and logic reduction. PMOS and NMOS transistors are used to implement this solid state switch. Transmission gate and inverters are utilized to implement D flip flop as illustrated in Figure 2 shows. At the negative edge of the clock period, transmission gates T1 and T4 are ON and transmission gates T2 and T3 are OFF. During this time the slave maintains a loop through two inverters P3, P4 and T4. Currently the previous triggered value from Din is stored in the slave. At the same time master latches next state but as T3 is OFF it is not passed to slave. At the positive clock edge T2 and T3 are turned ON and the new latched value passes to slave through the loop of two inverters P1, P2 and T2. Fig. 3 shows design –III with master-slave connection of two GDI D-latches [13]. The power dissipation is optimized by GDI technique and reduces the number of transistor. For two-transistor implementation of logic functions and restoration of in-cell swing within certain operation conditions,

GDI technique offers unique advantage for low power design techniques. Representation of two GDI based latches connected as master-slave configuration is illustrated in Figure 3. In this the body gates are responsible for the state of the circuit. These gates are controlled by the control signal i.e. clock (clk) signal and create two alternative paths. One for transparent state of the latch ,when the clock is low and the signals are propagating through PMOS transistors .The other one is for the holding state of the latch ,when the clk signal is high and internal values are maintained due to conduction of the NMOS transistors. The inverters are responsible for maintaining the complementary values of the internal signals and the circuit outputs.

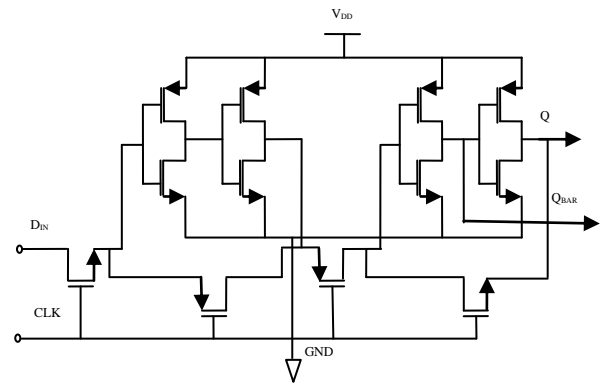


Fig.1. D flip-flop using Pass transistors

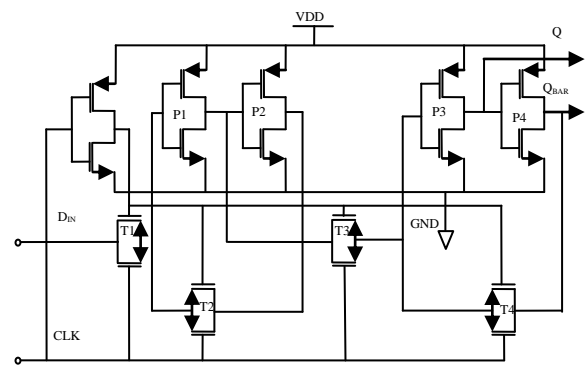


Fig.2. D flip-flop using transmission gates

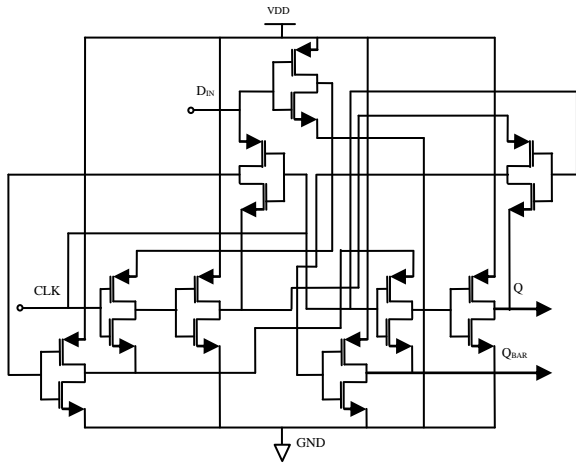


Fig.3. D flip-flop using GDI gates

III. PROPOSED LEAKAGE REDUCTION TECHNIQUES

In this section two leakage reduction techniques namely transistor stacking and self-controllable voltage level circuit that are applied to the above circuits are described.

A. Self-Controllable Voltage Level (SVL) Circuit for Low Power, High Speed CMOS Circuit

The SVL technique is used to minimize the leakage power of the circuit. Three types of self controllable voltage level circuit these are Upper SVL, Lower SVL and combination of both upper and lower SVL circuits have been proposed in this paper [12]. The figure 4 shows all these proposed SVL techniques which are applied on CMOS inverter for simplicity of explanation of the SVL circuit function. The circuits are operated in both operation modes which is Active mode and standby mode. When our circuit is working inactive mode at that time $CL = '1'$ and $CLB = '0'$. So our circuit will get maximum supply voltages and circuit will work in proper manner. When our circuit is working in standby mode at that time the value of $CL = '0'$ and $CLB = '1'$. So due to series connection of transistors, the value of V_D (Virtual Ground) will be minimum as compared to V_{DD} due to voltage drop. Same phenomenon is also occur in the Lower SVL circuit. Due to voltage drop the value of V_s will be greater as compared to V_{ss} . Finally it is said that

by using this technique the overall voltage of the circuit will be minimum. And when the circuit works on minimum voltage the leakage power is also reduced. The upper SVL circuit consists of a single PMOS act as a switch and a stack of two NMOS act as a resistors as shown in figure4 (a). In figure 4 (b) shown the lower SVL circuit, which is constructed by using of a single NMOS transistor and multiple PMOS act as a resistors connected in series. The combine circuits of both SVL circuits are also shown in figure 4(c) [13] [14].

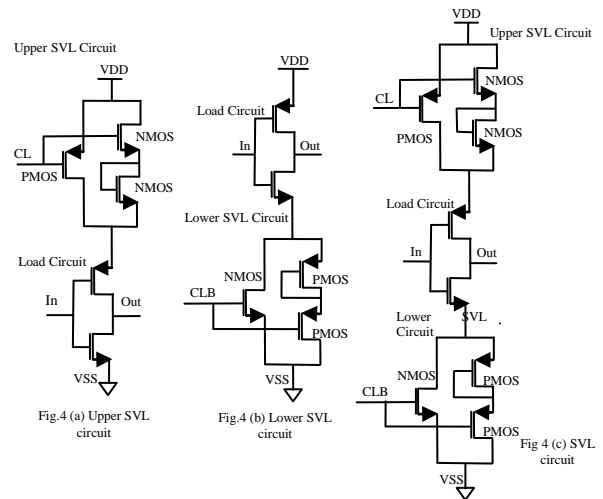


Fig. 4. SVL Circuits

B. Stacking Power gating technique

Power gating requires, for each circuit that can be turned off, the presence of a header (or footer) "sleep" transistor that can set the supply voltage of the circuit to ground level (or V_{DD} level for footer) throughout idle times. Power gating also requires control logic to predict when would be a good time to power gate the circuit [15]. This technique uses high threshold voltage sleep transistor that cut-off a circuit block when the block is not switching [16]. Here the sleep transistor is connected between actual ground rail and virtual ground [17], [18]. This insertion of sleep transistor divides the power network into a permanent power network connected to the power supply and a virtual power network that drives the cells and can be turned off during inactive period.

The figure 5 shown the power gating technique are applied on inverter circuit. In this circuit, the supply voltage is turned off during the standby mode by using a PMOS transistor or an NMOS transistor; with proper switch sizing leakage-power can be reduced by more than two orders of magnitude. In active mode, the sleep transistor is on and the circuit functions as usual. In standby mode, the switch transistor is turned off, which disconnects the logic gate from power or ground. The basic mechanism by which the switch transistor reduces the leakage current of the power gated logic transistors is the increased body effect.

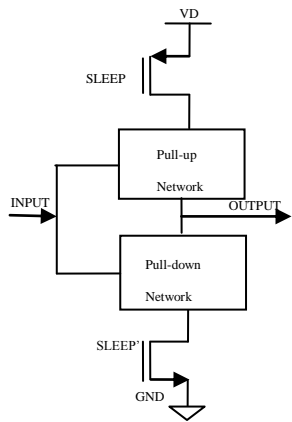


Fig. 5. Stacking power gating technique

IV. SIMULATION AND RESULT

The proposed circuits are simulated on “cadence virtuoso tool” using specter simulator at 45nm CMOS technology. Figure 4 show input output waveform of the D Flip-Flop circuit. The table 1 gives the comparative results of power and delay of proposed D Flip-Flops circuits with three different design style of CMOS logic. The obtained result of active and leakage power of D flip-Flop circuits with and without using of proposed SVL and stacking power gating techniques are presented in table 2, 3 and 4.

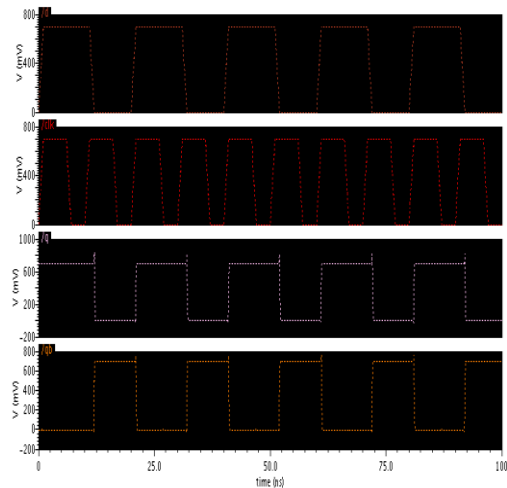


Fig. 6. Input Output waveform of D Flip-Flop circuit

Table 1
Show comparison result of delay and average power of designed D Flip-Flop circuits

DFF Design using	No. Of Transistor count	Delay	Avg. Power
PASS Transistors logic	12	21.93NS	426.0NW
Transmission Gate	18	20.51PS	41.55NW
Gate Diffusion Input (GDI)	18	14.68NS	37.56NW

Table 2
Show Active and Leakage power of Conventional D Flip-Flop Circuits

Conventional DFF Design using	Active Power	Leakage Power
PASS Transistors logic	426.0nw	297.1nw
Transmission Gate	41.55nw	10.1pw
Gate Diffusion Input (GDI)	40.25nw	13.87pw

Table 3
Show Active and Leakage power of D Flip-Flop combination of both SVL (upper and lower) Technique based Circuits

DFF DESIGN USING SVL CIRCUIT	ACTIVE POWER	LEAKAGE POWER
PASS Transistors logic	286.9nW	230.0nW
Transmission Gate	40.89nW	9.1pW
Gate Diffusion Input (GDI)	37.56nW	12.80pW

Table 4
Show Active and Leakage power of D Flip-Flop using stacking power gating Technique based Circuits

DFF Design Using Stacking	Active Power	Leakage Power
PASS Transistors logic	2.65 μ W	1.567nW
Transmission Gate	2.237 μ W	3.99pw
Gate Diffusion Input (GDI)	2.053 μ W	2.59pw

V. CONCLUSION

In this paper three CMOS implementations of DFFs using pass transistor logic (PTL), transmission gates and GDI based circuits are proposed. The comparison of average power and delay of proposed circuits are shown in this paper. As per simulation result the GDI based circuits are useful for low power applications, because these CMOS design styles exhibit minimum power as compared to other CMOS design style. The leakage power of all the designs decrease when reduction techniques are applied. This paper also

gives comparative analysis of leakage power with different CMOS logic style with and without using of leakage reduction technique. As per simulation result the stacking power gating technique is more effective of all design style as compared to SVL technique. All the simulation results are studied and verified on 'cadence virtuoso tool' at 45nm CMOS technology with 0.7V.

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REFERENCES

- [1] D. J. Frank et al., "Device Scaling Limits of Si MOSFETs and Their Application Dependencies," Proceedings of the IEEE, Vol. 89, No. 3, pp. 259-287, March 2001.
- [2] S. Borkar et al., "Parameter Variations and Impact on Circuits and Microarchitecture," Proceedings of the IEEE Design Automation Conference, pp. 338-342, June 2003.
- [3] S. H. Kulkarni and D. Sylvester, "High Performance Level Conversion for Dual VDD Design," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 12, No. 9, pp. 926 - 936, September 2004.
- [4] S. Borkar, "Design Challenges of Technology Scaling," IEEE Micro, Vol. 19, Issue 4, pp. 23- 29, (July-August) 1999.
- [5] Malya Ranjan Tripathy "nano CMOS", SRBmag-An Interdisciplinary Open Access Journal, Vol. 1,Page 19-23 ,2009.
- [6] K. Roy and S. C. Prasad "low-power CMOS vlsi circuit design," Wiley Publishers, New York, 2000.
- [7] Mark C. Johnson, Dinesh Somasekhar, Lih-Yih Chiou, Kaushik Roy "Leakage control with efficient use of transistor stacks in single threshold CMOS" IEEE Tran. VLSI Syst., vol. 10, NO. 1, Feb.2002.
- [8] Siva Narendra, Shekhar Borkar, Vivek De, Dimitri Antoniadis, Anantha Chandrakasan "Scaling of

stack effect and its application for leakage reduction" ISLPED, Aug.2001.

- [9] Saranya. L, Prof. S. Arumugam," Optimization of power for sequential elements in pulse triggered Flip-Flop using low power topologies," international journal of scientific & technology research, Vol.2, march 2013.
- [10] Doshi N. A, Dhobale S. B, and Kakade S.R, 2008, "LFSR Counter Implementation in CMOS VLSI", World Academy of Science, Engineering and Technology 48, 2008.
- [11] Morgenstein, A.Fish, I.Wagner, "A Efficient Implementation of D Flip- Flop Using the GDI Technique", ISCAS'04, pp.673-676, 2004.
- [12] Tadayoshi Enomoto, Yoshinori Oka, Hiroaki Shikano, and Tomochika Harada," A Self-Controllable-Voltage-Level (SVL) Circuit for Low-Power, High-Speed CMOS Circuits," ESSCIRC, 2002.
- [13] S.C.Omsakthi P.Dhanasekaran," AN efficient static RAM cell design for low power consumption," International Journal of Communications and Engineering Vol. 3, March2012.
- [14] A.Jagadeeswaran, Dr.C.N.Marimuthu," Power Optimization Techniques for Sequential Elements Using Pulse Triggered Flip-Flops with SVL Logic," IOSR Journal of VLSI and Signal Processing (IOSR-JVSP) Vol. 1, pp 31-36, Nov. - Dec. 2012
- [15] Kaijian Shi, David Howard "Sleep Transistor Design and Implementation – Simple Concepts Yet Challenges To Be Optimum" VLSI Design, Automation and Test, International Symposium, 2006.
- [16] K. Kawasaki et al., "A sub-us wake-up time power gating technique with bypass power line for rush current support," IEEE J. Solid-State Circuits, vol.44, pp.146–147, April 2009.
- [17] M. V. D. L. Varaprasad, Rohit Bapna, Manisha Pattanaik, "Performance Analysis of Low leakage 1-bit Nano-CMOS Based Full Adder Cells for Mobile Applications, " Proceedings of International Conference on VLSI Design & Communication Systems, pp.233-238, January 2010.
- [18] J. B. Kuo and J. H. Lou, "Low-Voltage CMOS VLSI Circuits", John Wiley: New York, 1999.

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