# Impact of Individual Charged Gate-Oxide Defects on the Entire $I_D$–$V_G$ Characteristic of Nanoscaled FETs

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***Abstract*—The measurement of the entire $I_D$–$V_G$ characteristic of a nanoscaled pMOSFET before and after the capture of a single elementary charge in a gate-oxide defect is demonstrated. The impact of a single trapped carrier on the device characteristics is compared with 3-D atomistic device simulations. The $I_D$–$V_G$ behavior is identified to depend on the location of the oxide defect with respect to the critical spot of the current percolation path in the channel.**

***Index Terms*—Nanoscale, negative bias temperature instability (NBTI), pMOSFET, reliability, time-dependent variability.**

## I. Introduction

With the ever decreasing device size, not only the number of dopant atoms but also the number of defects in each device reduces to numerable levels [1]. This results not only in increased time-zero (i.e., as-fabricated) variability but also in considerable time-dependent variability (i.e., reduced reliability) [2], [3]. This trend has recently lead to a shift in our perception of reliability: the "top-down" approach (deducing the microscopic mechanisms behind the *average* degradation in large devices) is being replaced in deeply scaled devices by the "bottom-up" approach, in which *the time-dependent variability is understood in terms of individual defects* [4]. We and others have recently shown that the properties of individual defects in the gate oxide can be observed and measured [5], [6]. Several groups have already foreseen an entire simulation flow based on this "atomistic" approach [7]–[9]. In particular, circuit simulations will require understanding of the impact of *individual charged defect*s on the entire FET current characteristics (compact models).

The latter issue is addressed in this letter for nanometer-scaled pMOSFETs by demonstrating the measurement of their $I_D$–$V_G$ curves *before and after the capture of a single hole*. Both increases and decreases of *apparent* mobility are observed for different defects on different devices and are matched well by atomistic 3-D device simulations.

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## II. Experimental Setup

Individual gate-oxide defect discharge events are visible in NBTI relaxation transients recorded on nanoscaled pFETs [Fig. 1(a)] [2], [4]–[6]. Due to the random dopant distribution in the devices [1], [3], the $\Delta V_{\rm th}$ steps caused by the individual defects are approximately exponentially distributed [Fig. 1(b)]. Single-charged defects causing gigantic $\Delta V_{\rm th}$, up to approximately ten times the simple electrostatic expectation (calculated by a charge sheet approximation $\eta_0 = q/C_{\rm ox} \approx$ 3.2 mV), are easily found [10]. A second set of 315 planar Si (SiON/Poly-Si, $EOT \approx 1.8$ nm) pMOSFETs, with $L_{\rm eff} =$ 35 nm and $W = 90$ nm, manifesting in total some 1200 active defects [the average number of observed defect per device was approximately four, as estimated from the preliminary characterization shown in Fig. 1(b)], was screened in order to select a smaller set complying with the following criteria: 1) The device shows a single dominant active trap; 2) the single trap $\Delta V_{\rm th}$ is large (i.e., *from the upper tail of the exponential distribution*); and 3) the characteristic trap-emission time is large enough ($> 1$ s) to allow a fast full $I_D$–$V_G$ measurement sweep before the hole is emitted. It is worth to emphasize that these criteria are solely chosen for the reason of experimental resolution and are otherwise unrelated to the observed effects. Fig. 1(a) shows the relaxation transients recorded on one such device. The subset of similarly behaving devices was then used to demonstrate the impact of *individual* charged gate-oxide defects on the entire nanoscaled device $I_D$–$V_G$, as presented in the next section.

## III. Results and Discussion

Fig. 2 shows the $I_D$–$V_G$ characteristic measured in the linear regime on one selected device [the same device as in Fig. 1(a)]

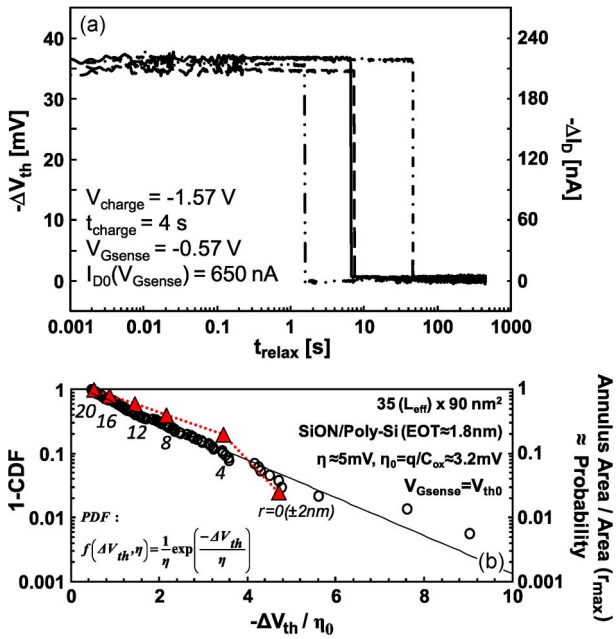


Fig. 1. (a) Typical set of relaxation traces recorded on one selected device from a larger 315-device set: One single dominant trap is observed, with $\Delta V_{\rm th} \approx 35$ mV and $\tau_e \sim 10$ s. Such device is suitable for the single trapped charge $I_D$–$V_G$ measurement (see Fig. 2). (b) Preliminary characterization of 32 randomly selected planar Si/SiON/Poly-Si pFETs ($EOT \approx 1.8$ nm) yields the distribution of single-carrier emission steps $\Delta V_{\rm th}$. The probability of finding a trap located at a given distance $r$ from the critical percolation spot (see Fig. 3 and discussion) is equal to the areas of the concentric annuli with radius $r$. Plotting this (triangles) probability versus the simulated $\Delta V_{\rm th}/\eta_0$ step heights (see Fig. 3) resembles remarkably well the measured distribution.

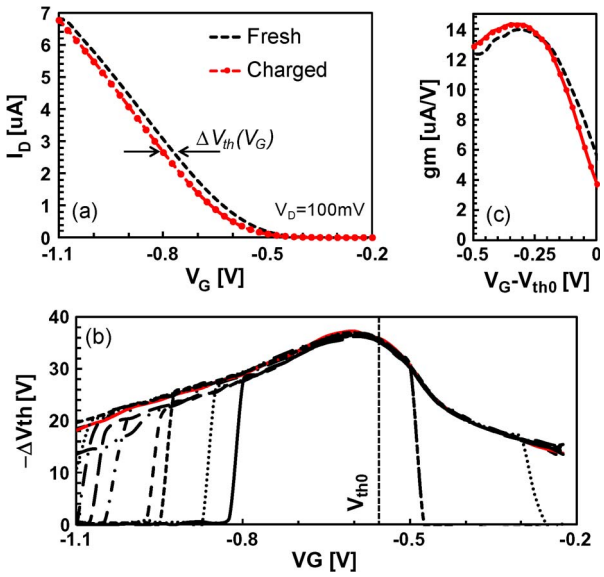


Fig. 2. (a) $I_D$–$V_G$ curves measured on one selected device (single trap $\Delta V_{\rm th} \approx 35$ mV, $\tau_e > 1$ s, see Fig. 1(a), *with the single oxide defect uncharged and charged*. (b) The shift of the characteristic can be described as a $V_G$-dependent $\Delta V_{\rm th}(V_G)$. This particular defect shows a maximum $\Delta V_{\rm th}(V_G)$ at $V_G$ above $V_{\rm th0}$. The measurement was repeated 12 times with excellent reproducibility (note that the single hole was emitted prematurely during some $I_D$–$V_G$ measurements). (c) Device transconductance ($g_m$) with the single oxide defect uncharged and charged. Assuming a simple model for the FET transconductance ($g_m \approx \mu C_{\rm ox} V_{\rm DS} W/L$), *apparent* mobility increase is observed.

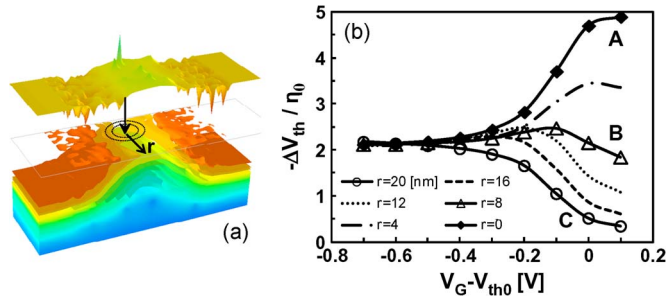


Fig. 3. (a) Atomistic 3-D device simulation showing the critical spot of the current percolation path. The simulations were performed for a *unique dopant configuration*, while the radial distance $r$ between the trap location and the critical spot was varied. (b) Different $\Delta V_{\rm th}(V_G)$ characteristics are expected as a function of $r$. Three notable cases are highlighted: (A) Charged trap located exactly at the critical spot of the channel current percolation path, (B) trap located 8 nm away, and (C) trap located 20 nm away. For different dopant configurations (i.e., different devices), different absolute magnitudes of the characteristics and different saturation values in ($\eta_0 = q/C_{\rm ox}$) are expected.

*with* and *without* the single trapped charge: The shift can be characterized as $\Delta V_{\rm th}$ [horizontal shift, Fig. 2(b)] or $\Delta I_D$ (vertical shift). As one can see, this particular trap causes a $\Delta V_{\rm th}$ which depends on the applied gate voltage, with the maximum impact at $V_G$ slightly above the threshold voltage of the fresh device ($V_{\rm th0}$). The reduced $\Delta V_{\rm th}$ at higher $V_G$ is correlated with the apparent mobility increase [Fig. 2(c)]. This is different from the behavior typically observed on larger area devices, where the $I_D$–$V_G$ curves before and after stress diverge due to the combination of parallel $V_{\rm th}$ shift (equal to $q\Delta N_T/C_{\rm ox}$, with $\Delta N_T$ representing the trapped charge) and mobility degradation. However, we note that each nanoscaled device is observed to behave differently, as discussed in the following.

From a *3-D atomistic device simulation* for a *unique dopant configuration* (Fig. 3) [11], different characteristics are expected as a function of the radial distance ($r$) between the oxide trap and the critical spot [i.e., the maximum confinement point, see Fig. 3(a)] of the channel current percolation path. A $\Delta V_{\rm th}(V_G)$ behavior with the maximum $\Delta V_{\rm th}$ at $V_G \approx V_{\rm th0}$ is ascribed to the single trap located directly above the critical spot (Fig. 3, group A), while a peak $\Delta V_{\rm th}$ at $|V_G| > |V_{\rm th0}|$ is ascribed to a trap at a medium $r$ (group B). Finally, an increasing $\Delta V_{\rm th}$ for increasing $|V_G|$ is expected for a trap located far from the critical spot (group C).

We propose that the overall behavior can be interpreted as follows: At low $V_G$, the current flow is highly localized through the critical percolation path, while at higher $V_G$ more conduction paths become available. A charged trap located directly above the critical spot (group A) suppresses the main contribution to the total current at low $V_G$ (large $\Delta V_{\rm th}$); however, its impact is reduced at higher $V_G$ when the relative weight of the percolation path on the total current flow is reduced. Conversely, a trap located away from the critical spot has a negligible effect on the overall current at low $V_G$ when the percolation path is the main contributor to the total current, while it causes a more significant impact when other conduction paths (eventually located closer to the charged trap) become available at higher $V_G$.

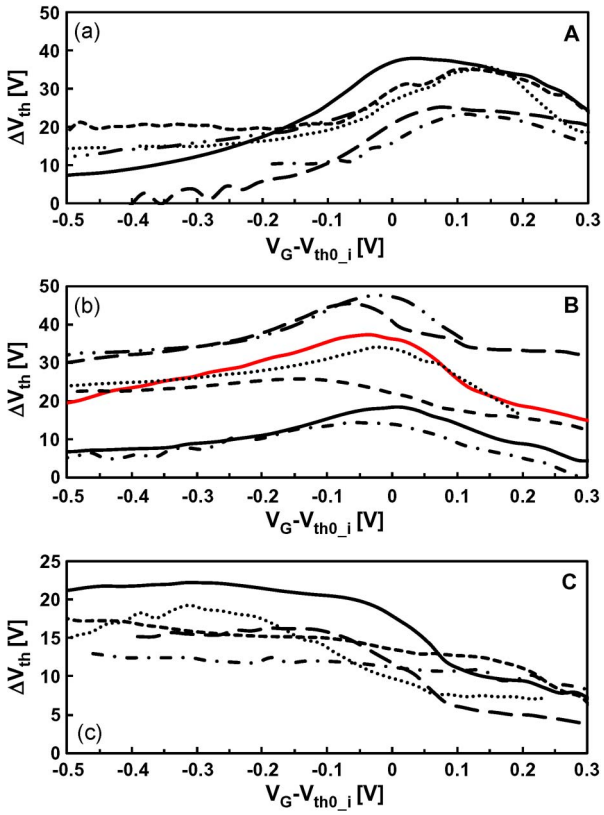


Fig. 4. $\Delta V_{\rm th}(V_G)$ characteristics measured on the set of selected nanoscaled devices, grouped by similar properties according to the simulated characteristics in Fig. 3 [the curve in red is the same as in Fig. 2, recorded on the selected device characterized in Fig. 1(a)]. The measured curves compare favorably with the (A–C) simulated behaviors, supporting the proposed interpretation. The additional variation in $\Delta V_{\rm th}$ magnitude within each group is ascribed to the variation in the confinement magnitude of the critical percolation spot for different dopant configurations on different devices.

The $\Delta V_{\rm th}(V_G)$ characteristics measured on the set of selected devices can be therefore grouped by similar properties, depending on $r$ (Fig. 4). Each group compares favorably with the device simulations, which correctly predict the *apparent mobility increase* [see Fig. 2(c)] after the capture of a single charge close to the critical spot (see groups A and B in Figs. 3 and 4: reduced $\Delta V_{\rm th}$ at high $V_G$). It is worth noting that, conversely to the simulation result for a unique dopant distribution, each measured curve shows a different saturation $\Delta V_{\rm th}$ at high $V_G$ as expected for different dopant configurations in different devices.

Further developing on this interpretation, the channel area can be divided into concentric annuli with increasing $r$, centered on the critical spot (see Fig. 3, each simulated behavior is assigned to an annulus equal to $r \pm 2$ nm). To the first approximation, the probability of finding a trap in a given annulus (i.e., the probability to have a trap with a given characteristic) is proportional to the area of each annulus. Within such a simplified picture, the probability of getting a given $\Delta V_{\rm th}/\eta_0$ value when sensing at $V_G \approx V_{\rm th0}$ already satisfactorily reproduces the observed exponential distribution (Fig. 1(b) triangles, constructed as a cutline of Fig. 3). In reality, the observed distribution is expected to be a weighted sum of distributions constructed from the simulations of multiple devices with different dopant configurations.

Finally, it is worth noticing that the $V_{\rm th}$ shifts, which are largest at $V_G$ around $V_{\rm th0}$, are strongly *reduced at higher* $|V_G|$'s (see group A in Fig. 3) where the FETs are typically operated. The resulting $\Delta V_{\rm th}$ distributions at higher sense $|V_G|$ are consequently expected to be narrower than the distributions customarily measured at $V_{G\rm sense} \approx V_{\rm th0}$ [Fig. 1(b)], hence relaxing the device lifetime distribution prediction at operating conditions [12].

## IV. Conclusion

In this letter, we have demonstrated the measurement of the impact of individual trapped charges on the entire nanoscale FET $I_D$–$V_G$. By comparing with 3-D atomistic device simulations, we have identified the $I_D$–$V_G$ behavior to depend on the location of the charged oxide defect w.r.t. the critical spot of the current percolation path in the channel. This interpretation predicts the probability of getting a given $\Delta V_{\rm th}$ when sensing at $V_G \approx V_{\rm th0}$ to appear exponentially distributed. These results should help in developing the next generation of atomistic circuit simulators.

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