Phase noise and jitter in digital electronics

Claudio E. Calosso* and Enrico Rubiola
*Division of Optics, INRIM, Torino, Italy
CNRS FEMTO-ST Institute, Besancon, France
Home page http://rubiola.org
E-mail: c.calosso@inrim.it and rubiola@femto-st.fr

I. Introduction

We tested a few digital integrated circuits of different technology and families with the ultimate target of understanding low phase noise frequency synthesis. Digital electronics features simplicity, reproducibility and cost, which is appealing in applications where the lower noise of analog circuits is not mandatory.

A side target of our work is the reduction of phase noise, first, by paralleling numerous gates, as in microwave and RF amplifiers, and second, to de-alias the output as we did in the Λ divider [Calosso.2013]. In the latter case, modern FPGAs make large pipeline possible because of the high toggling frequency (≈1 GHz).

II. Noise Model

We have identified two classes of phase noise behavior affecting complex digital devices, as suggested by Fig. 1. Some of the key concepts expanded underneath are already present in early articles, chiefly [Egan.1990] and [Phillips.1987]. Yet, the available literature is anterior to the devices we are interested in, and fits only partially.

A. The φ-type noise

The φ-type noise shows up as a random phase φ(t) not affected by the carrier frequency ν_0. This behavior results from a random fluctuation of the input threshold v(t) in the presence of a sinusoidal signal of peak amplitude V_p. Thus, $\varphi(t) = v(t)/V_p$. The fluctuation v(t) is generally not accessible, and even V_p may differ from the amplitude measured at the input pin. However, the signature of the pure φ-type noise is that the power spectral density $S\varphi(f)$ is independent of ν_0. For the sake of clarity we stress that $S\varphi(f)$ can be described by the usual polynomial law, while φ-type just means that $S\varphi(f)$ does not scale up/down with ν_0.

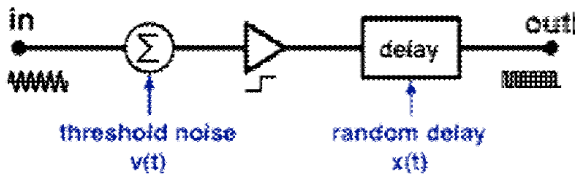

Fig. 1: Block diagram describing the two basic phase-noise types.

B. The x-type noise

The x-type noise is a fluctuation of the delay, independent of ν_0. This may be called jitter, or more appropriately phase time, defined as $x(t) = \varphi(t)/2\pi\nu_0$. See [Ferre-Pikal.2011] for further detail on x(t) and the other less-usual noise parameters. The x-type noise can be seen as a signal propagating along the complex path of the clock-distribution subsystem. Though the actual topology is often inaccessible to the designer, slew rate and noise bandwidth are determined by the internal structure, and independent of ν_0. The signature of the pure x-type noise is that the power spectral density $Sx(f)$ is independent of ν_0, thus $S\varphi(f)$ is proportional to ν_0^2.

C. Sampling and aliasing

The phase noise of a digital signal is sampled at each rising and falling edge, thus at the sampling frequency $2\nu_0$. By virtue of the Nyquist-Shannon theorem, sampling at $2\nu_0$ sets the phase-noise bandwidth B_φ equal to ν_0. Since the analog noise bandwidth it always holds that $\nu_0 < B_N$ (noise bandwidth of the circuit), aliasing folds B_N to B_φ, and increases the phase noise. High B_N/B_φ ratio (example, work at 5 MHz on 1-GHz device) results in unexpectedly high phase noise.

Anyhow, for a given technology (given B_N), aliasing introduces a proportionality factor $1/\nu_0$ to both $Sx(f)$ and $S\varphi(f)$. In turn, the two noise types split into four sub-types listed in Table I. The question of aliasing in the presence of non-white phase noise is kept for later.

D. Input chatter

At the high clock frequency used in modern digital electronics, often the input is a sinusoid that is converted into a square wave by the input stage. In some conditions described underneath, the sin-to-square conversion process is affected by chatter. Multiple random crossings occurs at the threshold, instead of one.

The slew rate SR of a pure sinusoid $v(t) = V_0\cos(2\pi\nu_0 t)$ is equal to $2\pi\,\nu_0 V_0$ The slew rate associated to random noise of power spectral density $Sv(f)$ is calculated by integrating all the spectral components in the system bandwidth B, each with a weight factor of $2\pi f$. Thus

$$\langle SR^2 \rangle = 4\pi^2 \int^B f^2 Sv(f)\, df$$

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TAB I: BASIC NOISE TYPES

NOISE TYPE	DEPENDENCE ON ν_0		NOTE
	$S\varphi(f)$	$Sx(f)$	
Pure x-type	ν_0^2	C vs. ν_0	Typical of $1/f$ time jitter
Aliased x-type	ν_0	$1/\nu_0$	Seldom encountered
Pure φ-type	C vs. ν_0	$1/\nu_0^2$	Typical of $1/f$ time jitter
Aliased φ-type	$1/\nu_0$	$1/\nu_0^3$	White phase noise

TAB II: DIGITAL CIRCUITS UNDER TEST

Brand	Device	Node size	Type
Altera	MAX 3000	300 nm	CPLD
Altera	MAX V	180 nm	CPLD
Altera	Cyclone II	90 nm	FPGA
Altera	Cyclone III	65 nm	FPGA
Xilinx	Zynq	28 nm	FPGA / ARM

$$= (4\pi^2/3)\,\sigma^2\,B$$

The system bandwidth B is of the order of three times the maximum toggling frequency. With a narrower bandwidth, the analog signal could not be converted into a square wave. Chatter occurs when the SR associated to noise exceeds the pure-signal SR at the threshold, so that the slope of the overall signal (sinusoid plus noise) can change sign unpredictably. The chatter threshold is given by the equation

$$\nu_0^2 = (Sv\,B^3) / (3\,V_0^2)$$

A problem with high-speed electronics is that the noise bandwidth B is so wide that chatter may occur in unexpected conditions. For example, a device toggling at 1 GHz (3 GHz noise bandwidth), having an equivalent input noise of 10 nV/√Hz and driven at 400 mV_{pp}, chatters at $\nu_0 \le 4.8$ MHz.

In all our experiments, the digital devices are operated out of the chatter region.

III. EXPERIMENTAL METHOD

Checking on the noise model, we measured the devices listed in Table II with a Symmetricom 5125A test set [Microsemi]. The DUT and the test set are driven by the same source, so its noise cancels. Nonetheless we used a high purity synthesizer. We collected noise data scanning the input frequency and changing the internal configuration (HDL program).

IV. SOME RESULTS

A. Cyclone III FPGA

Figure 1 shows an example of phase noise measured on an Altera Cyclone III FPGA used as a clock buffer. The input clock is a 10 dBm sinusoidal signal, and the output is a square wave at the same frequency.

In the central region, between 0.1 Hz and 10^2–10^3 Hz (depending on ν_0), the noise fits well the $1/f$ law. This region tells us about the general flicker behavior of the device. At $\nu_0 \ge 50$ MHz, with a smooth transition at 25–50 MHz, $S\varphi(f)$ follows precisely the ν_0^2 law (+6 dB per factor-of-2). This is the signature of the pure x-type noise. Of course, we expect that at high ν_0 the input SR is high enough to make the threshold noise negligible. In this condition the x-type noise of the clock distribution prevails.

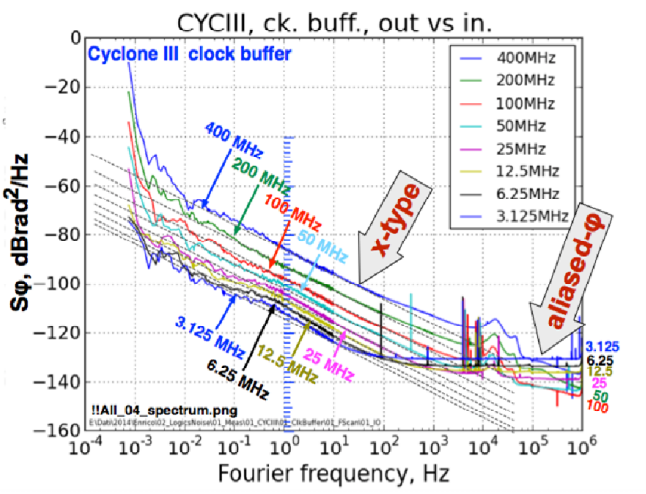
For $\nu_0 \le 25$ MHz, and still in the flicker region, $S\varphi(f)$ tends to the ν_0 law (+3 dB per factor-of-2). In principle, this would be the signature of aliasing in the x-type noise. However, this conclusion is incompatible with the rule that aliasing has a negligible effect on flicker. The explanation is still unknown. We are investigating on an alias-like phenomenon where the noise sidebands of the numerous harmonics $n\nu_0$ are folded down to ν_0.

Another unexplained effect is the bump at low Fourier frequency, between 0.1 Hz and 10 Hz, which shows up only at the lowest carrier frequencies ($\nu_0 \le 12.5$ MHz).

At low ν_0 (3.125…12.5 MHz), white noise shows up on the right hand of Fig. 1, with $1/\nu_0$ law (–3 dB per factor-of-2). This is the signature of φ-type noise, due to the low slew rate at the input, in the presence of aliasing. Since the additive noise integrated over the system bandwidth is not affected by ν_0, higher ν_0, results in higher $S\varphi(f)$. From a different standpoint, this is an outcome of the Parseval theorem, which states that the power can be obtained bi integrating the spectrum, or from the time domain, and the result is the same.

In synthesis, this experiment enables the to describe the buffer implemented in a Cyclone III using only two parameters. First, this device exhibits pure x-type noise in the flicker region for a wide range of carrier frequency and in a few decades of Fourier frequency. The flicker in $Sx(f)$ is of

Fig. 2: Phase noise of the Cyclone III FPGA used as a clock buffer.



22 fs/√Hz at 1 Hz. Conversely, at low carrier frequency

alias results in φ-type noise, described by $S\varphi(f) = k^2/\nu_0$. The parameter k can be extracted from Fig. 1. For example, at 12.5 MHz, the white phase noise is of 3.2×10^{-14} rad^2/Hz, thus k = 630 µrad. Assuming that the noise bandwidth is of 3 GHz (three times the maximum toggle frequency), and a peak input voltage of 1 V, after Section II we get a fluctuation of 10 nV/√Hz in the analog threshold.

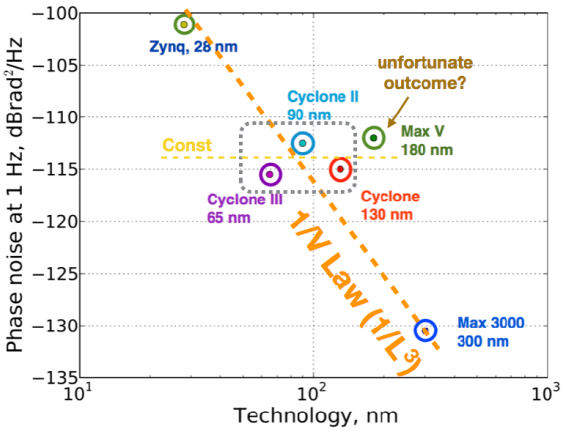
B. Thermal effects

It is well known that the charge/discharge cycle if the gate capacitance results in energy loss $E = CV^2$. Consequently, the dissipated power is proportional to ν_0, and of course also to the number of gates that switch. As a further consequence, a change in the toggle frequency affects the chip temperature via the junction-ambient thermal resistance, and also originates a thermal transient. A moderate thermal insulation was used to prevent the fluctuations of the air flow from spoiling the measured $S\varphi(f)$ at low Fourier frequencies. We had to respect a full one-hour delay after each frequency change for the results shown in Fig. 1 to be free from thermal transients.

C. Preliminary conclusions

A few experiments have been done, shortly summarized underneath. Others are in progress. The main point is shown in Fig. 3. The lowest phase noise is observed in elderly MAX 3000 CPLDs, in 300-nm technology. Oppositely, the highest phase noise is observed in the highest-density device we tested, which is the 28-nm, the FPGA inside a Zynq chip. This rather general behavior is only partially a surprise because the node size is clearly related to the volume of the active region, where gain and threshold decision take place. In microwave and RF amplifiers, it is well known that lower phase noise is achieved with larger size or by paralleling several devices [Boudot.2012, Phillips.1987, Rubiola.2008]. On the other hand, the short gate delay associated with high density and high speed does not go with

Fig. 3: Phase noise of the Cyclone III FPGA used as a clock buffer.



proportionally small jitter. Connecting in parallel numerous small-size gates works fairly with white noise, less with flicker. Similarly, the larger pipeline in the Λ scheme could not improve on a smaller pipeline with larger-size gates. In the end, the phase noise of our 300-nm Λ divider [Calosso.2013] is still unsurpassed.

V. Final Remarks

High-density electronics deserves to be studied now because it is inevitable in future design. Miniaturization and low power are per se interesting features. High speed enables to process high frequencies, while lower dissipation may help in achieving high stability and small interference to other parts of the system. The comparatively small complexity of frequency synthesis may even fit in the unused space of a complex system.

Our work is still in progress, and we will release more at the meeting.

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