Simulation of Error Control Schemes for Wireless and Satellite ATM

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Abstract

This paper summarizes the results of a set of simulations of error control schemes for transmission of ATM cells in Wireless and Satellite ATM networks. For Wireless ATM networks, we consider a scheme which incorporates separate FECs for ATM cell header and payload. This scheme is an effective scheme and achieves a trade-off between coding rate and bandwidth. A concatenated FEC scheme (RSCCC) is considered for Satellite ATM networks.

1 INTRODUCTION

ATM and wireless personal communication networks have emerged as the front runners in the telecommunications technologies individually. The increased dependence on networking for business, recreation and communications, the growing demand for multimedia applications together with a human desire for mobility and freedom from office-only or home-only computing constraints makes a strong argument for wireless integrated networks. Hence, Wireless ATM has gained importance over the past few years to fulfill the requirements [12].

On the other hand, there are several application scenarios that are motivating factors for Satellite ATM [5]. Some of the application scenarios where Satellite ATM has an edge over other technologies are: geographically distributed computing, distance learning and next-generation education, secure broadband communications, multimedia and multi-service applications, mobility in wireless ATM networks, etc. In these scenarios, satellite communications can solve the distance factor and ATM can solve the requirements of QoS guarantees.

Research on various aspects, design issues and limitations of Wireless ATM and Satellite ATM are going on around the globe extensively. One of the issues that have to be addressed for these systems is that of error control for the ATM cells. The attempt of ATM over wireless links and satellite links immediately identifies a fundamental difference in the way that ATM will be used. That is ATM cells will be subjected to transmission links that are unreliable. These radio transmission links are characterized by presence of fading and interference effects in addition to the additive white gaussian noise due to thermal factors. Because of these effects, these links is characterized by bustier error patterns, and a higher and time-varying error rate when compared with the fiber-based network for which ATM was designed. These links provide error rates typically around 10^{-2} and the fiber-based links provides error rates typically above 10^{-8}. As a result, such high difference leads to requirement of error control schemes to insulate the ATM network layers from wireless channel impairments.

This paper presents the simulation results of two such error control schemes presented in [1, 2] one each for Satellite ATM and Wireless ATM. The rest of the paper is organized as follows. In section 2, we present the error control scheme for Wireless ATM and its analytical performance. Section 3 presents the error control scheme for Satellite ATM and its analytical performance. Finally, section 4 presents the simulation methodologies used and the simulation results of these schemes.

2 ERROR CONTROL - WIRELESS ATM

FEC is used to improve BER performance and is designed with consideration of various parameters like BER and cell-loss probability. A straight forward FEC scheme would be to add parity bits calculated for the entire ATM cell (53 bytes including HEC) to it. In such scenario, if the FEC code is designed to achieve a low cell loss probability the coding rate decreases and hence the bandwidth requirement goes up. Where as, if the FEC code is designed with in rate and bandwidth constraints, it may not give the required CLP performance. Hence a scheme as proposed in [1] is considered here. This is an effective FEC scheme and achieves a trade-off between both the factors. The scheme is to use two FEC codes, one for the header one for the payload as shown in Figure 1. The header code has powerful coding gain and the payload code has a high coding rate. The coded cell is defined as a wireless ATM cell in which HEC is removed and FEC is added. Before creating a coded cell, a single bit error is corrected and cells with multiple bit errors are discarded. After this, HEC is removed. When errors after the header FEC are detected, the cells are

discarded in the radio section. After the wireless section a new HEC is generated for the wired section.

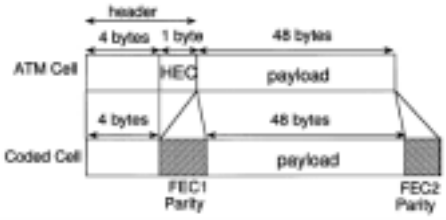

Figure 1 ATM Cell and Coded Cell Format

ATM cell payload consists of 384 bits. The FEC for this payload can be implemented in the following way. The 384 bits can be split into two blocks of 192 bits each and these blocks can be encoded separately. The codes for encoding 192 bits of block can be obtained from shortening the BCH code with original length of 255. Table 1 summarizes the details for the possible codes for the payload blocks. Note that the better the error correction capability, the coding rate decreases.

One of the parameter of our interest is to find the BER after FEC. This parameter BER after FEC (P_a) in case of a t-bit error correction (n, k) code is given by:

$$P_a = \sum_{i=t+1}^{n} nCi\,(1-p)^{n-i}\,p^i\left(\frac{i}{n}\right),$$

where p is the BER before FEC. From this equation, $nCi\,(1-p)^{n-i}\,p^i$ indicates the probability of i errors occurring in the n bits and (i/n) indicates the BER for i errors. If the number of errors is less than equal to t, then are those are corrected, hence they do not contribute to the BER after FEC. Hence for finding BER after FEC, the average of BERs is taken for all number of errors in interval [t+1, n]. Figure 2 shows the relative performance of these codes.

After considering the FEC codes for the payload, now the task remains to analyze the FEC codes for the header bits. The header consists of 32 bits after removal of HEC. Shortened BCH codes of original length 63 are used to encode these 32 bits of the ATM header. Table 2 shows the details of these FEC codes and their correction abilities.

Error Correction (t)	Shortened Code (n,k)	Original Code (n,k)	Shortened by (bits)	Coding Rate
1	(200, 192)	(255, 247)	55	0.96
2	(208, 192)	(255, 239)	47	0.923
3	(216, 192)	(255, 231)	39	0.889
4	(224, 192)	(255, 223)	31	0.857
5	(232, 192)	(255, 215)	23	0.828

Table 1 Candidate Codes for Payload Block of 192 bits

The cell-loss probability (CLP) for a t-error correcting (n, k) code is given by:

Error Correction (t)	Shortened Code (n,k)	Original Code (n,k)	Shortened by (bits)	Coding Rate
1	(38, 32)	(63, 57)	25	0.842
2	(44, 32)	(63, 51)	19	0.727
3	(50, 32)	(63, 45)	13	0.64
4	(56, 32)	(63, 39)	7	0.571
5	(62, 32)	(63, 33)	1	0.516

Table 2 Candidate Codes for Header Block of 32 bits

$$CLP = \sum_{i=t+1}^{n} nCi\,(1-p)^{n-i}\,p^i$$

where p is BER before FEC. If there are more than t errors in the header, then the cell is considered to be lost. The CLP equation is derived based on that. Figure 3 shows the cell loss probability vs. payload BER graph.

Creating a balanced design for the payload BER and cell-loss probability which is the same as the HEC for the wired ATM is extremely efficient from the viewpoints of coding gain and coding rate. Figure 3 shows the two bits higher ability of header FEC (four-bit error correction) than the payload FEC (double bit error correction) is the most similar in performance as HEC. This case was use for simulation and results are presented in section 4. Other cases as suggested in [1] with two bits higher ability header FEC give similar performance as of the case chosen here.

3 ERROR CONTROL - SATELLITE ATM

We consider a concatenated FEC scheme as proposed in [2] for error control in satellite ATM networks. This concatenated code consists of Reed-Solomon outer code and convolutional inner code (RSCCC). Other than concatenated codes, turbo codes are also emerging rapidly and are being widely tested for such satellite applications.

This scheme is envisioned for a scenario of broadband satellite providing Internet service, video-on-demand service, etc. In such scenario, a two-way satellite service is required. The downlink transmission for the user may be continuous stream, but the uplink transmission for the individual user terminal are typically very short and bursty (a single or few packets at a time). These bursty short duration transmissions on the uplink are nature of sending requests when establishing connections. Frequently such uplink transmissions need to be heavily encoded to achieve a suitable BER.

Though the performance of RSCCC is inferior to the performance of Turbo codes, they still have significant application in such scenarios. Moreover, concatenated schemes such as RSCCC when modified using Rate-Compatible Punctured Convolutional codes

(RCPCC), are applicable in providing adaptive error control schemes. Adaptive error control schemes based on such methods are discussed in [8, 9].

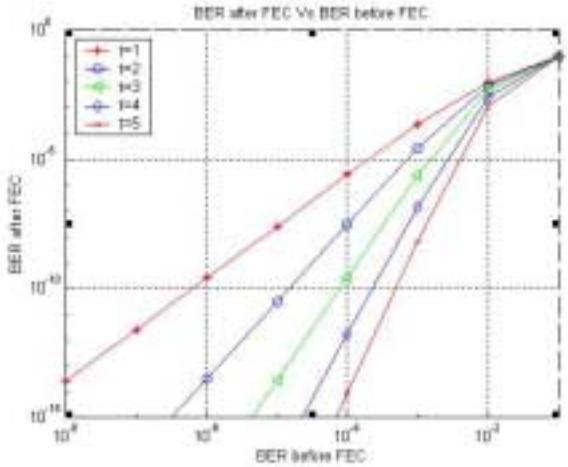

Figure 2 Theoretical Payload FEC Performances

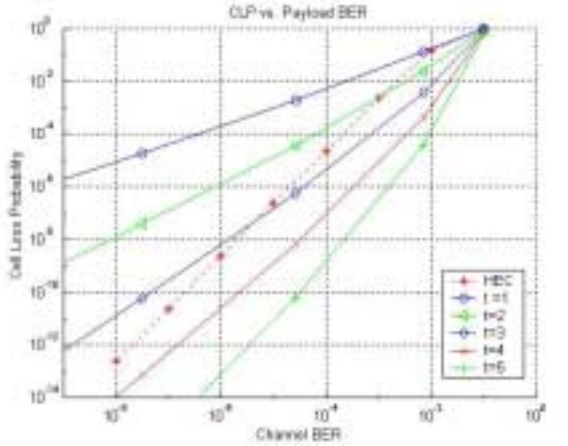

Figure 3 Theoretical Wireless FEC Performance

Hence, RSCCC method is considered here. The primary objective here would be to determine the Eb/No requirement for the uplink transmissions packets of four ATM cells by a small user terminal. The analytical performance and simulated performance using both hard and soft decision decoding of convolutional codes is presented.

For transmission of four ATM cell requires the concatenated coding scheme to handle 1694 information bits/ ATM bits (4 x 53 x 8 = 1696). The most common RS code used for satellite communication applications are of block length 255 bytes (n) and information bytes of 239 (k). The word "byte" was used because the symbol length for this RS code is 8 bits, that is the code is constructer over a Galios Field of 2^8 or referred to as GF(2^8). The 239 information bytes correspond to 1912 bits. It is thus straightforward to shorten the code by 27 bytes to obtain a (228, 212) RS code. This code can then be concatenated with the industry standard rate ½, k = 7 (constraint length) convolutional code. Additionally, since each "frame" of ATM cells is independent, the convolutional code must be forced into a known end state, resulting in an additional 14 bits on the channel. Thus total number of channel bits / encoded bits is 3662 channel bits (228 x 8 x 2 + 14). The over code rate is 1696/3662 = 0.463. Figure 3.4 shows the block diagram describing concatenated FEC scheme for satellite ATM. In this case the symbol interleaver block cannot be used since there is only one RS code word to carry the whole block.

3.1 Analytical Performance [3, 6, 8]

The constraint length of convolutional code is 7; hence the most frequently occurring error bursts at the output of the viterbi decoder will have length 7 or 8. Thus, the 8-bit symbols of the RS code will handle these bursts as single symbol error. The minimum distance of (n,k) RS code is n-k+1 (code property). The RS code can correct i symbols errors and j symbol erasures at the same time as long as (2i + j) ≤ (n-k) is satisfied. The symbol error rate for the codeword of n symbols at the output of the RS decoder that is capable of correcting up to t symbol errors is given as:

$$P_S = \sum_{2i+j>2t}^{i+j=n} \binom{n}{i,j} e^i s^j (1-e-s)^{n-i-j}, \quad i,j \geq 0,1,2,\ldots \tag{1}$$

where e denotes the symbol error rate and s the symbol erasure rate before the RS decoder. For the concatenated coding scheme, the RS decoder processes the output stream of the viterbi decoder. In this case, there are no symbol erasures (s = 0) and further the symbol error rate at the input of the RS decoder is same as the symbol error rate at the viterbi decoder output, $\mathbf{P_{sVit}}$. With ideal symbol interleaving between the viterbi decoder and the RS decoder the equation 3.1 can be simplified as:

$$P_S = \sum_{i=t+1}^{n} \binom{n}{i} P_{sVit}{}^i (1-P_{sVit})^{n-i} \tag{2}$$

when i (more than t) symbol errors occur, the RS decoder cannot correct them due to a decoder failure. Therefore, the symbol error rate after the RS decoder can be estimated by noting that i out of n symbols in an RS codeword will be delivered in error on a decoder failure. Furthermore, if about half of 8 bits in an errored RS symbol are assumed to be in error, then the probability of bit error at the RS decoder output is approximated as:

$$P_b \approx \frac{1}{2} \sum_{i=t+1}^{n} \frac{i}{n} \binom{n}{i} P_{sVit}{}^i (1-P_{sVit})^{n-i} \tag{3}$$

Since one RS symbol consists of 8 bits from the viterbi decoder the symbol error rate at the viterbi decoder output, P_{sVit} as,

$$P_{sVit} < 8P_{bVit} \quad (4)$$

The derivation of P_{bVit} for viterbi output as given in many texts including [6] is very complex and lengthy process. The final equation depends on the structure of the code. For this case of constraint length = 7 will be very difficult to fully evaluate analytically. Hence, the simulated performance of this code will be used to evaluate the analytical performance of the RSCCC. The simulated performance is shown in Table 3 (only values that falls in the performed simulation range). These values correspond to soft-decision viterbi decoding.

E_b / N_o (dB)	BER
2.0	9.0e-3
2.2	6.5e-3
2.4	4.0e-3
2.6	2.5e-3
2.8	1.5e-3
3.0	8.5e-4
3.2	4.75e-4

Table 3 Simulated Convolutional Code Performance

Using equations 3, 4 and Table 3 the theoretical plot for the concatenated code performance is shown in Figure 4. The graph also shows the plot of uncoded BPSK BER plot for comparison. The estimated Eb/ No required for obtaining a BER of 1e-10 is 3.5 dB using this concatenated coding scheme. This is a small value as compared to 13 dB required by the BPSK system.

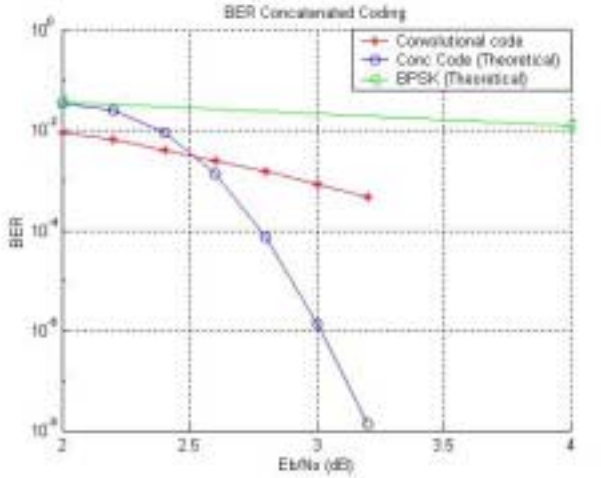

Figure 4 Theoretical Performance of Concatenated Code

4 SIMULATION AND RESULTS

The simulation of wireless ATM FEC performance is done using MATLAB and the simulation of satellite ATM concatenated FEC performance is done in Cadence's Signal Processing Work system (SPW). Both the simulations are done for an additive white gaussian noise channel (AWGN).

In MATLAB simulation, Monte-Carlo (MC) simulation methodology has been used. SPW inherently uses this methodology. This methodology is conventional in simulation of digital communication systems and offer generality and helps in modeling complex systems easily. However, for simulation that depends on occurrence of rare events, like in our case a very low BER (>1e-8), this technique requires a very large number of simulation runs. For example, it is shown that for the desired error rate P_e, MC requires at least $100/P_e$ trials to estimate a BER with a relative position of 10% [10], where the relative precision is defined as the standard deviation of the BER estimator divided by the actual BER. For a BER of 10^{-10} the minimum number of simulation runs is in excess of 10^{12} trials, which makes this approach infeasible for such low estimation of BERs. For such cases, rare event simulation methodologies like importance sampling (IS), error event simulation (EES), etc, should be used. The use of such methods would require in depth study of these methods and careful modeling our systems to get accurate results for high BERs. Hence simulation using such schemes would be very difficult. Due to the above reasons, we use Monte-Carlo simulation approach for our problems and use the simulation for reasonable BER estimation (~ 10^{-5}).

The following sub-sections explain the simulation approach used and also presents the results obtained using those simulations.

4.1 Wireless ATM FEC Performance

There are two primary tasks that are to be performed to estimate the wireless ATM FEC performance. First task is to simulate the payload FEC performance then the second task is to simulate the header FEC performance based on the payload FEC performance.

MATLAB offers several functions in their communication libraries that perform encoding and decoding using several methods. The main task in this simulation was to develop a system/ program using these functions that would run a certain number of simulation trials (as input by user) and for a given value of channel BER (as input by user) and provide cell loss probability (CLP) as output. The white gaussian noise generator is built using the box-muller method. The gaussian noise generator was tested for performance by building a simple BPSK system and simulated the BER performance. If the simulated BER performance matches the theoretical performance then the noise generator is working perfectly.

The determination of cell-loss was done based on two modes of operation (detection mode and

correction mode) of header error control (HEC). Each single simulation run indicates the complete transmission and reception of one ATM cell and also keeps track of the mode of operation and the number of cells lost.

For payload FEC performance is indicated by the plot of BER after FEC Vs. BER before FEC. This simulation has same input parameters as explained earlier, that is the number of simulation runs and the channel BER (BER before FEC). The output parameter is BER after FEC and not CLP. The payload blocks are divided into two blocks and are encoded using the FEC codes as explained earlier. The encoded bits is passed through the BPSK channel to the decoder. After decoding the BER is estimated by comparison with the original message. The simulation is done for all the FEC codes as mentioned in Table 1. The results of this simulation are shown in Figure 5. The maximum simulated performance was to get a BER after FEC of 1e-5. The plots for simulated performance follow closely for the plots for the theoretical performance as shown in Figure 5. The plots also match those presented in [1].

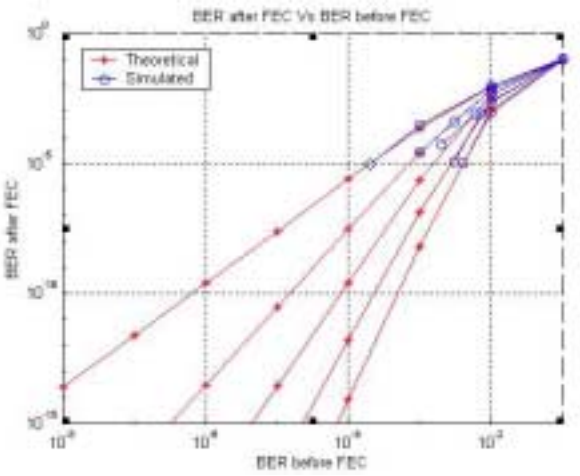

Figure 5 Simulated Payload FEC Performances

The header FEC performance with respect to the payload BER indicates the performance of Wireless FEC scheme. The simulation for this case is similar to the ATM HEC performance. Here both header and payload blocks are encoded using FEC codes. After decoding the cell-loss probability and payload BER are given as output of this simulation. Figure 6 shows the simulated performance of the ATM header FEC performance with respect to payload BER. The plot shows the performance for simulated case matches the performance for the theoretical case and also with the plots presented in [1].

4.2 Satellite ATM Concatenated FEC Performance

The performance simulation of the concatenated FEC scheme is done in Signal Processing Worksystem (SPW). SPW provides tools that you can use to interactively capture, simulate, test, and implement a broad range of digital signal processing (DSP) designs.

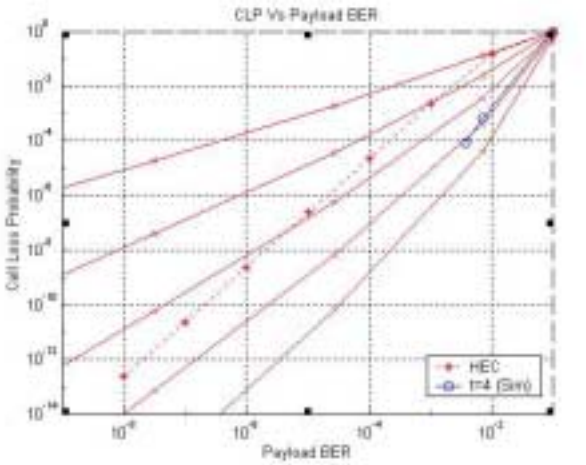

Figure 6 Simulated Wireless FEC Performance

The simulation is done for two different decoding methods of convolutional code: hard-decision decoding and soft-decision decoding. In hard-decision decoding the received signal is quantized into binary data (2-level quantization), that is zeros and ones. This binary data is used for decoding by the viterbi decoder. In this method much of the channel information is lost. In soft-decision decoding high level of quantization is used. In this simulation, 8-level quantization is used. Soft-decision decoding provides much better results than hard-decision decoding. The performance graphs plotted later will show at least 2 dB difference between the soft and hard-decision decoding methods.

The calculation of soft decision thresholds, which are input parameters for the metric input file for the viterbi soft decision decoder is based on [7] and is used by Advanced Hardware Architectures in their decoding chip implementations.

The other important parameter that is to be calculated for both the cases is the noise power (variance parameter of noise generator block) for different Eb/No values. The noise power values are calculated in the desired range for simulation, i.e. minimum noise power value will yield a BER of approx. 10 E -5.

Figure 7 shows the concatenated FEC scheme results. The theoretical results are different than the simulated results because the theoretical formula is computed using binomial distribution formula and

assumes that an infinite size interleaver (ideal interleaver) is used, whereas in simulation no interleaver was used. No interleaving is possible between the inner code and outer code in this system because there is only one Reed-Solomon codeword used to carry the whole block. However, the results as shown in Figure 7 matches perfectly with the results published in [2]. With this kind of scheme a BER of 1e-10 can be achieved by an Eb/ No in the range of 4.0 to 4.3 dB [2]. This requirement is quite low as compared to the 14 dB requirement by a simple BPSK system to achieve same BER. The difference in Eb/No for the hard-decision case and soft-decision case for the same BER is approximately equal to 2 dB.

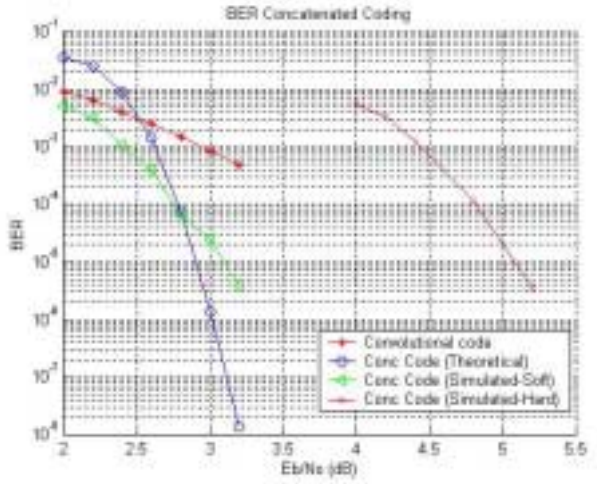

Figure 7 Simulated Performance of Concatenated Code

5 CONCLUSION

This paper analyzes the performance of the proposed FEC schemes for wireless and satellite ATM networks. The FEC scheme of using two different codes for the header and payload in wireless ATM gives us a trade-off between CLP and coding rate factors. The header code with a high coding gain and the payload code with high coding rate perform as a better combination. A concatenated code consists of Reed-Solomon outer code and convolutional inner code (RSCCC) is analyzed as a FEC scheme for satellite ATM. This scheme is to be used for bursty short duration transmissions (single or few cells) on the uplink, such as sending requests when establishing connections. RSCCC codes provide good coding gain to obtain the required BER. These schemes when used in adaptive strategy for FEC will give very high performance gains. Turbo codes are also emerging as powerful codes in satellite ATM networks.

6 REFERENCES

[1] S. Aikawa, Y. Motoyama and M. Umehira, "Error Correction and Error Detection Techniques for Wireless ATM Systems," Wireless Networks Vol. 3 Issue 4, September 1997, p285-290

[2] M. Vanderaar, R. Gedney, and E. Hewitt, "Comparitive Performance of Turbo Product Codes and Reed-Solomon Convolutional Concatenated Codes for ATM Cell Transmission," Fifth Ka Band Utilization Conf.: Proc., October 1999, p409-416.

[3] S. Lin and D. J. Costello, "Error Control Coding: Fundamentals and Applications," Prentice-Hall, 1983.

[4] U. Black, "ATM: Foundation for Broadband Networks," Prentice Hall 1995.

[5] I. Akyildiz and S. Jeong, "Satellite ATM Networks: A Survey," IEEE Communications Magazine, July 1997, p30- p43.

[6] S. B. Wicker, "Error Control Systems for Digital Communication and Storage," Prentice Hall, 1995, p313.

[7] AHA Application Note, "Soft Decision Thresholds and Effects of Viterbi Performance," Advanced Hardware Architectures, Document no ANRS07-0795, available at www.aha.com.

[8] I. Joe, "An Adaptive Hybrid ARQ Scheme with Concatenated FEC Codes for Wireless ATM," Wireless Networks Vol. 6 Issue 3, July 2000, p211-219

[9] S. Cho, "Adaptive Error Control for Hybrid (Satellite-Terrestrial) Networks," IEEE Wireless Communications and Networks Conference (WCNC'99), 1999.

[10] J. S. Sadowsky and J. A. Bucklew, "On Large Deviations Theory and Asmptotically Efficient Monte Carlo Simulation," IEEE Transcations on Information Theory, vol 36, No. 3, 1990, pp 579-588.

[12] D. Raychaudhuri and N.D.Wilson, "ATM-based transport architecture for multiservices wireless personal communication networks," IEEE Journal on Selected Areas in Communications 12(8), October 1994, p1401–1414.