The Scalable Modeling of Multi-layer Embedded Capacitor based on LTCC Substrate

Jongbae Park, *Albert Chee W. Lu, *Wei Fan, *Lai L. Wai, *Kai M Chua, Yujeong Shim, and Joungho Kim
Terahertz Interconnection and Package Laboratory, Department of Electrical Engineering and Computer Science,
Korea Advanced Institute of Science and Technology, 373-1 Guseong-dong, Yuseong-gu, Daejon 305-701, Korea
Tel: +82-42-869-9867, Fax: +82-42-869-8058, E-mail: pjb77@eeinfo.kaist.ac.kr, Homepage: http://tera.kaist.ac.kr
*Singapore Institute of Manufacturing Technology, 71 Nanyang Drive, Singapore 638075

Abstract

Low temperature co-fired ceramic (LTCC) technology is the preferred platform for integrating multi-layer capacitors due to excellent high frequency performance and low-loss dielectric properties. This letter describes a novel approach to perform modeling of multi-layer capacitors in LTCC technology. This hybrid approach combines both analytical modeling and numerical modeling to provide a scalable circuit model predicting the self-resonance frequency of the multiple dielectric and electrode layers. Good correlation between the simulation results and network analyzer measurements has been also achieved.

1. Introduction

Recently, as an alternative solution for the low cost and highly integrated system with multiple functionalities, System-on-Package (SoP) technology has emerged [1] [2]. The SoP brings multiple semiconductor dies of various semiconductor processes and materials, and passive devices such as termination resistors, decoupling capacitors, inductors, waveguide, filters, and antennas into a three-dimensional package, to create highly integrated products with optimized cost, size and performance. Markets for the SoP solution include wireless communication, networking, computing, and sensor and storage system applications. To integrate these multiple dies and passive devices into a tiny 3-D SoP, adoption of high-density multilayer substrate design is a common approach to mount the multiple dies on a substrate with the embedded passives, which are laterally or vertically integrated onto the package substrate. Low temperature co-fired ceramic (LTCC) technology is the preferred platform for integrating multi-layer passives due to excellent high frequency performance and low-loss dielectric properties [3]. To achieve efficient design of LTCC-based SoP, accurate modeling for embedded passives is an important component of the design flow [4] [5].

In this paper, we propose a scalable modeling method for multi-layer embedded capacitor. Even if many papers have published to accurately model capacitors and their model are quite accurate, none of them has considered the scalability of the model for the multi-layer capacitor [6-12]. In LTCC technology, multi-layer capacitor integration is a key process and there is a strong need for scalable modeling. Thus the scalability of multi-layer capacitor has to be taken into account for the efficient design of LTCC-based SoP. In this paper, we introduce the scalable model of multi-layer capacitor which uses the interdigitated via topologies. The scalable model was verified through 3-D HFSS simulation and measurement for the 14-pairs capacitor up to 20GHz. The results for the proposed scalable model show good correlation with the simulated and measured data. Based on the model, the library for embedded capacitor design is discussed.

2. Proposed Scalable Model

Two-port multi-layer embedded capacitor based on LTCC substrate is shown in Figure. 1. The capacitor uses an interdigitated via distribution with a total of three pairs. The interdigitated distribution significantly increases the mutual inductance between the pairs, resulting in the reduced effective loop inductance and the increased self-resonance frequency of the capacitor.

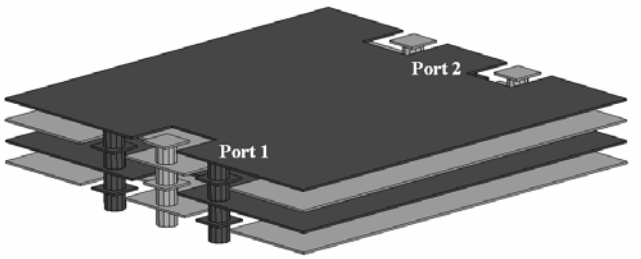

Figure 1. Two-port multi-layer embedded capacitor based on LTCC substrate with N =3

For scalable modeling of the multi-layer embedded capacitor, we use hybrid approach, which combines both analytical modeling and numerical modeling to provide a scalable circuit model for multiple dielectric and electrode layers. The modeling procedure can be simply explained as 3-steps. First, obtain the equivalent circuit model, which consists of plane capacitance, plane inductance, via inductance, and plane/dielectric loss, for 1-pair embedded capacitor using the 3-D simulator or hand calculation. The model parameter depends on the size of plane and the height of each layer. Second, find the equivalent series inductance and capacitance for over 2-pair embedded capacitor utilizing the model parameters calculated from 1-pair embedded capacitor. At last, we can generalize the model parameters for multi-layer embedded capacitor, as shown in Figure 2.

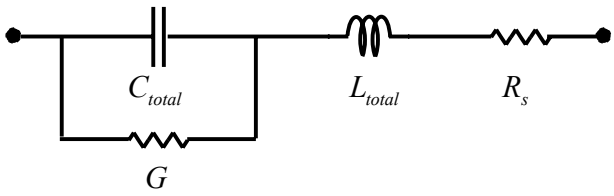

Figure 2. Scalable equivalent circuit model of multi-layer capacitor.

For the one-port multi-layer capacitor which port is located at the center of the capacitor, the model equation for C_{total} and L_{total} are as follows.

$$C_{total} = C_0 \cdot N$$

$$L_{total} = L_0 \,////\, N + (\frac{3 \cdot N - \chi}{2}) \cdot L_V + L_P - 15 \cdot (\frac{N - \chi}{2})\ [pH]$$

,where N represents the number of plane pair, L_0 represents the cavity inductance for 1 plane pair, L_V represents the via inductance between 1 plane pair, L_P represents the plane inductance between signal and ground via, and $L_0 \,////\, N$ represents

$$\underbrace{L_0 // L_0 // \cdots // L_0}_{N}$$

.

If N is odd number, χ is 1, and If N is even number, χ is 2. The equations for R_s and G are as follows.

$$R_s = R_{s0} \,////\, N$$

$$G = G_0 \cdot N$$

$$R_{s0} = \frac{1}{\sigma \cdot \delta_s}$$

$$G_0 = 2\pi f \cdot \tan\delta \cdot \mathrm{C}$$

For the two-port multi-layer capacitor shown in Figure 1, the model equation for C_{total} and L_{total} are as follows.

$$C_{total} = C_0 \cdot N$$

$$L_{total} = L_0 \,////\, N + L_V + \{L_{p1} + (\frac{N + \chi - 2}{2}) \cdot L_V\} // \{L_{p2} + (N + \chi - 2) \cdot L_V\} + (N - \chi) \cdot L_V // \{L_{p2} + \frac{(N - \chi)}{2} \cdot L_V\} - 15 \cdot (\frac{N - \chi}{2})\ [pH]$$

, where L_{P1} represents the plane inductance between signal and ground via of port 1, and L_{P2} represents the plane inductance between signal vias of port 1 and port 2.

The parameters, C_0, L_0, L_V, L_P, L_{P1}, and L_{P2} can be calculated using 3D-full wave simulation.

3. Verification of the Scalable Model using 3D Full-wave Simulation and Measurement

To verify the accuracy of the proposed scalable model, test vehicles, which have 2 x 2 mm size, were designed and fabricated using the Ferro A6 LTCC material with a dielectric constant of 5.9 and a fired dielectric thickness of 98 μm. The self-impedance, Z11, is used to compare the simulated and measured results with the proposed hybrid model. The measured results were compared with the hybrid model.

Figure 3 shows the comparison of the proposed hybrid model and the 3D full-wave simulation of the Z11 parameter, self impedance, for one port multi-layer capacitor with N =2, N =3, N =4, and N =5 up to 15 GHz. The self-resonance frequency of the one-port multi-layer capacitor with N=2 to 5 has a good correlation with the 3D full-wave simulation result.

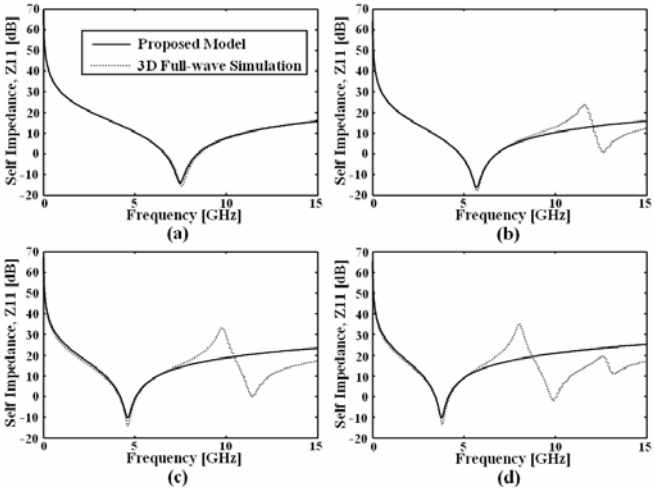

Figure 3. Comparison of the proposed hybrid model and the 3D full-wave simulation of the Z11 parameter, self impedance, for one port multi-layer capacitor with (a) N =2, (b) N =3, (c) N =4, and (d) N =5 up to 15 GHz. The Solid line represents the self impedance, Z11, obtained from the proposed hybrid model and the dotted line represents the self impedance obtained from 3D full-wave simulation by Ansoft HFSS.

The self-resonance frequency of two-port multi-layer capacitor with N =2 to 5 has also a good correlation with the full-wave simulation results as shown in Figure 4.

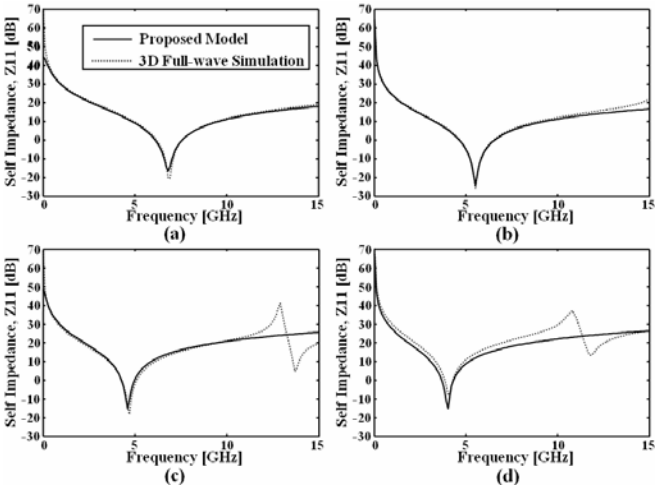

Figure 4. Comparison of the proposed hybrid model and the 3D full-wave simulation of the Z11 parameter, self impedance, for two port multi-layer capacitor with (a) N =2, (b) N =3, (c) N =4, and (d) N =5 up to 15 GHz. The Solid line represents the self impedance, Z11, obtained from the proposed hybrid model and the dotted

line represents the self impedance obtained from 3D full-wave simulation by Ansoft HFSS.

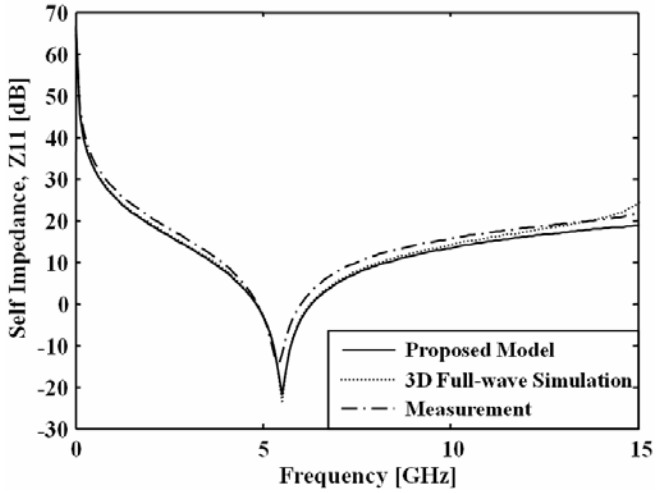

Figure 5. Comparison of the proposed hybrid model, the 3D full-wave simulation, and the measurement of the Z11 parameter, self impedance, for two port multi-layer capacitor with N =3 up to 15 GHz. The Solid line represents the self impedance, Z11, obtained from the proposed hybrid model, the dotted line represents the self impedance obtained from 3D full-wave simulation by Ansoft HFSS, and the dashed-dotted line represents the self impedance obtained from the measurement.

The comparison of the proposed hybrid model, the 3D full-wave simulation, and the measurement of the Z11 parameter, self impedance, for two port multi-layer capacitor with N =3 up is shown in figure 5. The correlation between the proposed hybrid model and 3D full-wave simulation is very good, but there is small error between the measurement and the proposed hybrid model. It is understood that the small difference comes from the shrink effect of the capacitor by LTCC process and the parasitic element of the probe for measurement.

No. of Capacitor Pairs	3D full-wave Simulation (GHz)	Proposed Hybrid Model (GHz)	Error Percentage (%)
N =1	10.5	10.41	0.86
N =2	7.59	7.562	0.37
N =3	5.72	5.7013	0.33
N =4	4.62	4.61	0.22
N =5	3.82	3.79	0.79
N =6	3.28	3.252	0.85
N =8	2.53	2.493	1.46
N =12	1.73	1.692	2.2
N =13	1.58	1.5706	0.59
N =14	1.5	1.463	2.47

Table 1. The error percentage between 3D full-wave simulation and the proposed hybrid model for the multi-layer capacitor with N = 1 to 14.

No. of Capacitor Pairs	C_{total} [pF]	L_{total} [pH]
N =1	2.6	70
N =2	5.2	87
N =3	7.8	100.2
N =4	10.4	114.5
N =5	13	136
N =6	15.6	153.67
N =8	20.8	195.75
N =12	31.2	282.83
N =13	33.8	307.4
N =14	36.4	327

Table 2. The library of the multi-layer capacitor using the proposed hybrid model.

Table 1 shows the error percentage between 3D full-wave simulation and the proposed hybrid model. The difference between the model and the full-wave simulation is within roughly 3%.

Using the proposed model, LTCC package designer can build the library for the multi-layer capacitor they may use like table 2. As shown in the table 2, the capacitance and inductance become increase as the number of the capacitor layer increase, resulting in decreasing the self-resonance frequency.

4. Conclusions

In conclusion, the hybrid model with scalability was proposed for LTCC-based multi-layer embedded capacitor to predict the self-resonance frequency of the multi-layer embedded capacitor. This hybrid approach combines both analytical modeling and numerical modeling to provide a scalable circuit model predicting the self-resonance frequency of the multiple dielectric and electrode layers. The results for the hybrid scalable model show good correlation with the simulated and measured data.

Acknowledgments

This research was supported by the Agency for Defense Development, Korea, through the Radiowave Detection Research Center at Korea Advanced Institute of Science & Technology and the Singapore Institute of Manufacturing Technology, A*STAR, Singapore.

References

[1] R.R. Tummala, Madhavan Swaminathan, Manos M. Tentzeris, Joy Laskar, Gee-Kung Chang, Suresh Sitaraman, David Keezer, Daniel Guidotti, Zhaoran Huang, Kyutae Lim, Lixi Wan, Swapan K. Bhattacharya, Venkatesh Sundaram, Fuhan Liu, and P. Markondeya Raj, "The SoP for Miniaturized, Mixed-Signal Computing, Communication, and Consumer Systems of the Next

Decade", *IEEE Transactions on Advanced Packaging*, Vol. 27, No. 2, pp. 250–267, May 2004.

[2] Sudo T, Sasaki H, Masuda N, and Drewniak J.L, ""Electromagnetic Interference (EMI) of System-on-Package (SoP)", *IEEE Transactions on Advanced Packaging*, Vol. 27, Issue 2, pp. 304–314, May 2004.

[3] Steve Annas, "Advances in Low Temperature Co-Fired Ceramic (LTCC) for Ever Increasing Microelectronic Applications", *Electronic Components and Technology Conference* 2003

[4] Sutono A., Heo D., Emery Chen Y.-J., Laskar J., "High-Q LTCC-based passive library for wireless system-on-package (SOP) module development", *Microwave Theory and Techniques, IEEE Transactions on*, Volume: 49 Issue: 10, Oct 2001, pp 1715-1724

[5] Kim E., Young-Shin Lee, Chan-Sei Yoo, Woo-Seong Lee, Jong-Cheol Park, "A power amplifier module with fully embedded passive components in a LTCC substrate for K-PCS band mobile phone", *Microwave Conference*, 2003. 33rd European, Volume: 1 7-9 Oct. 2003, pp 253- 256 Vol.1

[6] Delaney K., Barrett J., Barton J., Doyle R., "Characterization of the electrical performance of buried capacitors and resistors in low temperature co-fired (LTCC) ceramic", *Electronic Components and Technology Conference*, 1998. 48th IEEE, 25-28 May 1998, pp 900-908

[7] Fathy A., Pendrick V., Ayers G., Geller B., Narayan Y., Thaler B., Chen H.D., Liberatore M.J., Prokop J., Choi K.L., Swaminathan M., "Design of embedded passive components in Low-Temperature Cofired Ceramic on Metal (LTCC-M) technology", *Microwave Symposium Digest*, 1998 IEEE MTT-S International, Volume: 3 7-12 Jun 1998, pp 1281-1284 vol.3

[8] Poddar R., Brooke M.A., "Accurate high speed empirically based predictive modeling of deeply embedded gridded parallel plate capacitors fabricated in a multilayer LTCC process", *Advanced Packaging, IEEE Transactions on*, Volume: 22 Issue: 1 Feb 1999, pp 26-31

[9] Delaney K., Barrett J., Barton J., Doyle R., "Characterization and performance prediction for integral capacitors in low temperature co-fired ceramic technology", *Advanced Packaging, IEEE Transactions on*, Volume 22, Issue 1, Feb 1999, pp 68-77

[10] Carastro L., Ilgu Yun, Poddar R., Brooke M., May G.S., "Statistical analysis of embedded capacitors using Monte Carlo simulation", *Electronic Components and Technology Conference* 2000, pp 198-205

[11] Blood W., Feng Ling, Kamgaing T., Myers T., Petras M., "Simulation, modeling, and testing embedded RF capacitors in low temperature cofired ceramic", *Electronic Components and Technology Conference* 2001, pp 852-857

[12] Chiu C.T., Horng T.S., Ma H.L., Wu S.M., Hung, C.P., "Super broadband lumped models for embedded passives", *Electronic Components and Technology*, 2004. Volume: 1, 1-4 June, pp 1104- 1107 Vol.1