Journal of The Electrochemical Society, **153** (4) C265-C271 (2006)
0013-4651/2006/153(4)/C265/7/$20.00 © The Electrochemical Society

Current Distribution for the Metallization of Resistive Wafer Substrates under Controlled Geometric Variations

Jong-Min Lee,[a,*,z] Heather McCrabb,[a] E. Jennings Taylor,[a,*] and Ron Carpio[b,*]

[a]*Faraday Technology, Incorporated, Clayton, Ohio 45315, USA*
[b]*SEMATECH-ATDF, Austin, Texas, 78741, USA*

Current distribution simulation results are presented for the metallizaton of 200-mm resistive wafer substrates. A novel horizontal plating cell design that features an insulating hole and a wafer holder that is capable of varying the wafer position vertically during the metallization process is considered to improve the current distribution across the wafer substrate surface. Numerical analysis is used to investigate the influence of the insulating hole size, wafer position, and wafer movement during the deposition process on the current distribution and is compared to experimental data for copper deposition when possible.
© 2006 The Electrochemical Society. [DOI: 10.1149/1.2171820] All rights reserved.

Manuscript submitted October 27, 2005; revised manuscript received December 15, 2005. Available electronically March 2, 2006.

Submicrometer scale multilevel metallization is one of the key technologies for the next generation of ultralarge-scale integration.[1] The fabrication of integrated circuits and electronic devices includes several processing steps to incorporate the necessary conducting, semiconducting, and dielectric layers. Electrodeposition of copper for metallization of microchips contained on resistive wafer substrates has become an important processing step.[2-4] Prior to the copper electrodeposition process, a thin conductive copper seed layer, is deposited onto an insulating material, such as a polymer or ceramic, by electroless deposition, physical vapor deposition, or chemical vapor deposition. However, the resistance of the thin conductive seed layer can produce a large potential drop near the interface between the electrolyte and wafer substrate during the electrochemical deposition process, resulting in nonuniform copper thickness distribution across the substrate surface. Typically, the current density is larger at the edges of the wafer, where electrical contact is made to the wafer, than at the center of the wafer, far from the point of electrical contact. This phenomenon is known as the terminal effect.

A number of research studies[5-10] have focused on describing the interfacial phenomena. Matlosz et al.[5] provided a range of valid theoretical approaches. Mehdizadeh et al.[6] presented the influence of a coplanar auxiliary electrode on the current distribution, and Choi and Kang[7] suggested a three-dimensional model to optimize the range of the auxiliary electrode for minimizing the nonuniform thickness distribution across a rectangular patterned substrate. Lee et al.[8] addressed several advantages of using an insulating shield to produce a homogeneous current distribution. They also presented the feasibility of modifying the insulating shield to improve the current distribution across a 3-in. wafer. Deligianni et al.[9] and Cao et al.[10] presented simulation results that analyze the insulating shields' ability to improve the thickness distribution onto a 300-mm wafer. Lanzi and Landau[11] presented a model of current distribution that results from the terminal effect under Tafel kinetics that can be used to estimate the current density variation along the wafer surface. Wilson et al.[12] described a unique plating tool that utilizes a novel electrolyte flow scheme and a multitude of anodes whose distance from the wafer has been optimized to control the current distribution, and Klocke et al.[13] provided simulations and experimental work on 300-mm wafers in which they dynamically control the current distribution during the plating process in order to maintain a uniform current distribution from the initial stage to the final stage of metal deposition.

In this present work, a novel horizontal cell design that features an insulating hole and a wafer holder that is capable of varying the wafer position vertically during the metallization process is considered to improve the current distribution and the resulting metal thickness distribution on a 200-mm resistive wafer substrate that contains a thin copper seed layer. Simulations are compared to experimental data in some cases.

Experimental

The copper electroplating experiments were conducted on the wafer processing tool. An acid copper plating solution containing 0.1 M sulfuric acid, 0.63 M copper sulfate, 50 ppm Cl^-, and 300 ppm polyethylene glycol (PEG) was used for all electroplating experiments. Silicon blanket 200-mm wafers with a 100-nm copper seed layer were used for the current distribution studies. Copper was deposited onto the wafers using direct current under galvanostatic control using a Dynatronix DPR series power supply model DPR20-5-10. Copper balls in titanium baskets were used for the anodes. The current density for the experiments ranged from 6 to 10 mA cm^{-2}. The wafer rotation rate, plating time, and insulating hole opening were held constant for all experiments at 50 rpm, 5 min, and 15 cm, respectively. The distance between the wafer and the insulating hole opening was varied between 5 and 25 cm during the stationary experiments to examine its effect on the current distribution. The lift rate for experiments involving movement of the wafer during the deposition process was held constant at 0.03 cm s^{-1}. Optoacoustic metrology was used to determine the copper thickness distribution across the surface of the as-plated wafers at 49 different points in Fig. 1.

An electrochemical plating cell was designed and built with attributes that allow manipulation of the current field across the surface of semiconductor wafers during the interconnect metallization process. A schematic of the plating cell is shown in Fig. 2. The

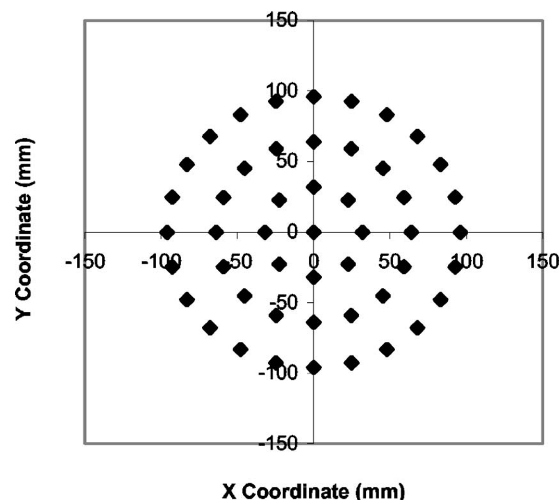

Figure 1. Copper thickness data points measured by optoacoustics.

* Electrochemical Society Active Member.
[z] E-mail: jongminlee@faradaytechnology.com

Downloaded 23 Dec 2010 to 24.106.113.125. Redistribution subject to ECS license or copyright; see http://www.ecsdl.org/terms_use.jsp

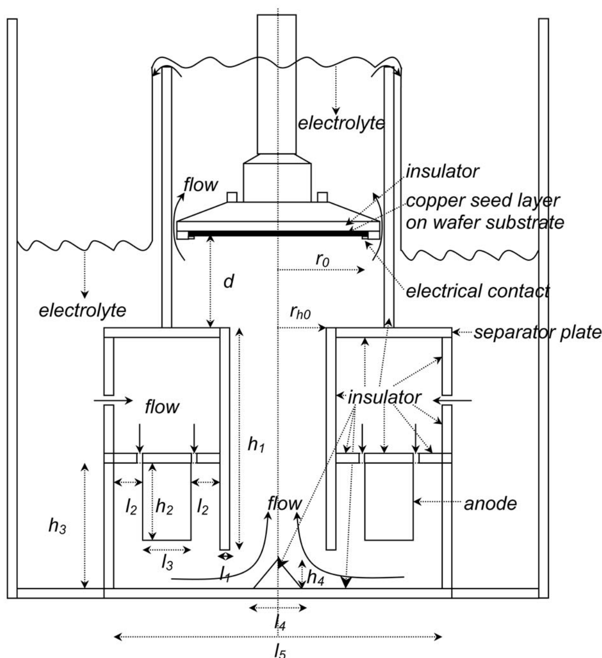

Figure 2. A schematic diagram of the cell design to control the movement of the wafer during the deposition process.

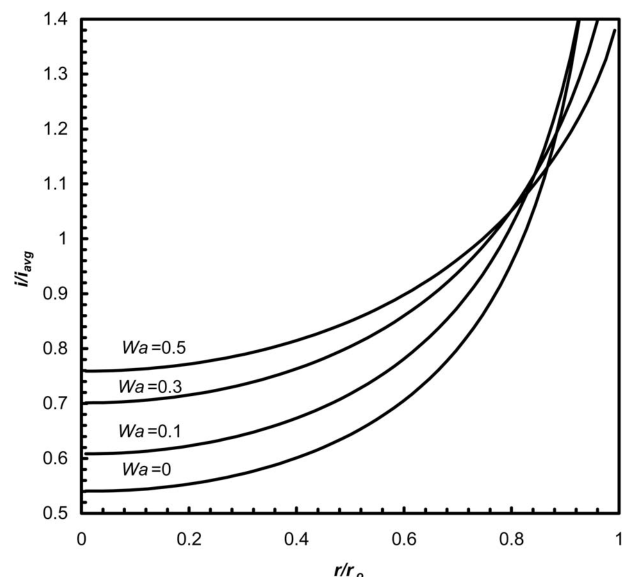

Figure 3. The initial current distribution at $r_{ho}/r_o = 1$ and $d/r_o = 0.5$ for $K_o = 2.0$ and four different *Wa* numbers.

plating cell consists of a tank to hold the plating electrolyte solution, a wafer holder to secure the wafer face down during the plating process, a cylindrical chamber where wafer plating occurs, and a lower chamber to house the insulating hole and anodes. A stainless steel ring is incorporated into the wafer holder to make electrical contact directly to the seed layer at the outer circumference of the wafer. The wafer holder is capable of rotating at rates between 50 and 400 rpm. The wafer holder is lowered face down into the upper cylindrical chamber of the cell at some distance between 5 and 25 cm from the insulating hole opening and can be moved vertically away from or toward the insulating hole opening at rates of 0–5.1 mm s^{-1} during the plating process. The vertical movement allows for the manipulation of the dynamic current distribution that results from the thickening of the copper layer on the surface of the wafer.

The upper plating chamber in the plating cell is mounted on a separator plate that is attached to the lower chamber. The lower chamber contains the insulating hole shaft. The insulating hole shaft shields the anodes from being in the direct line of sight of the wafer, which minimizes current dispersion that can lead to excessive copper thickness at the edge of the wafer. The insulating hole opening is located at the top of the lower chamber and the diameter of the insulating hole opening is adjustable. The insulating hole is another attribute available to control the current distribution during the plating process. Inside the lower chamber around the outside of the insulating hole are six nodes contained inside titanium baskets. A metal bar connected to the electrode container extends up through the separator plate above the electrolyte solution to enable electrical connection to be made to the anodes.

A pump is used to circulate the electrolyte through a filter and into a manifold of inlet pipes that are attached to the separator plate. The electrolyte flows into the lower chamber, past the anodes in the titanium baskets and travels up through the insulating-hole shaft, into the upper chamber and impinges the wafer surface. The electrolyte exits the upper chamber through a gap between the wafer holder and the chamber. The diameter of the gap between the upper chamber and the wafer holder is slightly larger than the diameter of the wafer holder so as to allow the electrolyte to overflow the chamber unimpeded while at the same time minimizing current dispersion that can increase the current density at the edge of the chamber opening.

The electroplating experiments were performed at current densities that were sufficiently lower than the limiting current density. Performing experiments at or near the limiting current density could interfere with determining the extent to which the novel cell design described above influences the current distribution, since operating under mass-transport conditions produces a more uniform current distribution across the entire substrate because the current near the wafer contact cannot exceed the limiting current.

For a rotating disk electrode, such as the case of a rotating wafer, the limiting current density can be approximated by the Levich equation

$$i_l = (0.620)nFD^{2/3}\omega^{1/2}\nu^{-1/6}c \qquad [1]$$

For the electroplating experiments reported here, the Cu^{2+} concentration, c, is 6.3×10^{-4} mol cm^{-3}, the angular rotation rate, ω, of the electrode is 5.24 rad s^{-1}, the kinematic viscosity of the plating solution, ν, was measured and determined to be 1.08 $cm^2\,s^{-1}$ at 25°C, and the diffusion coefficient,[14] D, for Cu^{2+} is taken to be 5.37×10^{-6} $cm^2\,s^{-1}$, yielding a limiting current density of 113 mA/cm^2. The current densities employed for the experiments reported in this paper were between 5 and 9% of the approximated limiting current density; therefore, it is reasonable to assume the influence of tertiary current distribution on copper thickness distribution was negligible.

When quantified, the variation in the copper thickness distribution is quantified using the following equation

$$\%\ \text{deviation} = \frac{(b_{\max} - b_{\min})}{b_{\text{avg}}} \times 100 \qquad [2]$$

Mathematical Model

The schematic diagram of the cell is shown in Fig. 2. The novel horizontal cell design featuring an insulating hole and a wafer holder that can vary the wafer position during the deposition process is considered to reduce spatial variations in the potential fields on the resistive substrate. The cell design includes many geometric dimensions. Several geometric dimensions were fixed in corresponding to experimental cell dimensions. The dimensional distance d and hole

Downloaded 23 Dec 2010 to 24.106.113.125. Redistribution subject to ECS license or copyright; see http://www.ecsdl.org/terms_use.jsp

Table I. Typical variables and parameter values for simulation.

Variables	Values
a	0–100 nm
h_1	25 cm
h_2	10 cm
h_3	16 cm
h_4	3 cm
l_1	0.5 cm
l_2	2 cm
l_3	6 cm
l_4	6 cm
l_5	37.4 cm
r_o	10 cm
σ_a	$5.6 \times 10^5\ \Omega^{-1}\ \text{cm}^{-1}$
κ	$0.01–0.6\ \Omega^{-1}\ \text{cm}^{-1}$
K_o	0–5
Wa	0–2

radius r_{ho} were varied. All the dimensional values were converted to dimensionless values by wafer radius $r_o = 200$ mm.

It is assumed that concentration variations can be neglected. The current density is determined by the local gradient of an electrical potential in the electrolyte by Ohm's law

$$i = -\kappa \nabla \phi_s \qquad [3]$$

The potential field in the electrolyte can be solved using Laplace's equation in cylindrical coordinates

$$\frac{\partial^2 \phi_s}{\partial r^2} + \frac{1}{r}\frac{\partial \phi_s}{\partial r} + \frac{\partial^2 \phi_s}{\partial z^2} = 0 \qquad [4]$$

subject to the following boundary conditions

$$\nabla \phi_s = 0 \quad \text{on insulating walls} \qquad [5]$$

$$V_{\text{anode}} = \phi_s \quad \text{at the anode(s)} \qquad [6]$$

Along the working electrode, the current density is obtained from the gradient in the electrolyte potential through

$$i_c = -\kappa \nabla \phi_s \qquad [7]$$

subject to two types of boundary conditions. For a primary current distribution, valid when the Wagner number is zero

$$\phi_m = \phi_s \qquad [8]$$

When polarization resistance varies with current density, the potential fields in the metal phase and electrolyte phase can be solved with a mixed boundary condition,[5] relating potential fields across the interface to the local current density. A Tafel kinetics would be relevant to metallization

$$\phi_m - \phi_s = \frac{RT}{\alpha_c F}\ln(|i_c|/i_o) \qquad [9]$$

Along the cathode, a combination of a charge balance in the metal phase combined with Ohm's law leads to a second equation

$$i_c = \frac{1}{r}\frac{d}{dr}\left(rs(r)\frac{d\phi_m}{dr}\right) \qquad [10]$$

where $s(r,t) = a\sigma_a + b(r,t)\sigma_b$ is the local conductance of the cathode. The boundary conditions on the potential in the metal phase can be written as

$$\frac{d\phi_m}{dr} = 0 \quad \text{at } r = 0 \qquad [11]$$

and at the periphery of the resistive disk electrode, the potential of the current collector $\phi_m = V_m$ is set so that

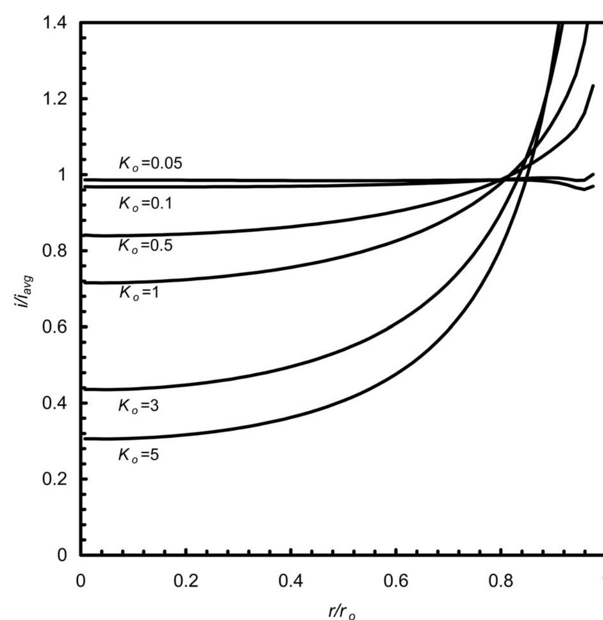

Figure 4. The initial current distribution at $r_{ho}/r_o = 0.75$ and $d/r_o = 1.5$ for $Wa = 0$ and five different K_o values.

$$2\pi r i_{\text{avg}} = s\frac{d\phi_m}{dr} \quad \text{at } r = r_o \qquad [12]$$

The deposited film thickness b based on Faraday's law varies with a position and time on the resistive disk electrode as follows

$$b(r,t) = \int_0^t \frac{|i_c(r,t)|}{nF\rho}dt \qquad [13]$$

Results depend on several dimensionless groups that emerge from detailed analysis for a two-dimensional model[5] and that are geometric parameters, a dimensionless initial seed layer resistance

$$K_o = \frac{\kappa r_o}{a\sigma_a} \qquad [14]$$

and a Wagner number for Tafel kinetics[15]

$$Wa = \frac{\kappa RT}{\alpha_c nFr_o i_{\text{avg}}} \qquad [15]$$

where $i_{\text{avg}} = 10$ mA cm^{-2}, $\kappa = 0.045\ \Omega^{-1}\ \text{cm}^{-1}$, $a = 1000$ Å, $r_o = 10$ cm, $K_o = 0.08$, and $Wa \approx 0.01$ for experimental results reported here.

The electric potential field in the electrolyte was solved by a boundary element method (BEM). A block, tridiagonal matrix algorithm [BAND(J)][15] was used to solve the potential field in the resistive cathode. The two solutions were coupled through the algorithm.[10] The numerical results were validated by varying grid size and the time step size systematically until results did not change further in all calculations.

Results and Discussion

Figure 3 shows the initial current distribution at $r_{ho}/r_o = 1$ and $d/r_o = 0.5$ for $K_o = 2$ and four different Wa numbers. As the radius of insulating hole is equal to that of the wafer, the calculated current distribution is nonuniform at $Wa = 0$, when the ohmic potential drop dominates during the plating process. The distribution becomes more uniform as the Wa number increases.

When the dimensionless parameter h_1/r_o was larger than 2.5, varying the geometric parameters h_2, h_3, h_4 l_1, l_2, l_3, l_4, and l_5 had little influence on the current distribution across the cathode in pre-

Downloaded 23 Dec 2010 to 24.106.113.125. Redistribution subject to ECS license or copyright; see http://www.ecsdl.org/terms_use.jsp

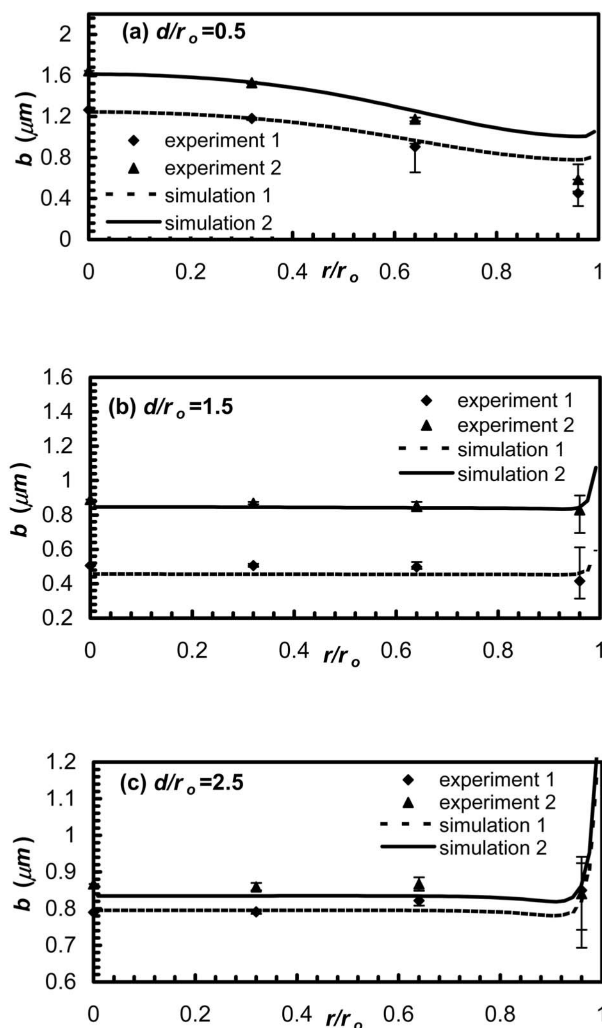

Figure 5. Film thickness as a function of position on the wafer at three different d/r_o in the stationary cell for average film thickness b_{avg}: (a) $b_{avg} = 0.95$ μm for experiment 1 and simulation 1 and $b_{avg} = 1.23$ μm for experiment 2 and simulation 2; (b) $b_{avg} = 0.48$ μm for experiment 1 and simulation 1 and $b_{avg} = 0.86$ μm for experiment 2 and simulation 2, and (c) $b_{avg} = 0.81$ μm for experiment 1 and simulation 1 and $b_{avg} = 0.86$ μm for experiment 2 and simulation 2. In all cases, $r_{ho}/r_o = 0.75$, $K_o = 0.08$, and $Wa = 0.01$.

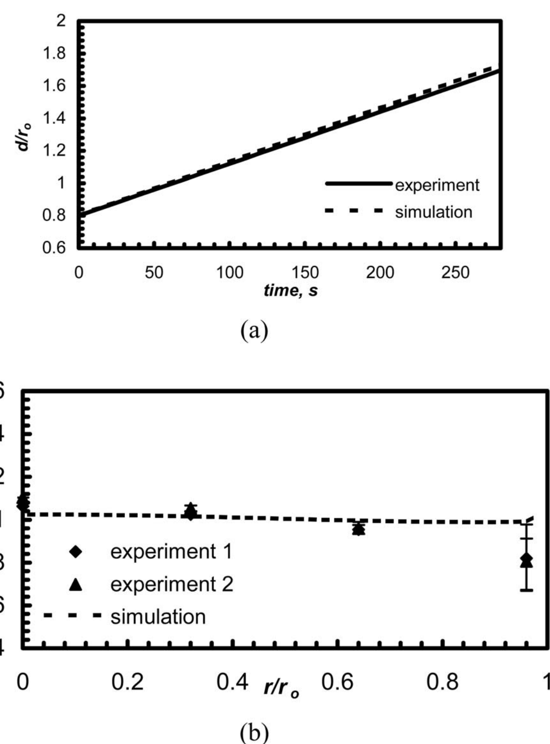

Figure 6. (a) Position of wafer with respect to the insulating hole as a function of deposition time for the moving tool experiments and (b) average film thickness (b_{avg}) distribution as a function of position on the wafer resulting from varying the wafer to insulating hole opening during the deposition process, $b_{avg} = 0.904$ μm for experiment 1, $b_{avg} = 0.905$ μm for experiment 2, and $b_{avg} = 0.9$ μm for simulation. In all cases, $r_{ho}/r_o = 0.75$, $K_o = 0.08$, and $Wa = 0.01$.

liminarily simulated results. Thus, the value of h_1/r_o was set at 2.5 and the other parameters were not varied in this analysis. Table I presents more detailed information on these parameters.

The influence of the dimensionless initial seed layer resistance is shown at $r_{ho}/r_o = 0.75$ and $d/r_o = 1.5$ for $Wa = 0$ and five different K_o values in Fig. 4. The results indicate that the dimensionless initial seed layer resistance has a large influence on the current distribution. The current distribution becomes more uniform as K_o approaches zero, while it becomes increasingly more nonuniform as K_o increases.

Stationary tool experiments.— Two sets of three experiments that fixed the wafer to insulating hole entrance distance at $d/r_o = 0.5$, 1.5, or 2.5 for two different average film thickness values, b_{avg}, were conducted in order to examine the influence of the wafer to insulating hole entrance distance on the current distribution and the influence of the evolution of the deposit thickness on the wafer position in the stationary cell during the deposition progress. The deposit thickness as a function of wafer radius was obtained for each of the three experiments performed at the two different average film thickness values. Although this experimental approach does not provide the growing deposit directly, it was useful for obtaining the experimental data needed for comparison with the simulation results that shows the evolution of deposit thickness for average film thickness.

Figure 5 shows two final deposit thickness values as a function of the dimensionless wafer radius at $r_{ho}/r_o = 0.75$ for the three values of d/r_o when$K_o = 0.08$ and $Wa = 0.01$. The average film thickness, b_{avg}, was 0.95 μm for experiment 1 and simulation 1 and 1.23 μm for experiment 2 and simulation 2 at $d/r_o = 0.5$, 0.48, and 0.86 μm at $d/r_o = 1.5$, 0.81, and 0.86 μm at $d/r_o = 2.5$, respectively, in Fig. 5a. The experimental results are generally in good agreement with the simulation results except at the wafer edge. This discrepancy is possibly due to the exposure of the stainless steel ring that makes electrical contact at the outer circumference of the wafer during the deposition process and due to the fluid flow that impinges the wafer surface and then passes through a small gap between the wafer holder and the chamber more strongly at $d/r_o = 0.5$ than at $d/r_o = 1.5$ and 2.5.

When the wafer is held stationary in close proximity to the insulating hole opening, such as the case in Fig. 5a, the current is strongly focused in the center of the wafer, resulting in a reverse terminal effect that causes the copper to be thicker in the center of the wafer and thinner at the edge of the wafer. Although this situation is not ideal for uniform copper deposition on wafers, it may be beneficial for removal of the copper overburden that occurs during deposition and is removed subsequent to plating using chemical mechanical planarization (CMP). It has been suggested that removing copper from the center of the wafer out toward the edge can circumvent wafer scale nonuniformities that create feature dishing or elec-

Downloaded 23 Dec 2010 to 24.106.113.125. Redistribution subject to ECS license or copyright; see http://www.ecsdl.org/terms_use.jsp

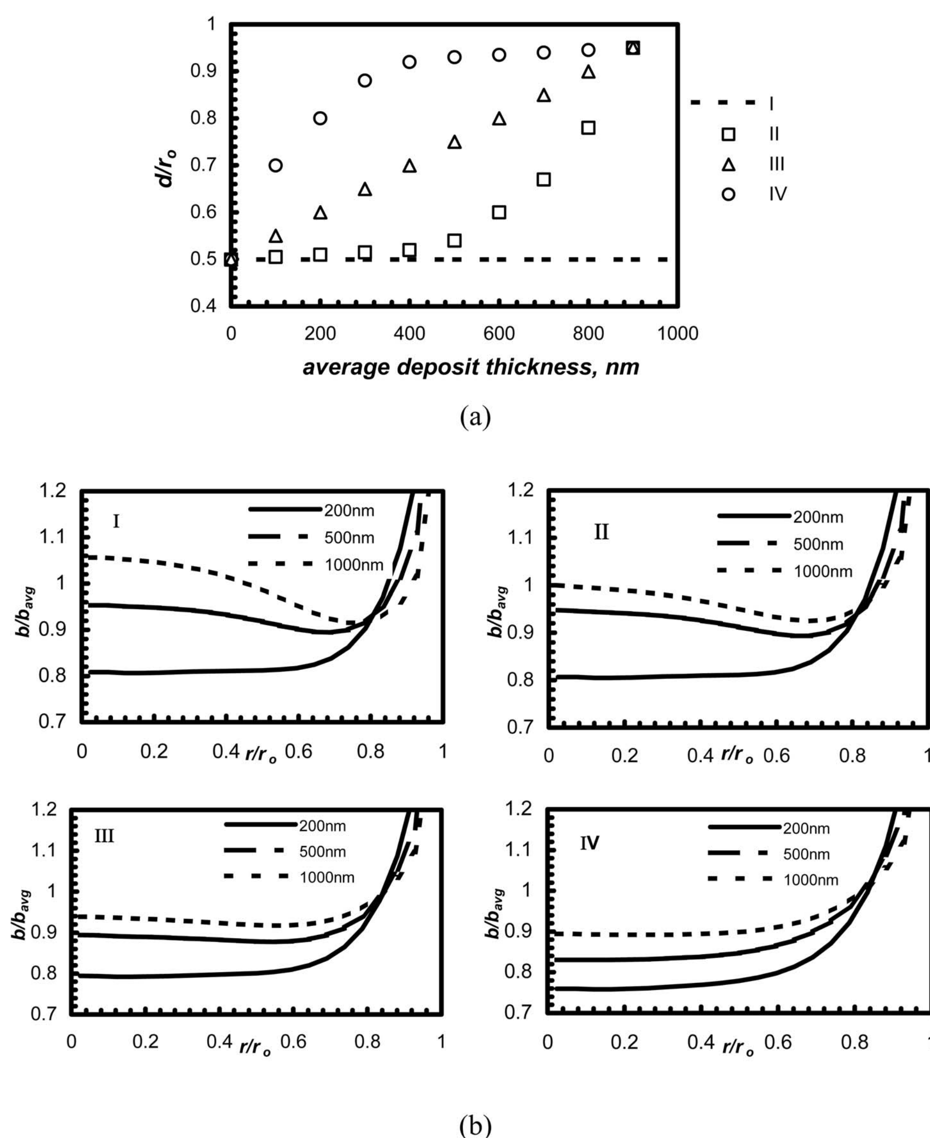

Figure 7. (a) Wafer position with respect to the insulating hole opening as a function of film thickness. Case I-Wafer position remains fixed during the deposition process. Case II-Increasing wafer movement rate results in small increase in wafer to insulating hole distance initially followed by a larger increase in wafer to insulating hole distance as the wafer lift rate increases throughout the deposition process. Case III-Constant wafer movement rate results in linear increase in distance between wafer and insulating hole during the deposition process. Case IV-Decreasing the wafer movement rate results in a large increase in wafer to insulating hole distance, initially followed by a smaller increase in wafer to insulating hole distance as the wafer movement rate decreases as the deposition process progresses. (b) The deposit thickness normalized by average thickness as a function of position on the wafer at $r_{ho}/r_o = 0.75$ for $K_o = 2$ and $Wa = 0$ for the four different cases represented in (a).

trically isolated copper islands that negatively impact the performance of the interconnect.[16] When d/r_o is 1.5 and 2.5, the current distributions are generally uniform in both cases.

Moving tool experiments.— Two experiments that involve increasing the distance between the wafer and the insulating hole opening during the deposition process were conducted in order to examine how varying the wafer position with respect to the insulating hole opening influences the current distribution. The initial value of d/r_o was 0.8 from the insulating hole opening, and the final value of d/r_o was 1.7 from the insulating hole opening. The experiment was repeated in order to ascertain the precision of the design of the electrochemical plating cell. Figure 6b shows the film thickness as a function of position on the wafer when varying d/r_o during the deposition process for $K_o = 0.08$ and $Wa = 0.01$. The average film thickness values, b_{avg}, for experiment 1, experiment 2, and the simulation were 0.904, 0.905, and 0.9 μm, respectively. Although the optimization of the variation of d/r_o was not attempted here, the simulation and experimental results indicate that there is an optimal variation of d/r_o. The experimental results are in good agreement with the simulation results except the case at the edge in Fig. 6b. Possible reasons for this discrepancy are described in the previous section. Results shown in Fig. 4-6 clearly indicate that when K_o is close to zero, the initial cell parameter is important for uniform current distribution while the variation of the geometric parameter is not necessary during the metallization process.

For $K_o = 2$, the importance of the dimensionless distance d/r_o between the wafer and the insulating hole entrance is presented for $r_{ho}/r_o = 0.75$ and $Wa = 0$ in Fig. 7. Here the distance between the wafer and the insulating hole entrance, d/r_o, varies during the plating process, and the target average deposit thickness is near 1000 nm, as shown in Fig. 7a. The deposit thickness normalized by average thickness as a function of position on the wafer is shown in Fig. 7b.

For case I in Fig. 7b, d/r_o remains constant at 0.5. The thickness distribution becomes more uniform as the deposit thickness increases. The deviation in the thickness distribution at 1000-nm average film thickness is about 15% for $r/r_o \leq 0.8$. The deviation becomes 25% at 2000 nm, even though the data is not shown here. The nonuniformity in the thickness distribution is caused by the variations in the local conductivities on the substrate as deposition evolves. The uneven copper topography that results from the nonuniform copper thickness distribution may cause difficulties, such as dishing or erosion, for the subsequent CMP process when depositing films on patterned wafers. The simulation results for case I support the need for modification of the geometric parameter d/r_o during the

Downloaded 23 Dec 2010 to 24.106.113.125. Redistribution subject to ECS license or copyright; see http://www.ecsdl.org/terms_use.jsp

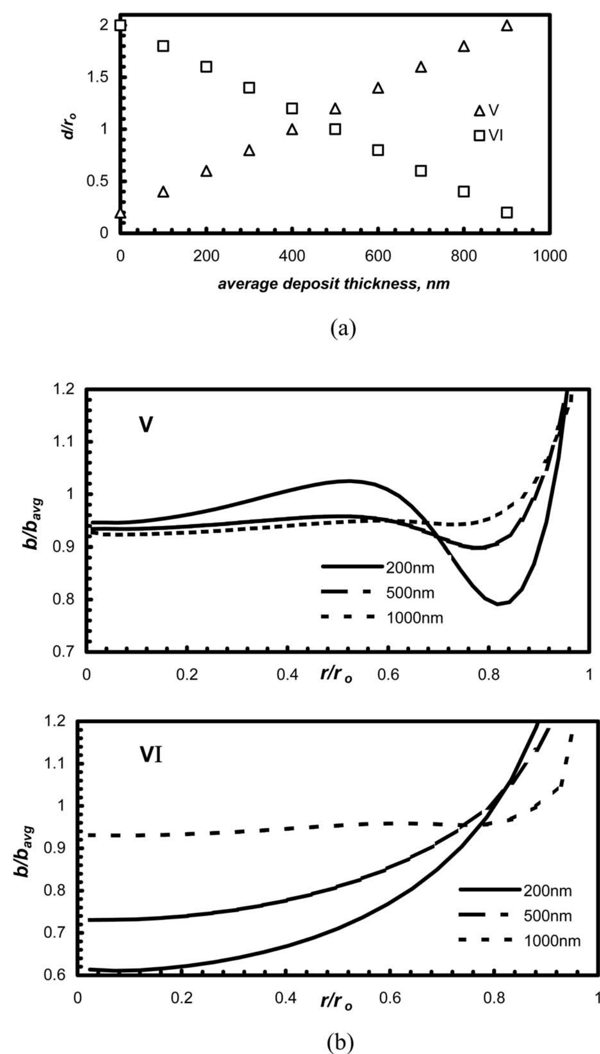

Figure 8. (a) Wafer position with respect to the insulating hole opening as a function of film thickness. Case V-Constant wafer movement rate results in linear increase in distance between wafer and insulating hole during the deposition process. Case VI-Constant wafer movement rate results in linear decrease in distance between the wafer and insulating hole during the deposition process. (b) The deposit thickness normalized by average thickness as a function of position on the wafer at $r_{ho}/r_o = 0.75$ for $K_o = 2$ and $Wa = 0$ for the two different cases represented in (a).

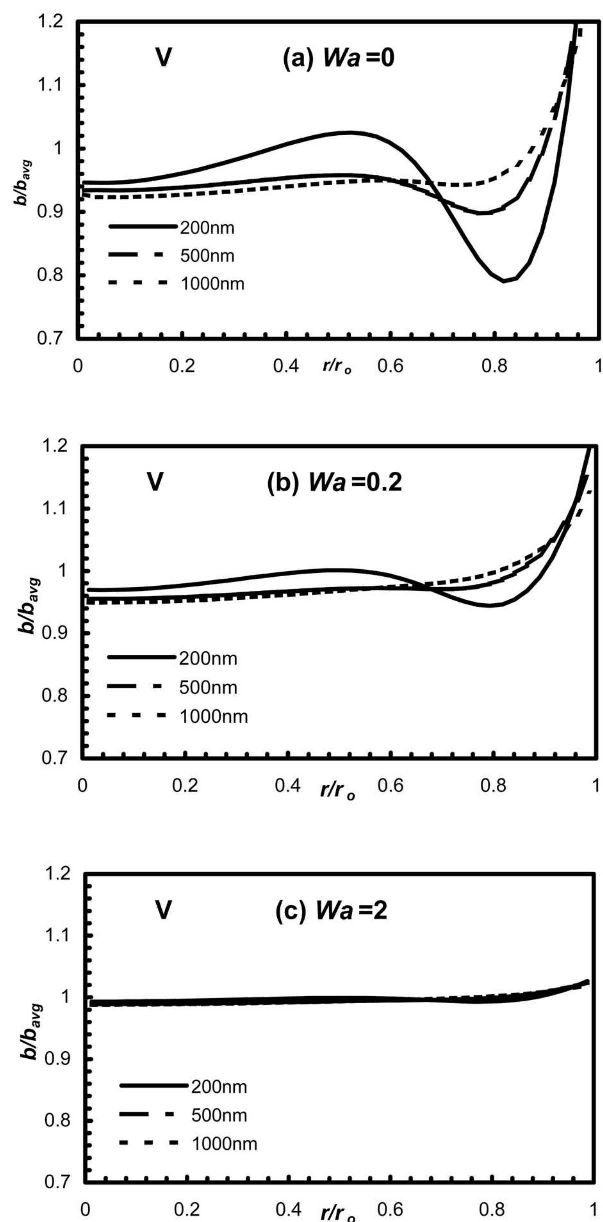

Figure 9. Deposit thickness normalized by average thickness as a function of position on the wafer for three different *Wa* numbers at $r_{ho}/r_o = 0.75$ for $K_o = 2$ for case V.

deposition process to improve electrical fields between electrolyte and substrate in order to achieve a uniform thickness distribution at a target thickness deposit.

Case II represents the situation where the distance between the wafer and insulating hole opening increases gradually during the deposition until a deposit thickness of 500 nm, at which time the distance d/r_o increases considerably until the final average deposit thickness of 1000 nm is achieved. For case II, the deviation in the thickness distribution at 1000-nm average film thickness is about 7% for $r/r_o \leqslant 0.8$. Case III represents a linear change of $d/r_o = 0.05$ after every 100 nm of metal deposition. Case IV is the converse of case II, that is, the wafer to insulating hole-opening distance, d/r_o, changes rapidly up to 500 nm average deposit thickness, at which time the change in distance between the wafer and the insulating hole, d/r_o, progresses much more slowly until the final average deposition thickness of 1000 nm. The deviation in the thickness distribution at 1000 nm average film thickness is approximately 2 and 8% for $r/r_o \leqslant 0.8$ for cases III and IV, respectively. In cases II–IV, even though these three cases are not optimized, the simulated results clearly show improved thickness distribution values for a 1000-nm deposit as compared to the case I results.

Another scenario in which the deposit thickness normalized by average thickness as a function of wafer position for $r_{ho}/r_o = 0.75$, $Ko = 2$, and $Wa = 0$ under controlled wafer position during the deposition process (Fig. 8a) is presented in Fig. 8b. Case V represents a linear increase of $d/r_o = 0.2$ from an initial wafer to insulating hole distance of $d/r_o = 0.2$ to a final wafer to insulating hole distance of $d/r_o = 2$ after every 100 nm of metal deposition. Case VI is the converse of case V. The wafer to insulating hole distance, d/r_o, decreases linearly from $d/r_o = 2$ to $d/r_o = 0.2$ in increments of 0.2 every 100 nm of metal deposition. The film thickness distribution values vary significantly at 200, 500, and 1000 nm in both cases, but the final film thickness distributions at 1000 nm areuniform and equal to approximately 2% for $r/r_o \leqslant 0.8$ for both cases V and VI.

Downloaded 23 Dec 2010 to 24.106.113.125. Redistribution subject to ECS license or copyright; see http://www.ecsdl.org/terms_use.jsp

The influence of the electrode kinetics is shown in Fig. 9 for case V ($K_o = 2$ and $r_{ho}/r_o = 0.75$) for three different *Wa*. The results indicate that the thickness distribution uniformity improves and the influence of the geometric variation on the thickness distribution values decrease as the *Wa* number increases.

Conclusions

Current and thickness distribution simulation results are presented for the metallization of 200-mm resistive wafer substrates. A novel horizontal cell design that features an insulating hole and a wafer holder that is capable of varying the wafer position vertically during the deposition process is considered to improve current distribution across the wafer substrate. The experimental results are generally in good agreement with the simulation results. When the dimensionless initial seed layer resistance K_o was close to zero, the initial geometric parameter d/r_o was important for uniform current distribution and the variation of the geometric parameter d/r_o was not necessary during the process. In contrast, when $K_o = 2$, the variation of the geometric parameter d/r_o was effective for improving the thickness distribution on the substrate during the deposition process. Therefore, geometric parameters or geometric variation should be carefully optimized with the initial seed layer resistance and final film thickness.

Acknowledgments

This material is based upon work supported by the National Science Foundation under grant no. DMI-04216388 and DMI-0131791. Any opinions, findings, conclusions, or recommendations expressed in this material are those of the authors and do not necessarily reflect the views of the National Science Foundation.

Faraday Technology assisted in meeting the publication costs of this article.

List of Symbols

- a seed layer thickness, cm
- b local electrodeposit thickness, cm
- b_{avg} average electrodeposit thickness
- b_{max} maximum local electrodeposit thickness, cm
- b_{min} minimum local electrodeposit thickness, cm
- c concentration of copper ion, mol cm^{-3}
- d distance between insulating hole entrance and cathode, cm
- D diffusion coefficient, cm^2 s^{-1}
- F Faraday's constant, 96,487 C/equiv
- h_1 length of the height in the insulating hole, cm
- h_2 length of the height in the anode, cm
- h_3 length of the height in the bottom chamber, cm
- h_4 length of the height in the insulator, cm
- i_{avg} average current density on the cathode, A/cm^2
- i_c local current density on the cathode, A/cm^2
- i_o exchange current density, A/cm^2
- i_l limiting current density
- l_1 length of the width in the insulator, cm
- l_2 length of the width in the insulator, cm
- l_3 length of the width in the anode, cm
- l_4 length of the width in the insulator, cm
- l_5 length of the width in the bottom chamber, cm
- K_o dimensionless initial seed layer resistance
- r_{ho} radius of the hole in the electrical current shield, cm
- r_o radius of the cathode, cm
- n valence number, equiv/mol
- r cylindrical coordinate, cm
- R ideal gas constant, 8.314 J/mol K
- s cathode conductance, Ω^{-1}
- t time, s
- T absolute temperature, K
- V_{anode} potential of anode, volt
- V_m electrode potential at cathode current collector, volt
- Wa Wagner number
- z cylindrical coordinate, cm

Greek

- α_c cathodic charge-transfer coefficient, 0.5
- κ electrolyte conductivity, Ω^{-1} cm^{-1}
- ν kinematic viscosity of the solution, cm^2 s^{-1}
- ρ molar density of the electrodeposit, mol cm^{-3}
- σ_a seed layer conductivity, Ω^{-1} cm^{-1}
- σ_b deposit conductivity, Ω^{-1} cm^{-1}
- ϕ_m potential in electrode, V
- ϕ_s potential in electrolyte, V
- ∇ gradient operator
- ω angular rotation rate of the electrode, rad/s

References

1. A. Duboust, S. S. Chang, L. Y. Chen, Y. Wang, S. Neo, L. Sun, and F. Q. Liu, U.S. Pat. 6,776,693B2 (2004).
2. L. L. Chen, U.S. Pat. 6,197,181 (2001).
3. C. E. Uzoh, H. Deligianni, and J. O. Dukovic, U.S. Pat. 6,261,426 (2001).
4. E. K. Broadbent, U.S. Pat. 6,027,631 (2000).
5. M. Matlosz, P. H. Vallotton, A. C. West, and D. Landolt, *J. Electrochem. Soc.*, **139**, 752 (1992).
6. S. Mehdizadeh, J. Dukovic, P. C. Andricacos, L. T. Romankiw, and H. Y. Cheh, *J. Electrochem. Soc.*, **137**, 110 (1990).
7. Y. S. Choi and T. Kang, *J. Electrochem. Soc.*, **143**, 480 (1996).
8. J.-M. Lee, J. T. Hachman, J. J. Kelly, and A. C. West, *J. Microlithogr., Microfabr., Microsyst.*, **3**, 146 (2004).
9. H. Deligianni, J. O. Dukovic, E. G. Walton, R. J. Contolini, J. Reid, and E. Patton, in *Electrochemical Processing in ULSI Fabrication and Semiconductor/Metal Deposition II*, P. C. Andricacos, P. C. Searson, C. Reidsema-Simpson, P. Allongue, J. L. Stickney, and G. M. Oleszek, Editors, PV 99-9, p. 83, The Electrochemical Society Proceedings Series, Pennington, NJ (2000).
10. Y. Cao, J.-M. Lee, and A. C. West, *Plat. Surf. Finish.*, **90**, 40 (2003).
11. O. Lanzi and U. Landau, *J. Electrochem. Soc.*, **137**, 1139 (1990).
12. G. J. Wilson, P. R. McHugh, and K. M. Hanson, U.S. Pat. 6660137 B2 (2003).
13. J. Klocke, P. R. McHugh, K. Ritari, M. Roberts, and T. Ritzdorf, in *Proceedings of Advanced Metallization Conference*, Materials Research Society, pp. 373–377 (2002).
14. B. Q. Wu, Z. Liu, A. Keigler, and J. Harrell, *J. Electrochem. Soc.*, **152**, C272 (2005).
15. J. S. Newman, *Electrochemical Systems*, Prentice-Hall, Inc., Englewood Cliffs, NJ (1973).
16. W. E. Corbin, Jr., M. Datta, T. E. Dinan, and F. W. Kern, U.S. Pat. 5,865,984 (1999).

Downloaded 23 Dec 2010 to 24.106.113.125. Redistribution subject to ECS license or copyright; see http://www.ecsdl.org/terms_use.jsp