Hindawi Publishing Corporation
Active and Passive Electronic Components
Volume 2010, Article ID 702759, 5 pages
doi:10.1155/2010/702759

Research Article

A 12 dB 0.7 V 850 μW CMOS LNA for 866 MHz UHF RFID Reader

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Received 4 March 2010; Revised 5 May 2010; Accepted 12 May 2010

Academic Editor: Yuh-Shyan Hwang

The design of a narrow-band cascode CMOS inductive source-degenerated low noise amplifier (LNA) for 866 MHz UHF RFID reader is presented. Compared to other previously reported narrow-band LNA designs, in this paper the finite g_{ds} $(= 1/r_0)$ effect has been considered to improve the nanometric design, achieving simultaneous impedance and minimum F_{min} noise matching at a very low power drain of 850 μW from a 0.7 V supply voltage. The LNA was fabricated using the IBM 130 nm CMOS process delivering a forward power gain (S_{21}) of $\approx$ 12 dB, a reverse isolation (S_{12}) of ≈ -34 dB, an output power reflection (S_{22} @866 MHz) of ≈ -25 dB, and an input power reflection (S_{11} @866 MHz) of ≈ -12 dB. It had a minimum pass-band NF of around 2.2 dB and a third-order input referred intercept point (IIP3) of ≈ -11.5 dBm.

1. Introduction

RFID (radio-frequency identification) is one of the fastest growing wireless communication technologies for commercial product tracking. As the low noise amplifier (LNA) is the first block in the front-end of the RFID reader which is tuned at a certain transreceiver frequency, it needs to be designed optimally to minimize the noise for the following stages and avoid the distortion of the source signal (requires good linearity). To overcome design trade-off difficulties between gain, power, noise figure (NF) and matching in the optimization of the LNA, the design of the matching circuits at the input and the output are based, respectively, on minimal NF and maximal power transfer. In recent years, considerable research on CMOS LNA design in submicron technologies at 900 MHz have been reported by many authors in [1–4]. A lower frequency standard for UHF RFID at 866 MHz is also implemented in Europe, Africa, and New Zealand. Low power dissipation at low supply voltage is a significant design criterion for RFID applications synthesized by design trade-off between gain, NF, input and output impedance matching and high linearity. In this paper we discuss the design and the experimental results for a 0.7 V low-power 130 nm CMOS 866 MHz single-ended common-source telescopic cascode LNA using an *enhanced* power constrained simultaneous noise and impedance matching (PCSNIM [5, 6]) technique.

2. Principles and Circuit Design

An inductively source degenerated telescopic cascode topology has been chosen for the 866 MHz RFID LNA design due to its current reuse structure and hence it consumes less bias current than the folded cascode. Figure 1 shows the circuit diagram of the proposed RFID LNA. M_1 and M_2 forms the cascode configuration and their bias currents are driven by M_3 and R_{ref}. L_d, R_d, and C_d form the output tank circuit tuned at 866 MHz with an angular frequency bandwidth of $1/(R_d * C_d)$. C_{ac} denotes ac-coupling capacitor (one at the source input and the other at the output load) while C_b is an ac grounding capacitor at the gate of the cascoding device M_2. L_s provides the inductive source degeneration. An *improved* PCSNIM technique is adopted here for the telescopic cascode LNA structure optimization. C_e is in parallel with C_{gs1} of M_1 in order to achieve minimum noise figure F_{min} with power constraint and higher unity gain frequency ω_T. Optimal impedance Z_{opt}

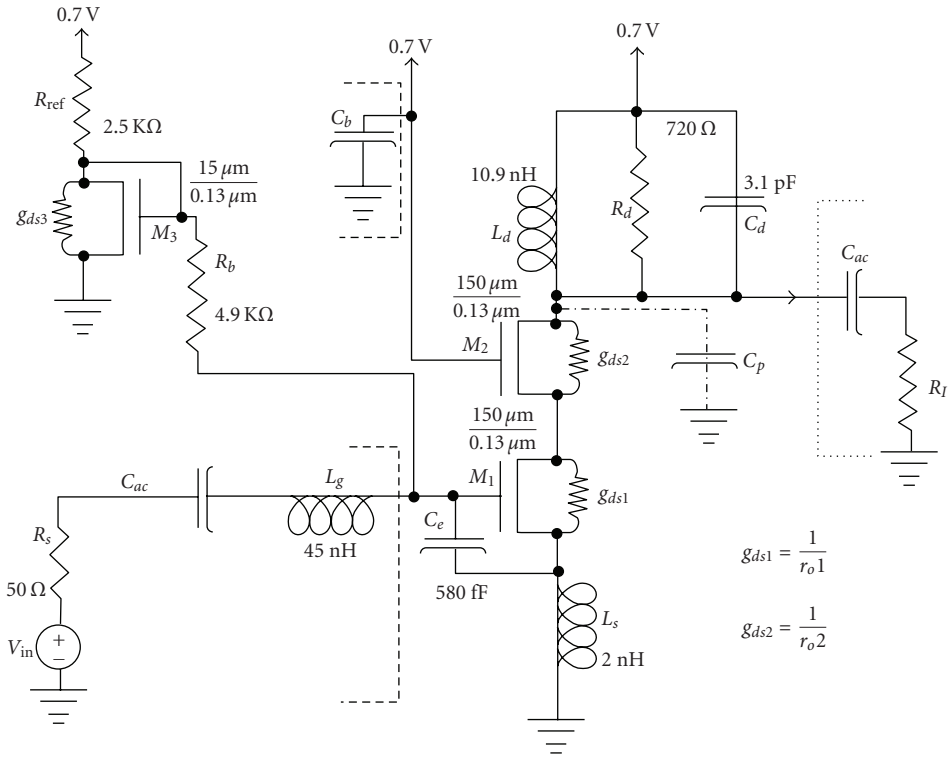

Figure 1: Proposed narrow-band circuit topology for 866 MHz RFID LNA.

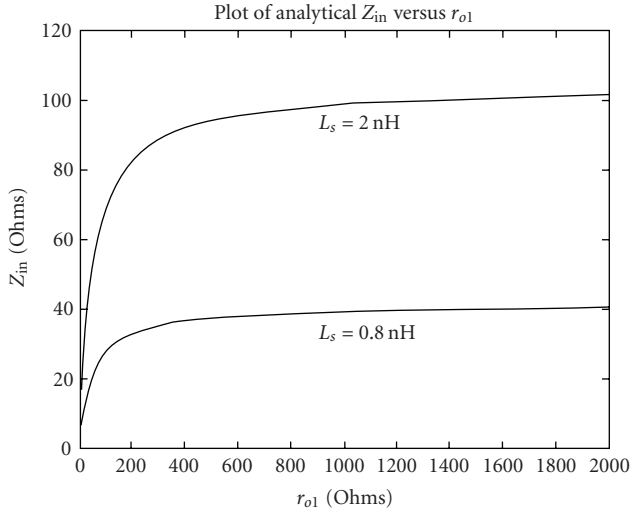

Figure 2: Variation of the analytical Z_{in} with finite output impedance (r_{o1}) of M1 fornanometric CMOS.

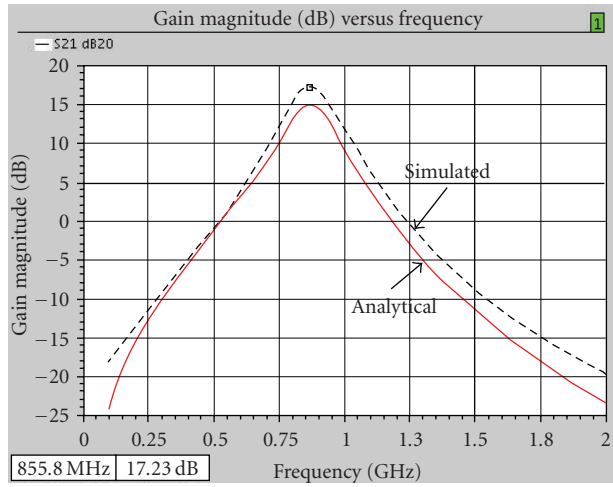

Figure 3: Analytical and simulated gain-magnitude (A_V in dB) of the RFID LNA.

for noise match can be derived to achieve the theoretical F_{min} [5, 6]. The effect of the finite device conductance g_{ds} (= $1/r_0$) due to the deeply scaled short channel length is included in this design optimization. With regard to the input impedance matching at resonance, we can easily derive

$$Z_{in} \cong \frac{g_{m1}}{C_t} \frac{L_s g_{m2}}{(g_{ds1} + g_{m2})}, \quad (1)$$

where C_t equals $C_{gs1} + C_e$, $g_{ds1}(= 1/r_{o1})$ is the output conductance of M_1, while g_{m1} and g_{m2} are the transconductances of the cascode transistors M_1 and M_2, respectively. Typically Z_{in} at resonance changed by 6%–12% due to the inclusion of g_{ds1} in (1) as indicated by the plot in Figure 2 of the analytical Z_{in} with variation in the r_{o1} of M_1 (being around 450 ohms in this design) from the long channel assumption ($r_{o1} \rightarrow \infty$). In addition, as shown in Figure 2, the extent of Z_{in} inaccuracy with long channel assumption also varies

with the chosen value of L_s, the source inductor. Equation (1) also indicates that for deep nanometric design the finite output conductance of M_1 adds an additional trade-off factor in determining the value of the capacitor C_e (in C_t) required for achieving power-constrained input matching. Changing the overdrive and/or the geometry of M_2 (and hence g_{m2}) in relation to g_{ds1} provides an additional degree of freedom to reach this value of C_e for input matching. Essentially this trade-off enables a lower value of C_e and hence a higher ω_T in achieving input impedance matching for a given g_{m1}. In addition, inclusion of the finite g_{ds} effect provides a more accurate power constrained simultaneous optimization of noise and impedance matching for nanometric CMOS (hence it is termed *enhanced* PCSNIM). The s-domain gain transfer function of the RFID LNA can be determined by first finding the short circuit transconductance (G_{M1}) and then the open circuit output impedance ($Z_{\mathrm{OUT}M1}$) at the drain of M_1. Hence, we can deduce the voltage gain as

$$A_v(s) = \frac{\left[g_{m1} + \left((sC_t + g_{m1})(R_{Ls} + sL_s)\right)/(r_{01} + R_{Ls} + sL_s)\right] * \left(1/(sC_d + 1/R_d + 1/sL_d)\right)}{\left[1 + sC_t\left(R_s + R_{\mathrm{Lg}} + R_{Ls} + R_{\mathrm{ge}} + sL_g + sL_s\right) + \left(g_{m1} + sC_t\right)\left((r_{01}(R_{Ls} + sL_s))/(r_{01} + R_{Ls} + sL_s)\right)\right]}, \tag{2}$$

where R_s is the source resistance, R_{Lg} is the series resistance of the gate inductor, R_{Ls} is the series resistance of the source inductor, and R_{ge} is an equivalent gate resistance due to the addition of C_e, which is smaller than the original gate resistance R_g of the transistor M_1. The dB magnitude comparison of the theoretical (analytical) gain with the simulated gain is shown in Figure 3 indicating close agreement between the two. A technique based on determining the short circuit output noise current power at the drain of M_1 was used for the noise analysis. In this method the output load is shorted compared to the method in [5] where the output noise current is determined with the output load. Since the noise factor is defined as the ratio of the total mean-squared output noise current due to all the noise sources to the input source only, and as the noise factor mostly depends on the front-end noise sources farthest from the output load, almost the same value of noise factor is obtained using this technique without the extra calculation, compared to if the output noise current with load is used in the computation. Hence, the noise factors of the front-end noise sources using this short circuit output noise current method, are added to obtain the overall frequency behavior of the noise factor ($N(f)$) given by

$$\begin{aligned} N(f) = 1 &+ \frac{\delta_1\alpha_1}{5}\frac{\omega^2 C_{gs1}^2}{R_s g_{m1}}\frac{\left\{g_{m1}r_{01}^2R_s - \omega^2L_s\left[L_s + g_{m1}r_{01}\left(L_s + L_g\right)\right]\right\}^2 + \omega^2 r_{01}^2\left[L_s(1 + g_{m1}R_s) + g_{m1}r_{01}\left(L_g + L_s\right)\right]^2}{\omega^2C_t^2\left(r_{01}^2 + \omega^2L_s^2\right)\left(\omega L_s + g_{m1}r_{01}/\omega C_t\right)^2} \\ &+ \frac{\gamma_1 g_{m1}}{\alpha_1 R_s}\frac{r_{01}^2\left\{\left[1 - \omega^2C_t\left(L_g + L_s\right)\right]^2 + \omega^2C_t^2R_s^2\right\}}{\omega^2C_t^2\left(\omega L_s + g_{m1}r_{01}/\omega C_t\right)^2} \\ &+ 2j|c_1|\frac{\omega C_{gs1}r_{01}}{R_s\omega^2C_t^2\left(\omega L_s + g_{m1}r_{01}/\omega C_t\right)^2} \\ &\times\sqrt{\frac{\delta_1\gamma_1}{5}\frac{\mathfrak{A}\omega^2r_{01}^2\left[L_s(1 + g_{m1}R_s) + g_{m1}r_{01}\left(L_g + L_s\right)\right]^2\left\{\left[1 - \omega^2C_t\left(L_g + L_s\right)\right]^2 + \omega^2C_t^2R_s^2\right\}}{\left(r_{01}^2 + \omega^2L_s^2\right)}}, \end{aligned} \tag{3}$$

where $\mathfrak{A}$ denotes $\{g_{m1}r_{01}^2R_s - \omega^2L_s[L_s + g_{m1}r_{01}(L_s + L_g)]\}^2$. It is evident from (3) that inclusion of $g_{\mathrm{ds}1}$ $(= 1/r_{o1})$ provides a more detailed expression and hence a more accurate estimate of the noise factor.

3. Simulation and Experimental Results

The LNA (as part T8BTAU) was fabricated using the 130 nm IBM CMOS process available through MOSIS. Figure 4 shows the microphotograph of the 0.571 sq.mm die. The outer diameters of the inductors were, respectively, 240 μm for L_d and 140 μm for L_s with 5 μm wide trace of top thick aluminum layer MA and underpass contact copper layer E1. The capacitors C_e and C_d were fabricated as MIM (metal-insulator-metal) capacitors, and the resistors were fabricated using p+ poly layer with high-sheet resistance (340 $\Omega/\square$). Figure 5 shows the simulated and measured forward power gain, S_{21} under matched condition [8], indicating reasonably high-Q tuning at 866 MHz with measurement being 4 dB below simulation due to loss along external matching circuit. The measured input reflection coefficient S_{11} is approximately ≈ -12 dB at 866 MHz as shown in Figure 6, while the

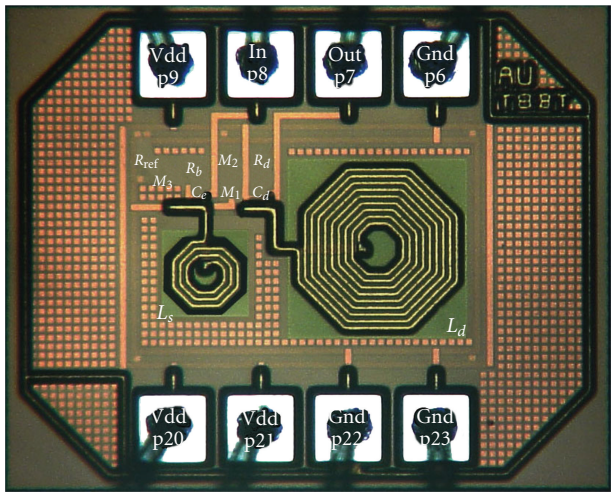

FIGURE 4: Microphotograph of the fabricated RFID LNA.

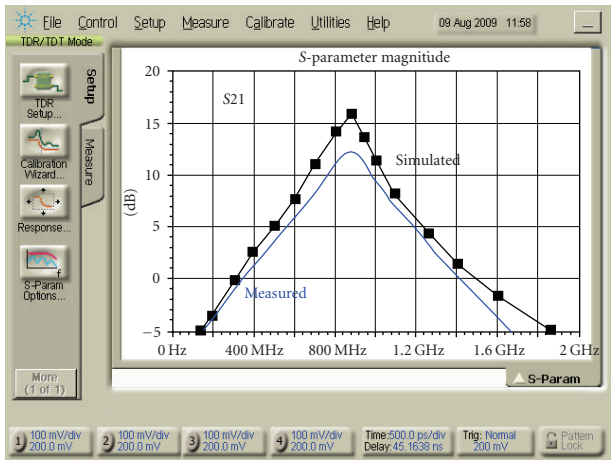

FIGURE 5: Forward gain, S_{21} (in dB) of the RFID LNA.

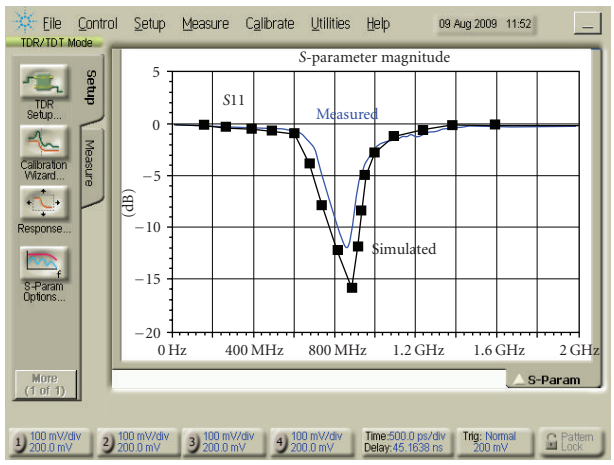

FIGURE 6: Input reflection coefficient, S_{21} (in dB) of the RFID LNA.

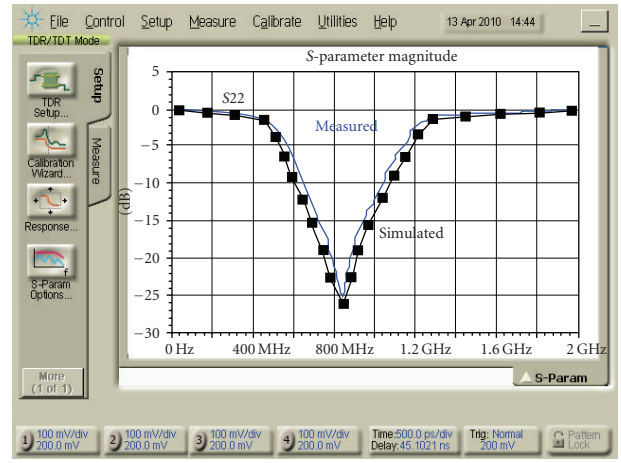

FIGURE 7: Output reflection coefficient, S_{22} (in dB) of the RFID LNA.

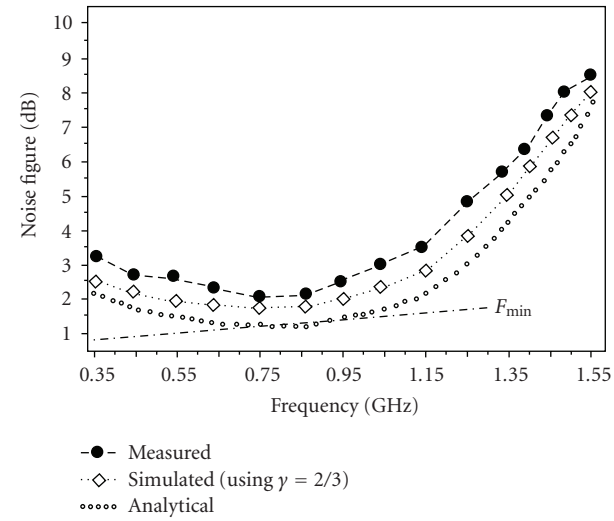

FIGURE 8: Noise figure (NF in dB) of the RFID LNA.

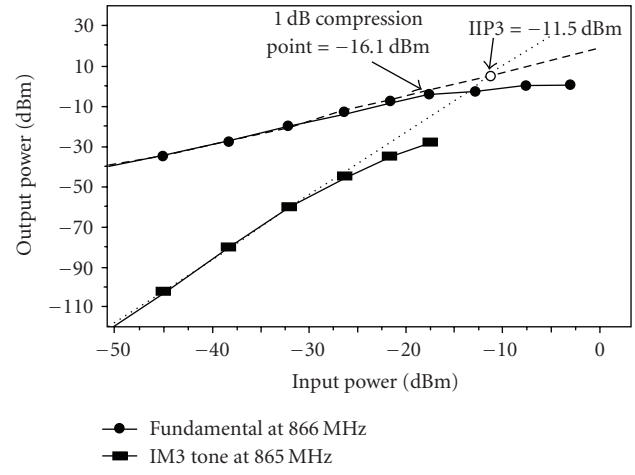

FIGURE 9: The IIP3 and 1 dB compression points for the UHF RFID LNA.

Table 1: Summary of the 866 MHz UHF RFID LNA performance and comparison with previous UHF LNA designs.

	This work	[1]	[2]	[3]	[4]	[5]	[7]
Technology (nm)	130	250	350	180	350	0.25	180
S_{11} (dB)	−12	−11.8	−10	−29	−14	−18	N/A
S_{21} (dB)	12	7.2	17.5	12.5	17	12	15
S_{12} (dB)	−34	−27.4	N/A	−60	−22	N/A	N/A
S_{22} (dB)	−25	−20	N/A	−33	N/A	N/A	N/A
NF (dB)	2.2	4.7	2	0.7	3.4	1.35	2.9
IIP3 (dBm)	−11.5	−1.8	−6	−4	−5.1	−4	N/A
P1dB (dBm)	−16.1	−9.3	N/A	−9	−23	−15	−15
P_{diss} (mW)	0.85	19.5	21.6	3.9	13	2	4.32
Supply Voltage (V)	0.7	2.5	2.7	1.8	2.3	1.25	1.8
f_0 (MHz)	866	900	900	915	900	900	900

output reflection coefficient S_{22} is measured to be ≈ -25 dB at 866 MHz as shown in Figure 7. These measurements were carried out using external matching elements and indicates close agreement with the simulation. All measurements include trace and connector losses. Figure 8 shows the comparison of the analytical, simulated and measured NF spectrum which verifies the close approximation provided by (3) due to the inclusion of the finite g_{ds} effect. The measured NF was around 2.2 dB. The IIP3 and the 1-dB compression points were determined to be −11.5 dBm and −16.1 dBm, respectively, as shown in Figure 9. Finally, Table 1 shows a summary of performance comparison of the proposed UHF LNA with other UHF LNA designs indicating the low NF achieved at sub-mW power.

4. Conclusion

The improved power constrained optimization of an UHF RFID LNA design at 866 MHz considering finite g_{ds} effects is presented and measurement results are demonstrated. The design achieves very low NF using only a 0.7 V supply voltage and consuming only 850 μW

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