

NANO-/MICRO METALLIC WIRE SYNTHESIS ON GaAs SUBSTRATE AND THEIR CHARACTERIZATION

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Nano-/micro wires of copper are grown on semiconducting GaAs substrate using the template method. It involves the irradiation of 8 μm thick polymeric layer coated on GaAs with 150 MeV Ni ion beam at a fluence of 2×10^8 . Later, by using the simple technique of electrodeposition, copper nano-/micro wires were grown via template synthesis. Synthesized wires were morphologically characterized using SEM and electrical characterization was carried out by finding I-V plot.

(Received September 2, 2011; accepted November 22, 2011)

Keywords: nanowires, GaAs

1. Introduction

Nano-/micro structures fabrication is not only of immense importance for the technology involved in electronics but also plays an important role for carrying out investigations relating to behavior of materials at sub-micron scales (1-4). A variety of possible applications based on microstructures include high-power microwave generation, ultra-fast computer and tera-hertz amplifier devices, radiation and temperature-insensitive electronics, field emitters, electrochemistry, conductive polymer nanofibres fabrication, transparent metal structures and macroscopic quantum tunneling phenomenon. Of the many possible geometrical shapes and growth patterns, the simplest structure is probably an ensemble of wires(5-9). A variety of techniques like optical, X-ray, electron and ion beam lithography have been used for fabrication of such ensembles. However, electrochemical methods involving electro deposition of metals into the etched pores of nuclear track filters (NTFs) of mica and polymers are convenient and simple techniques (9-16).

The template approach represents an interesting method for the preparation of nano/micro objects with controlled morphological properties mainly due to the fact that by appropriate choosing of host templates the shape and dimension of the prepared structures are precisely determined [17-19]. A type of templates which is widely used for such experiments is the nanoporous membranes. Most of the studies reported in literature are based on two types of such membranes: polymer ion track membranes and anodic alumina. Both present a number of advantages, which makes them suitable for the fabrication of high aspect ratio nanostructures, namely nanowires and nanotubes.

Here in the present work, an attempt is made to grow nanowires on the semiconducting substrate itself. Because of the wide applications of nanowires in electronics, it seems that the growth of metallic nanostructures on the semiconducting substrates themselves might found

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potential applications. However, template synthesis provides the most convenient route to this otherwise difficult task.

2. Experimental

The preparation of samples was carried out at Inter University Accelerator Center (IUAC), New Delhi, India, and the CSIO, Chandigarh, India. p-doped GaAs (111) was used as semi conducting substrate. To remove the dirt and oxide layer from the surface of GaAs substrate, wafer was dipped in trichloroethylene, acetone and methanol for 10 min each in succession followed by rinsing in 10% hydrochloric acid for 1 min. Finally, the wafer was rinsed with de-ionized water for 5 min. Using the technique of resistive heating, a thin layer of gold of thickness (ca. 95nm) was deposited on the wafers with 5×10^{-7} Torr pressure during deposition. Later on, a thin layer (10 μ m) of polycarbonate (Makrofol) was deposited onto the Au layer by spin coating. The adhesion of the polycarbonate film on the substrate was improved by the use of a primer (hexamethyldisilazane HDMS).

The prepared samples were irradiated at room temperature with 150 MeV Ni⁺¹¹ ions at a fluence of 2×10^8 using the ion beam facility at 15UD Pelletron accelerator IUAC, New Delhi, India. During irradiation, the samples were kept at room temperature and in vacuum of the order of 5×10^{-6} mbar.

Irradiated samples were then exposed to UV (365 nm, 150 W/cm²) so as to increase the selectivity of the chemical etching. Samples were then etched using 6N NaOH solution at room temperature under atmospheric pressure for 25mins in a home made one-compartment cell.

Aqueous CuSO₄.5H₂O (200 g/l) + H₂SO₄ (20 g/l) was used as electrolyte. The electrodeposition in a specially designed cell was carried out potentiostatically for 12 min at 0.8 V (current 0.0137–0.0140 A) under room temperature (nearly $25 \pm 2^\circ\text{C}$) and atmospheric pressure, with a pure copper sheet used as anode. After completion of electrodeposition, the electrolyte was drained out and the cathode flushed with 3% H₂SO₄, followed by Milli Q water rinsing and air-drying.

3. Results and discussion

For morphological characterization, the fabricated nano-/micro structures were viewed under scanning electron microscope using the SEM facility at SEMCF IIT New Delhi. Fig 1 (a) shows the image of the so-called pores generated and Fig 1(b) shows the image of the deposited nano/microstructures after the removal of polymeric layer. Electrical characterization of these structures was carried out by measuring the resistance across the filled membranes using simple two-probe technique. The *in-situ* I-V characteristics of nano-/micro structures was carried out at room temperature by leaving the structures embedded in the insulating template membrane itself. A KEITHLEY 2400 source meter was used for the measurement. Fig (2) shows the variation of current with applied voltage and fig (3) gives ln(I) vs V plot. It can be seen from fig (2) that the contact between semiconductor and the deposited copper metal shows schottky like behavior when forward biased. That indicates that system behaves non-ohmic when forward biased but in reverse biased region, I-V variation is ohmic. From Fig (2) Ohmic resistance in reverse biased region is around 517 ohms and the cut in voltage is around 0.68V.

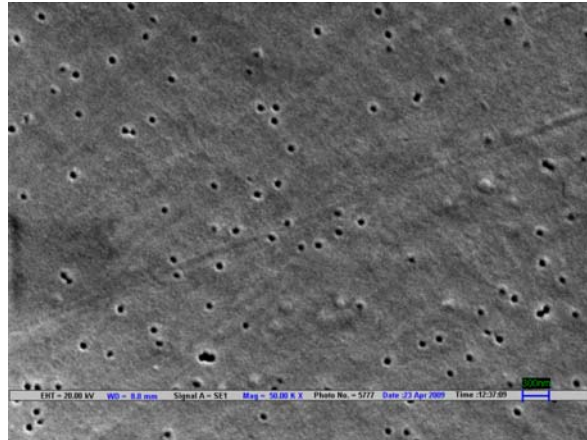


Fig. 1(a). SEM image of nanowires grown

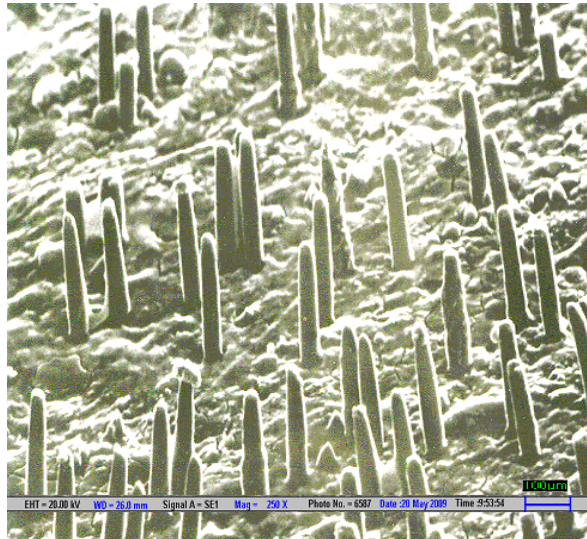


Fig. 1(b). SEM image of nanowires grown

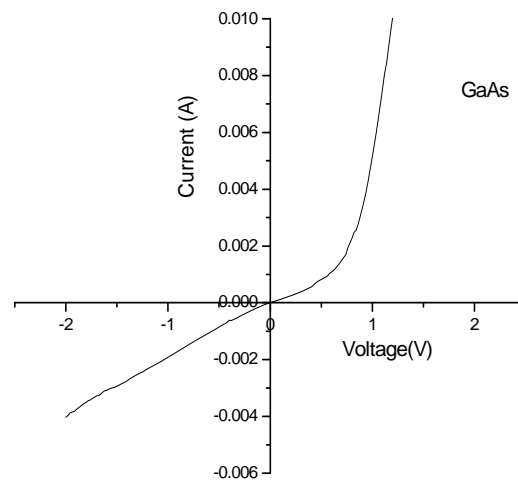


Fig. 2. IV characteristics of copper nano/micro wires deposited on GaAs

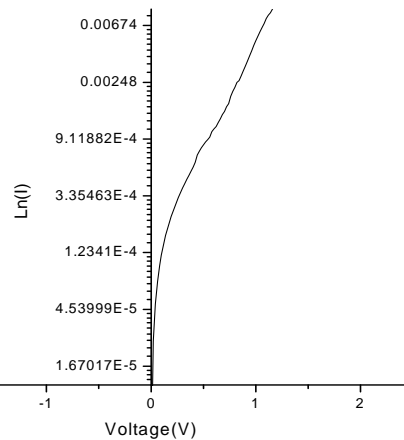


Fig. 3. $\ln(I)$ vs V plot for copper nano-/micro wires grown on GaAs substrate

At a metal- semiconductor contact, current varies according to the equation
Under the forward biased V at a fixed temperature

$$I = I_0[\exp\{(q(v-IR_s)/nkT)-1\}] \quad (1)$$

n is the ideality factor and R_s is the diode series resistance. For a pure thermionic emission $n=1$. Fit of linear region of the forward biased semilog IV curve (where $V > 3k_B T$ and R_s is negligible) the value of ideality factor and Schottky barrier height can be determined. Extrapolation of straight line portion of the plot to $V=0$ gives I_0 and the slope $S=d(\ln I)/dV$ gives n . Using I_0 barrier height may also be calculated using the equation

$$\Phi_B = (kT/q)(AA^*T^2/I_0)$$

Following equation (1), fig (3) shows that the saturation current for this system is about $1.1139E-4$ Amps with the slope (giving the value of ideality factor n) around 3.452. Higher ideality factor may result from the presence of nonlinear metal semiconductor contact.

Acknowledgement

The financial assistance to one of the author (Jaskiran Kaur) and heavy ion-irradiation facility provided by the IUAC, New Delhi is gratefully acknowledged. Thanks are also due to Dr Chatar Singh, IIT New Delhi for carrying out SEM analysis.

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