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VLSI HOTSPOT COOLING USING TWO-PHASE MICROCHANNEL CONVECTION

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ABSTRACT

Two-phase microchannel heat sinks are promising for the cooling of high power VLSI chips, in part because they can alleviate spatial temperature variations, or hotspots. Hotspots increase the maximum junction temperature for a given total chip power, thereby degrading electromigration reliability of interconnects and inducing strong variations in the signal delay on the chip. This work develops a modeling approach to determine the impact of conduction and convection on hotspot cooling for a VLSI chip attached to a microchannel heat sink. The calculation approach solves the steady-state two-dimensional heat conduction equations with boundary conditions of spatially varying heat transfer coefficient and water temperature profile. These boundary conditions are obtained from a one-dimensional homogeneous two-phase model developed in previous work, which has been experimentally verified through temperature distribution and total pressure drop measurements. The new simulation explores the effect of microchannels on hotspot alleviation for 20 mm × 20 mm silicon chips subjected to spatially varying heat generation totaling 150 W. The results indicate that a microchannel heat sink of thickness near 500 μm can yield far better temperature uniformity than a copper spreader of thickness 1.5 mm.

KEYWORDS

Microchannel heat sink, Two-phase flow, Hotspot

NOMENCLATURE

A_s	solid cross sectional area per channel pitch of microchannel heat sink, m^2
Bi	Biot number (=$H_c/R''_{TIM} k_c$)
D	hydraulic diameter of channels, m
Fr	Froude Number (=$m''^2/\rho_l g D$)
g	acceleration due to gravity, m/s^2
H	height of channels, m
H_c	thickness of the chip, m
H_s	thickness of the microchannel heat sink, m
$H_{s,e}$	effective thickness of the microchannel heat sink, m
H_{TIM}	thickness of thermal interface material, m
h_0	heat transfer coefficient , W/m^{2}K
$h_{0,eff}$	effective heat transfer coefficient, W/m^{2}K
i_f	fluid enthalpy, J/kg
k	thermal conductivity, W/mK
$\dot{m}$	mass flowrate, kg/s
m''	mass flux, kg/m^{2}s
p	perimeter of channel, m
Q	total applied heat generation, W
Q_1	heat generation in the upstream half of channels, W
Q_2	heat generation in the downstream half of channels, W
q''	heat flux, W/m^2
R_{eff}	effective thermal resistance, K/W
R''_{TIM}	thermal resistance of TIM, m^{2}K/W
T	temperature, K
w	pitch of channels, m

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x, y, z coordinates, m
Greek symbols
η_0 fin effectiveness
ρ_l liquid density, kg/m^3
Subscripts
avg average value
c silicon chip
f fluid
j junction
max maximum value
s microchannel heat sink
TIM thermal interface material

INTRODUCTION

The heat dissipation from high performance Very Large Scale Integration (VLSI) chips has been increasing rapidly and is expected to exceed 150 W from approximately a 3.5 cm^2 chip area by the year 2004, according to International Technology Roadmap for Semiconductors (ITRS) [1]. It is impractical to remove this large amount of heat from the chip with a conventional fin heat sink because of the associated large volume and weight. Besides the increase in the total rate of heat generation, hotspots arise from the localized power dissipation within the high performance logic circuit block. The nonuniform heat flux imposed by the presence of hotspots increases the peak junction temperature, which deteriorates the reliability and performance of the chip [2]. Advanced cooling solutions are needed to reduce junction temperature and to improve junction temperature uniformity. Microchannel heat sinks using two-phase forced convection are particularly promising because they occupy a small volume at the chip backside [3] and can improve the uniformity of junction temperatures [4]. There is little past work on the thermal performance of two-phase microchannel heat sinks with two-dimensionally varying heat generation.

Microchannel heat sinks received much attention after Tuckerman and Pease [5] demonstrated removal of 790 W/cm^2 using forced single-phase liquid convection. Peng et al. [6] investigated the flow and heat transfer characteristics in microchannels and reported distinct behavior of two-phase flow and flow transition. Stanley et al. [7] performed two-phase flow experiments in rectangular channels using inert gases mixed with liquid water and proposed a friction factor correlation for one-dimensional two-phase flow models. Zhang et al. [8] measured wall temperature distributions and pressure drops of single micromachined rectangular silicon/glass channels with hydraulic diameters ranging from 30 μm to 60 μm with nearly-constant heat flux conditions. Based on experimental observation, Zhang et al. [8] and Koo et al. [9] proposed that two-phase flow regimes in microchannels contain only the annular flow regime without bubbly and plug flow patterns. They developed a homogeneous two-phase flow model to calculate the pressure drop and wall temperatures and verified it through comparison with experimental data. Jiang et al. [3] demonstrated a closed-loop cooling system utilizing microchannel heat sinks, which were designed using a homogeneous two-phase model. They found that a careful design is important to avoid dry-out and high junction temperatures. Koo et al. [4] calculated the temperature field

and pressure drop along the channels of the heat sink subjected to one-dimensional nonuniform heat generation. They recommended that the heat sink be attached to the chip such that the hotspot is located near the exit of the channels to reduce the pressure drop along channels and the peak junction temperature. Two-dimensionally varying heat generation yields different flow conditions for each channel. The balance of the pressure drop dictates the distribution of the mass flow rate for each channel, which makes a two-dimensional model essential to simulate the effect of hotspots.

The present work addresses the challenges of removing highly nonuniform heat generation rates totaling 150 W from 20 mm × 20 mm silicon chips. A full chip thermal simulation approach solves the two-dimensional steady-state heat conduction equation, incorporating spatially varying heat transfer coefficients and water temperature profiles, obtained from the one-dimensional homogeneous model [9]. While the large thermal resistance of the single-phase region causes a high peak junction temperature, subchannels are incorporated to improve the heat sink performance. This study examines the effect of hotspot locations on the uniformity and the peak temperature of the junction. The simulated junction temperature field with the microchannel heat sink is compared with that of a conventional cooling system.

THEORETICAL APPROACH

Figure 1 shows schematics for a microchannel heat sink and a conventional copper thermal spreader implemented on top of a VLSI chip. The heat sink or thermal spreader is attached to the chip using a conventional thermal interface material (TIM). This configuration is relevant for a practical closed-loop cooling system that uses a novel electroosmotic pump [3]. This heat sink geometry is investigated in the present theoretical work.
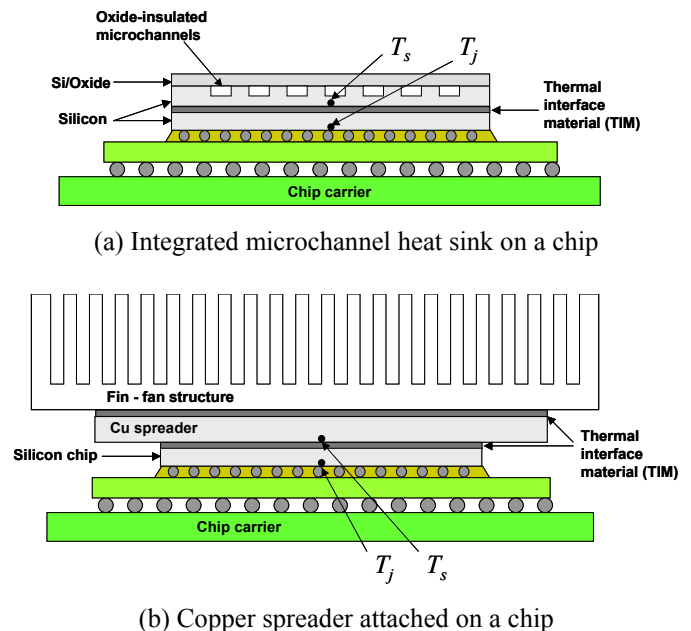

(a) Integrated microchannel heat sink on a chip

(b) Copper spreader attached on a chip

Figure 1   Schematics of a microchannel heat sink and a conventional spreader-fin heat sink integrated on top of a silicon chip.

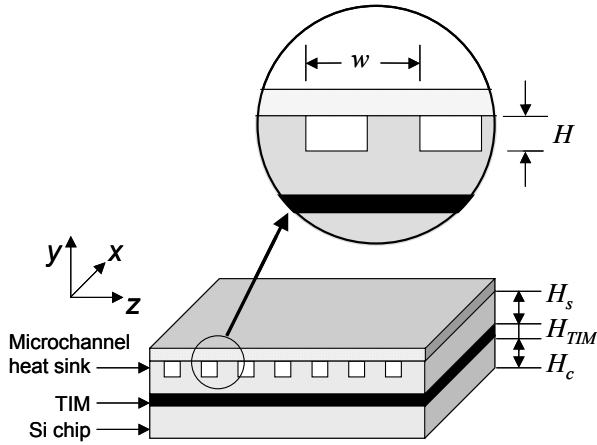2   Copyright © 2002 by ASME

Figure 2 Schematic of a two-phase microchannel heat sink mounted on a silicon chip.

Figure 2 assigns a coordinate system and establishes the critical dimensions to the chip structure. A nonuniform heat flux, q'', is generated by the junctions which are located at the bottom surface of the chip. The junction temperature field, which is strongly coupled to the working fluid temperature distribution, can be obtained by solving the two-dimensional conduction equations for the chip and the heat sink simultaneously, given by

Chip:
$$\frac{\partial}{\partial x}\left(k_c H_c \frac{\partial T_j}{\partial x}\right) + \frac{\partial}{\partial z}\left(k_c H_c \frac{\partial T_j}{\partial z}\right) + q'' - \frac{(T_j - T_s)}{R''_{TIM}} = 0 , \qquad (1)$$

Heat sink:
$$\frac{\partial}{\partial x}\left(k_s H_{s,e} \frac{\partial T_s}{\partial x}\right) + \frac{\partial}{\partial z}\left(k_s H_{s,e} \frac{\partial T_s}{\partial z}\right) + \frac{(T_j - T_s)}{R''_{TIM}} - h_{0,eff}(T_s - T_f) = 0 . \qquad (2)$$

The analysis employs the thermal lumped capacitance assumption in the y direction for each infinitesimal control volume of the chip and the heat sink, and assumes that the chip surface temperature is the same as the junction temperature. This assumption is valid if the Biot number, Bi, for the chip in the y direction, which incorporates the area normalized heat transfer coefficient to the working fluid, is much smaller than unity. Since the thermal resistance of the thermal interface material is orders of magnitude larger than the conduction thermal resistance of the silicon, this assumption is a reasonable approximation. The top surface of the microchannel heat sinks and all sides of the chip and heat sink are assumed to be adiabatic. The silicon chip thickness is H_c, and $H_{s,e}$ is the effective thickness of the microchannel heat sink ($= H_s - H$), where H is the height of the channels. Assuming that the temperature of the silicon wall between the channels is the same as that of the fluid, the effective heat transfer coefficient, can be calculated by using the relation, $h_{0,eff} = h_0 p/w$, where p is the perimeter of a channel and w is the pitch of channels. The thermal interface material has the homogeneous and isotropic thermal resistance, R''_{TIM}, defined as H_{TIM}/k_{TIM}.

The fluid temperature, T_f, can be obtained from the quasi-one-dimensional conjugate conduction/convection heat transfer analysis for each channel, while the convective heat transfer coefficient on the channel wall, h_0, is determined using Kandlikar's correlation [10]. In the analysis of the two-phase flow, liquid and vapor phases are assumed to be in equilibrium at the saturation temperature and pressure. The one-dimensional energy equations are

Solid:
$$\frac{d}{dx}\left(k_s A_s \frac{dT_s}{dx}\right) - \eta_0 h_0 p(T_s - T_f) + q''w = 0 , \qquad (3)$$

Fluid:
$$\dot{m}\frac{di_f}{dx} = \eta_0 h_0 p(T_s - T_f). \qquad (4)$$

The fin effectiveness, η_0, accounts for the temperature variation within the channel walls. This time- and space-averaged one-dimensional model considers the thermal conduction within the silicon wall and the forced convection within the channels. Two complimentary relations are required for the convective heat transfer coefficient and the pressure drop. For the single-phase flow region, they are evaluated from a correlation for a rectangular channel of a given aspect ratio. For the two-phase microchannel flow, Kandlikar's correlation [10] is employed to calculate the heat transfer coefficient, and the pressure drop is calculated using a homogeneous flow model with the friction factor proposed by Stanley et al. [7]. The friction factor correlation of Stanley et al. [7] has been experimentally determined for values of the two-phase Re including those relevant for the current work. However, Kandlikar's correlation was developed for values of Fr between 1.14 and 19.07 for two-phase horizontal flow, which is not representative of the values of Fr of about 0.98 in the present work. In applying this correlation for the present calculations, the relative importance of convective and boiling terms is shifted substantially, while it is assumed that they still capture the essential physics of the boiling process at the microscales. Future experimental work in this area will more closely examine the accuracy of this correlation at low Fr.

This calculation approach is applied to a nonhomogeneous heat flux boundary condition on a two-dimensional chip. First, the one-dimensional heat transfer model, Eqs. (3) and (4), is solved for two different channel locations on the chip. One of the channels is located directly on top of the hotspot region and the other channel does not pass the hotspot. The actual heat flux and heating area are estimated by considering thermal diffusion through the silicon chip and the thermal interface material for each channel. This model determines the mass flowrate distribution among channels by the requirement that the pressure drop is the same for both channels and the sum of the mass flow from all channels is equal to the total mass flowrate. This approximation may underestimate the heat diffusion in the z direction and may yield errors in chip temperature near the hotspot. Furthermore, using the heat transfer coefficient and fluid temperature obtained from the one-dimensional model, Eqs. (1) and (2) are solved simultaneously using the finite volume method.

To compare the performances between conventional and microchannel heat sinks, this study models the impact of

3

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microchannel cooling using an effective thermal resistance, which excludes the effect of other components of the cooling solution. The effective performance of heat sinks is strongly dependent on the thermal resistance of the thermal interface material and can be evaluated by the effective thermal resistance, defined as $R_{eff} = (T_{j,max} - T_{s,avg})/Q$. This resistance includes the thermal resistance of the chip and the thermal interface material, as well as the characteristics of the heat sink.

RESULTS AND DISCUSSION

This study addresses the specific solution of a closed-loop cooling system [3] removing 150 W from a chip with dimensions 20 mm × 20 mm × 750 μm. The working fluid is water and the liquid water flowrate for the entire channel array is 20 ml/min, which yields a quality of 0.20 at the exit of the heat sink. Our past experimental work has suggested that stable two-phase boiling can be achieved with this relatively low exit quality, and that dry-out can be prevented. The thermal interface material between the heat sink and the chip has a thermal conductivity of 2 W/mK and a thickness of 20 μm, which yields R''_{TIM} of 1×10^{-5} m²K/W. This thermal resistance strongly affects the ability of the heat sink to remove on-chip hotspots due to the large temperature difference across the interface. Reductions in the thermal interface resistance will result in improved hotspot cooling. Figure 3 shows the geometric configuration of a microchannel heat sink. The channel pitch is fixed at 800 μm and there are 25 channels. To avoid a large pressure drop, as well as to provide fabrication feasibility and mechanical strength of the chip, the channel depth is fixed at 300 μm. Koo et al. [4] showed that the pressure drop is the most important constraint to achieve a low and uniform junction temperature, and recommended use of larger channels to avoid large pressure drops. Channels with high aspect ratios, however, may induce flow instability due to the lateral variation of the flow and the relatively low value of viscous forces per unit volume. Considering this past work, the channel width and wall thickness are fixed at 700 μm and 100 μm, respectively. To simulate the sub-atmospheric operation, the exit pressure of the heat sink is set to 0.31 bar so that the water saturation temperature is about 70 °C. The inlet liquid temperature is fixed at 69 °C, assuming that the heat rejecter is capable of condensing the two-phase fluid.
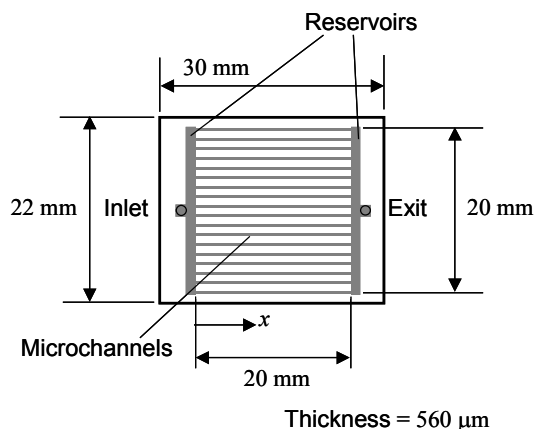

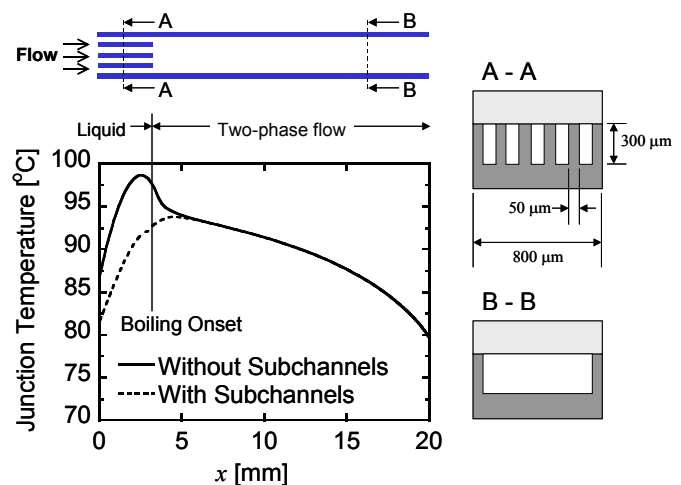Figure 3 Geometric configuration of a microchannel heat sink.

Figure 4 Effect of subchannels in the single-phase region on the junction temperature field. The microchannel is 700 μm wide and 300 μm deep. Each subchannel is 100 μm wide.

Subchannels in Single Phase Region

Figure 4 illustrates the typical junction temperature distribution in the flow direction when a uniform heat generation of 150 W is applied. The microchannel heat sink has a distinct characteristic of a nonuniform temperature distribution, even under the uniform heating condition, due to the single-phase region and the fluid saturation temperature variation in the two-phase region. The junction temperature has its peak in the single-phase region due to the relatively low heat transfer coefficient in this region compared to that in the two-phase region. To reduce the peak temperature in the single-phase region, the channel is divided into a finite number of sub-channels. Each of six subchannels is 100 μm wide and 3 mm long in the x-direction to cover the entire single-phase region. These subchannels increase the heat transfer coefficient and heat transfer area, which contribute to lowering the thermal resistance between the heat sink wall and the fluid. The following calculations include subchannels in the single-phase region to achieve better performance for the two-phase microchannel heat sinks.

One-Dimensional Nonuniform Heat Generation

This section examines the effect of one-dimensionally varying heat flux on the wall temperature of two-phase microchannel heat sinks. The wall temperature is a better representation of the thermal behavior of a microchannel heat sink than the junction temperature, since it does not include thermal diffusion through the thermal interface material and the chip. Figure 5 shows the wall temperature and pressure drop of a two-phase microchannel heat sink with respect to a fraction of the heat applied to the first half of the channel. The channel width is 700 μm and the channel wall thickness is 100 μm. Each channel incorporates the subchannels in the single-phase region to reduce the peak wall temperature. The amount of heat applied to the upstream half of the channel is Q_1, and Q_2 is to the downstream half. As Q_1 increases, the boiling onset is shifted towards the inlet, which causes a larger pressure drop due to the longer length of the two-phase region with a higher quality.

4

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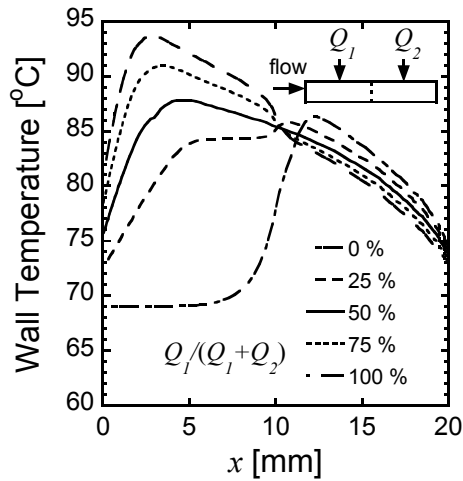
(a) Wall temperature distribution along the channel.
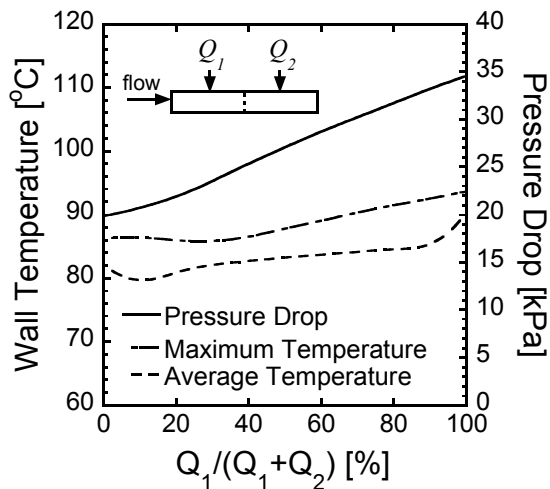
(b) Maximum and average wall temperature and pressure drop as a function of the fraction of heat applied to the first half of the channel.

Figure 5   Wall temperature and pressure drop of a microchannel heat sink with nonuniform heat generations. The heat sink has 25 channels 700 μm wide and 300 μm deep, and sub-channels in single-phase region. The total heat generation is 150 W.

The maximum and average temperatures tend to increase due to the overlap of the highest saturation temperature at the onset of boiling and the high heat flux in this region. The optimal thermal condition for one-dimensional heating is to apply about 10 % of the total heat to the first part of the channel, which acts as a preheating region followed by the high heat flux region.

Two-Dimensional Hotspot Simulation

To investigate the effect of the hotspot location, this work simulates two representative cases: a hotspot in the center and a hotspot in the corner. The chip size is 20 mm × 20 mm and the hotspot (core) size is 5 mm × 5 mm. The power in the core is 50 W while the power in the rest of the chip is 100 W. The balance of the pressure drop in each channel determines the
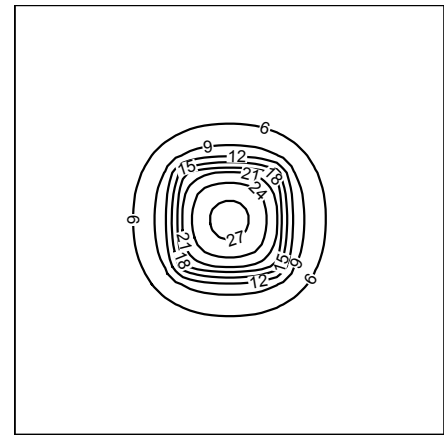
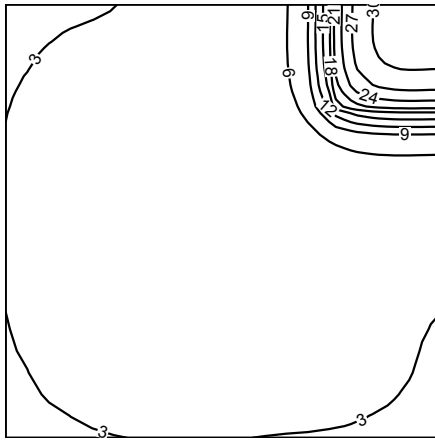(a) Conventional spreader-fin heat sink ($T_{j,max} - T_{s,avg}$ = 28 ^{o}C)
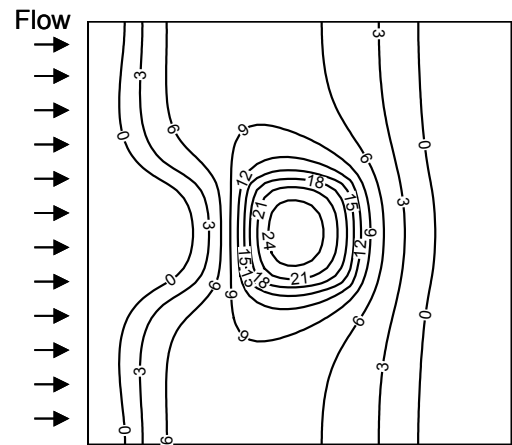
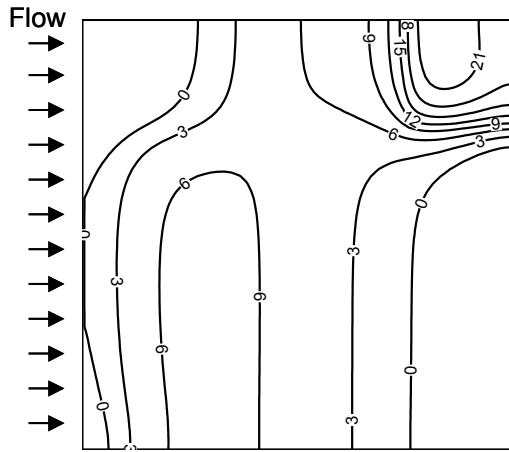(b) Microchannel heat sink ($T_{j,max} - T_{s,avg}$ = 26 ^{o}C)
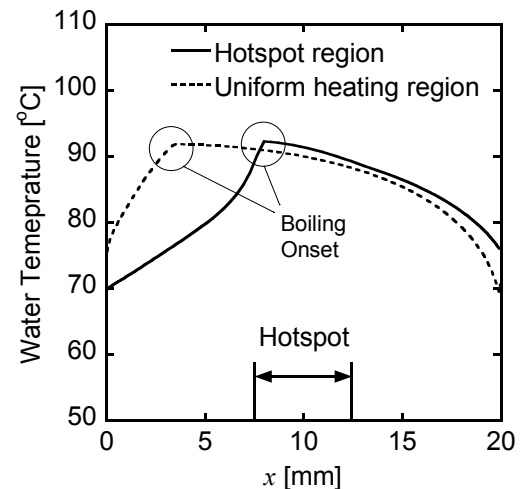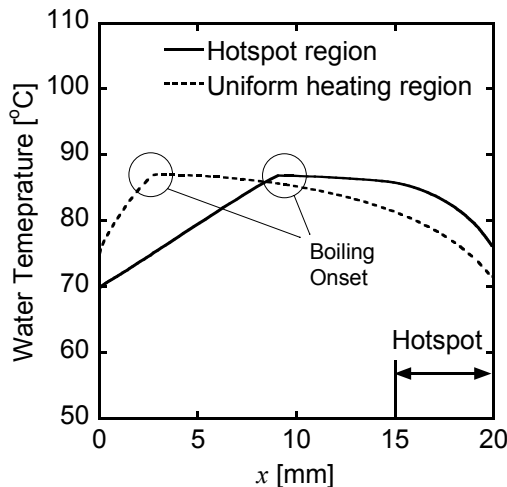

(c) Water temperature profiles along channels

Figure 6   Contours of the temperature difference between the junction and average surface of the heat sink with the hotspot at the center ($T_j - T_{s,avg}$). The water temperature profile is shown in (c) for two types of channels. The hotspot size is 5 mm × 5 mm. The temperature difference between the adjacent contour lines is 3 ^{o}C.

5   Copyright © 2002 by ASME

(a) Conventional spreader-fin heat sink ($T_{j,max}$ - $T_{s,avg}$ = 32 ^{o}C)

(b) Microchannel heat sink ($T_{j,max}$ - $T_{s,avg}$ = 23 ^{o}C)

(c) Water temperature profiles along channels

Figure 7 Contours of the temperature difference between the junction and average surface of the heat sink with the hotspot in the upper-right corner (T_j – $T_{s,avg}$). The water temperature profile is shown in (c) for two types of channels. The hotspot size is 5 mm × 5 mm. The temperature difference between the adjacent contour lines is 3 ^{o}C.

distribution of the mass flowrate between channels. When all of the channels have the same geometry, the channels on top of the hotspot region have less flowrate than everywhere else due to the large pressure drop. This reduction in flowrate may cause dry-out and failure of core circuit components due to high junction temperature. The present study optimizes the channel widths such that the channels in the hotspot region have more mass flux to ensure stable operations of the core.

A three-dimensional finite element simulation is performed using ANSYS to evaluate the thermal performance of a conventional heat sink under localized junction hotspots. For a conventional fin heat sink, shown in Figure 1(b), the properties of the thermal interface material are assumed to be the same as those for the microchannel heat sink. The dimensions of a copper heat spreader are 40 mm × 40 mm × 1.5 mm. The chip is attached to the center of the spreader. ANSYS calculates the temperature of the chip, the thermal interface material, and the spreader with a constant temperature boundary condition at the top surface of the spreader.

Figure 6(a) and (b) compares hotspot cooling performance of conventional and microchannel heat sinks, and shows the contours of the temperature difference between the junction and average surface of the heat sink when the hotspot is located at the center. Figure 6(c) plots the water temperature profiles along two channels: one in the hotspot region and the other in the uniform heating region. The channels in the hotspot region are 700 μm wide, while the rest of the channels are 300 μm wide. This channel configuration forces half of the mass flow into the hotspot region and yields a quality of about 0.2 at the exit of each channel. The water temperature increases in the single-phase region by sensible heat and then decreases in the two-phase region due to the large pressure drop. Because the mass flux is high in a small hotspot region, the channel with the hotspot has a delayed onset of boiling point. The pressure drop across the heat sink is about 45 kPa, which is rather large because the hotspot is not located at the exit, but at the center. The maximum junction temperature rises above the average heat sink temperature for conventional and microchannel heat sinks are 28 ^{o}C and 26 ^{o}C, respectively. The effective thermal resistances are 0.19 K/W and 0.17 K/W, respectively. The peak temperature rise with microchannels is not significantly reduced from that of the conventional heat sink because the hotspot is located at the center. For conventional heat sinks, placing the hotspot at the center can minimize the junction temperature rise due to thermal spreading through the silicon substrate. With microchannel heat sinks, however, the hotspot at the center applies high heat flux to the region where the fluid temperature is at its maximum, as shown in Figure 6(c), and causes a higher junction temperature than in the case where the hotspot is near the exit. A comparison between Figure 6(a) and (b) reveals that the microchannel heat sink has less steep temperature gradients near the hotspot.

The contour plots of the temperature difference between the junction and average surface of the heat sink are shown in Figure 7(a) and (b) when the hotspot is at the upper-right corner. Figure 7(c) illustrates the water temperature profile along channels. Channels in the hotspot region are 700 μm wide and the rest are 450 μm wide. With these channel geometries, half of the mass flows into the hotspot region at the

6

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corner, which yields a quality of around 0.2 at the exit of each channel. The pressure drop across the heat sink is about 32 kPa, which is much smaller than the previous case because the hotspot is located near the exit. The maximum junction temperature rises above the average heat sink temperature for conventional and microchannel heat sinks are 32 ^{o}C and 23 ^{o}C, which translate into effective thermal resistances of 0.21 K/W and 0.15 K/W, respectively. Due to the water temperature variation along the channel, as shown in Figure 7(c), the microchannel heat sink has intrinsic nonuniform temperature distributions. By taking advantage of this nonuniformity, locating the hotspot in the downstream part of the channels can minimize the pressure drop and the peak junction temperature. The temperature gradient near the hotspot is greatly reduced with microchannel heat sinks. With a conventional metal heat spreader and heat sink, the corner hotspot represents the worst case from a thermal standpoint because of the reduced thermal diffusion volume at the two sides. For the case of the microchannel heat sink, however, the corner hotspot can be readily accommodated due to the pressure dependence of the saturation temperature.

CONCLUSIONS

The present work develops a two-dimensional modeling approach to investigate the effect of microchannel heat sinks on the junction temperature distribution of a VLSI chip. The new simulation approach is used to explore the temperature field in 20 mm × 20 mm silicon chips experiencing highly nonuniform heat generation. The results show that the hotspot location has a significant impact on the junction temperature field and the pressure drop. The optimal thermal arrangement is to apply higher power at the exit region. The microchannels can reduce the peak junction temperature rise with respect to the average heat sink temperature by up to 30% compared with conventional copper spreaders. This result is achieved in part through the use of subchannels in the single-phase region to reduce the convective thermal resistance and junction temperature in this region. The subchannels impose a relatively small pressure drop in this region because of the low fluid velocity.

The present methodology is the basis for a compact and practical tool that can capture the multi-dimensional conjugate conduction/convection heat transfer behavior in high performance VLSI chips. Future work needs to investigate the dry-out conditions of two-phase flow in microchannels, which are critical in optimizing the mass flowrate distribution among the channels. Complete simulations incorporating two-phase flow and heat transfer calculation for every channel is needed to predict a more accurate temperature field of the chip and the heat sink.

ACKNOWLEDGMENTS

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