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Numerical Analysis of Coaxial Double Gate Schottky Barrier Carbon Nanotube Field Effect Transistors

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Abstract. Carbon nanotube field-effect transistors (CNTFETs) have been studied in recent years as a potential alternative to CMOS devices, because of the capability of ballistic transport. The ambipolar behavior of Schottky barrier CNTFETs limits the performance of these devices. A double gate design is proposed to suppress this behavior. In this structure the first gate located near the source contact controls carrier injection and the second gate located near the drain contact suppresses parasitic carrier injection. To avoid the ambipolar behavior it is necessary that the voltage of the second gate is higher or at least equal to the drain voltage. The behavior of these devices has been studied by solving the coupled Schrödinger-Poisson equation system. We investigated the effect of the second gate voltage on the performance of the device and finally the advantages and disadvantages of these options are discussed.

Keywords: carbon nanotube field effect transistor, ambipolar behavior, Schottky barrier, ballistic transport

1. Introduction

Carbon nanotubes (CNTs) have emerged as promising candidates for nanoscale field effect transistors. The contact between metal and CNT can be of Ohmic [1] or Schottky type [2–4]. Schottky contact CNTFETs operate by modulating the transmission coefficient of carriers through the Schottky barriers at the metal-CNT interface [4,5]. However, the ambipolar behavior limits the performance of these devices [2,6–8]. For suppressing this ambipolar behavior a double gate (DG) structure has been proposed [9]. Using this structure carrier injection at the source and drain contacts can be separately controlled. The behavior of a DG structure has been studied within the WKB approximation [9]. In this work the structure has been studied in more detail by numerically solving the coupled Schrödinger-Poisson equation system.

2. Approach

To account for the ballistic transport we solved the coupled Poisson and Schrödinger equations for the Schottky barrier CNTFET [10].

$$\frac{\partial^2 V}{\partial \rho^2} + \frac{1}{\rho}\frac{\partial V}{\partial \rho} + \frac{\partial^2 V}{\partial z^2} = -\frac{Q}{\epsilon} \quad (1)$$

$$-\frac{\hbar^2}{2m^*}\frac{\partial^2 \Psi^{n,p}_{s,d}}{\partial z^2} + (U^{n,p} - E)\Psi^{n,p}_{s,d} = 0 \quad (2)$$

We considered an azimuthal symmetric structure, in which the gate fully surrounds the CNT, such that the Poisson Eq. (1) is restricted to two-dimensions. In (1) $V(\rho, z)$ is the electrostatic potential, and Q is the space charge density.

In the Schrödinger Eq. (2) the effective mass was assumed to be $m^* = 0.06\ m_0$ [5] for both electrons and holes. Superscripts denote the type of the carriers. Subscripts denote the contacts, where s stands for the source contact and d for the drain contact. For example, Ψ_s^n is the wave function associated with electrons that have been injected from the source contact, and U^n is the potential energy that is seen by electrons. The Schrödinger equation is solved on the surface of the tube, and by assuming azimuthal symmetry, (2) is restricted to one-dimension.

The space charge density in (1) is calculated as:

$$Q = \frac{q(p-n)\delta(\rho - \rho_{\mathrm{cnt}})}{2\pi\rho} \tag{3}$$

where n and p are total electron and hole concentrations per unit length. In (3) δ/ρ is the Dirac delta function in cylindrical coordinates, implying that carriers are described by means of a sheet charge distributed uniformly over the circumference of the CNT [10]. Including the source and drain injection components, the total electron concentration in the CNT is calculated as:

$$n = \frac{4}{2\pi}\int f_s\left|\Psi_s^n\right|^2 dk_s + \frac{4}{2\pi}\int f_d\left|\Psi_d^n\right|^2 dk_d \tag{4}$$

where $f_{s,d}$ are equilibrium Fermi functions at the source and drain contacts. In this work we focus on ambipolar devices, where the metal Fermi level is located in the middle of the CNT band gap at each contact. All our calculations assume a CNT with 0.6 eV band gap, corresponding to a diameter of 1.4 nm [5]. The total hole concentration in the CNT is calculated analogously.

Current is calculated by means of the Landauer-Büttiker formula:

$$I^{n,p} = \frac{4q}{h}\int \left[f_s^{n,p}(E) - f_d^{n,p}(E)\right] TC^{n,p}(E)\,\mathrm{d}E \tag{5}$$

where $TC^{n,p}(E)$ are the transmission coefficients of electrons and holes through the device. The factor 4 in (4) and (5) stems from the twofold band and twofold spin degeneracy [4].

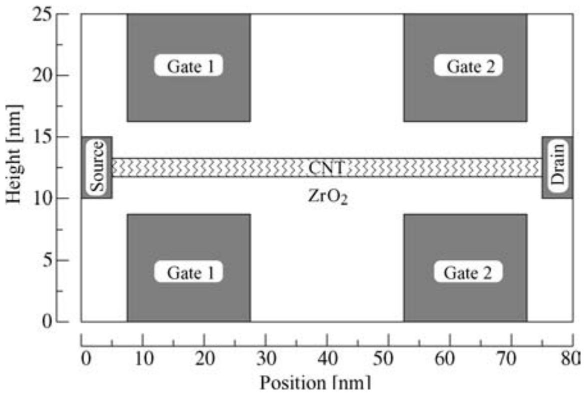

Figure 1. 2D Sketch of the coaxial DG structure.

The discussed model has been implemented in the device simulator MINIMOS-NT [11].

3. Double Gate Structure

To suppress the ambipolar behavior and improve the performance of CNTFETs, a DG structure as shown in Fig. 1 has been proposed [9]. In this structure the first gate controls carrier injection at the source contact and the second one controls carrier injection at the drain contact, which can be used to suppress parasitic current.

In order to suppress the ambipolar behavior it is necessary that the voltage of the second gate is equal or higher than the voltage of the drain contact [9]; therfore we consider two possibilities for the second gate voltage:

(a) Applying the same voltage as the drain voltage.
(b) Applying a constant voltage higher than the maximum drain voltage.

If the drain voltage is applied to the second gate, at any drain voltage the band edge profile near the drain contact will be flat, as shown Fig. 2. As a consequence the parasitic tunneling current of holes at the drain contact is suppressed and the parasitic current at the drain contact is limited to thermionic emission of holes, see Fig. 3.

Applying a voltage higher than the maximum drain voltage to the second gate (see Fig. 2) thermionic emission current of holes at the drain contact will decrease exponentially and consequently a lower parasitic current can be achieved, see Fig. 3.

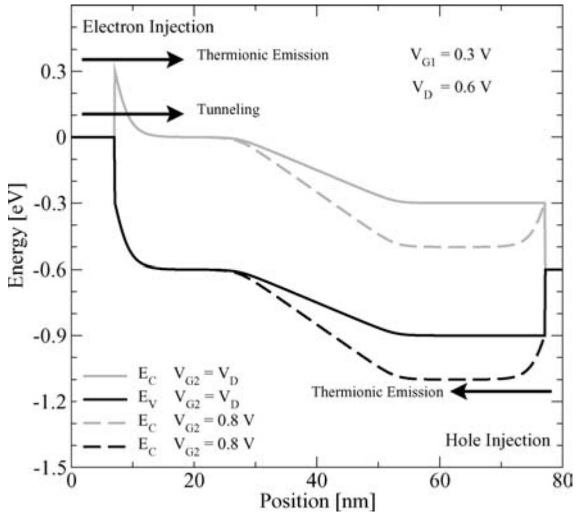

Figure 2. Band edge profile of the DG structure.

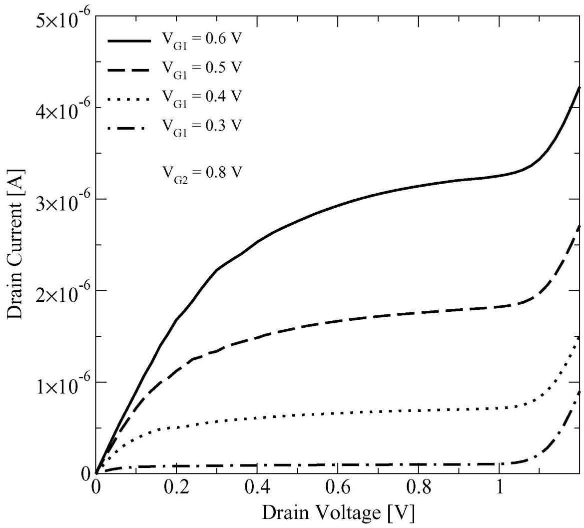

Figure 4. Output characteristics of the DG structure.

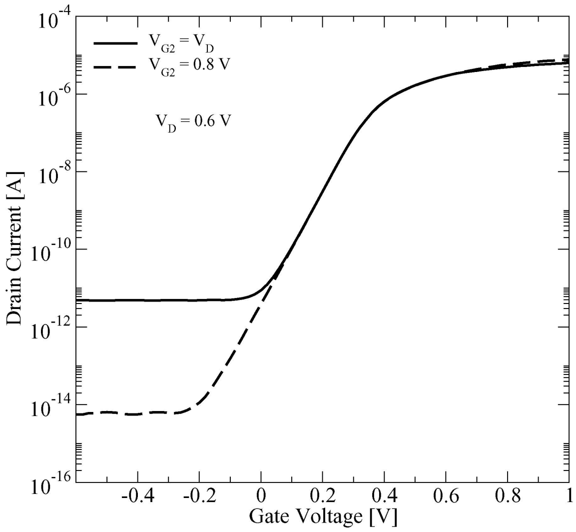

Figure 3. Transfer characteristics of the DG structure.

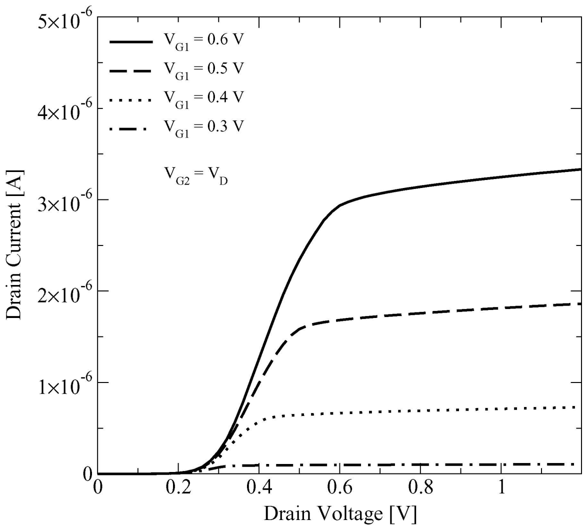

Figure 5. Output characteristics of the DG structure.

The output characteristics of the DG structure for these two options are shown in Figs. 4 and 5. As shown in Fig. 4, when the drain voltage reaches a voltage higher than the second gate voltage, a parasitic current emerges. The reason of this behavior is that at these drain voltages, the barrier for holes at the drain contact is suppressed (see Fig. 6) and as a result the tunneling current of holes increases.

If the second gate is biased at the drain voltage, at any drain voltage the band edge profile near the drain contact is flat (see Fig. 6) and the parasitic current at any drain voltage is limited to the negligible thermionic emission current of holes, but as shown in Fig. 5 the drain current will be small until the drain voltage reaches the first gate voltage. The reason of this behavior is that injected carriers from the source have to overcome a thick barrier near the drain until the drain voltage reaches a voltage higher than the first gate voltage, see Fig. 7. If the second gate is biased at a voltage higher than the maximum drain voltage,

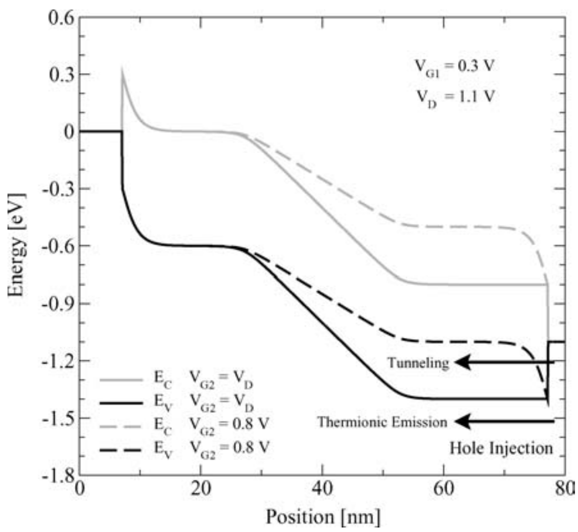

Figure 6. Band edge profile of the DG structures.

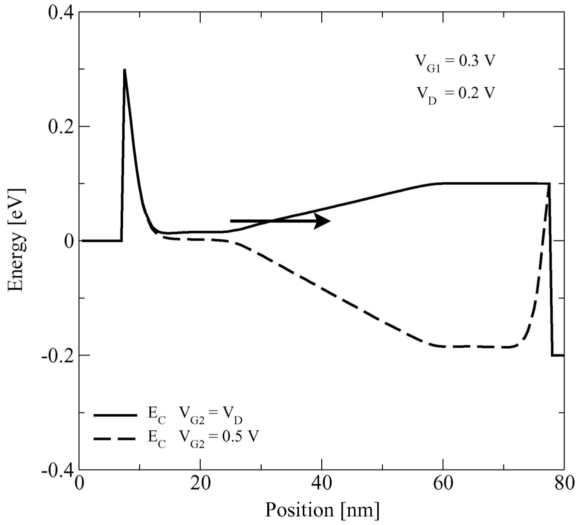

Figure 7. Conduction band edge profile of the DG structures.

injected carriers from the source have to overcome a thin barrier even at low drain voltages.

4. Conclusion

We showed that in a DG structure the first gate controls carrier injection at the source contact and the second gate suppresses parasitic carrier injection at the drain contact. We considered the cases where either the drain voltage or a constant voltage higher than the maximum drain voltage are applied to the second gate. It is of advantage to apply the drain voltage to the second gate, because parasitic capacitances between the second gate and the drain contact are avoided, no separate voltage source for the second gate is needed, and the fabrication is more feasible. The off-current is limited to the thermionic emission current over the Schottky barrier. The drain current, however, is small until the drain voltage reaches a voltage higher than the first gate voltage. By applying a voltage higher than the maximum drain voltage to the second gate, a high I_{on}/I_{off} ratio can be obtained. However, for both of these methods the I_{on}/I_{off} ratio exceeds five orders of magnitude which is satisfactory for conventional logic applications.

Acknowledgments

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References

1. A. Javey et al., "Ballistic carbon nanotube field-effect transistors," *Letters to Nature*, **424**(6949), 654 (2003).
2. R. Martel et al., "Ambipolar electrical transport in semiconducting single-wall carbon nanotubes," *Physical Review Letters,* **87**, 256805 (2001).
3. J. Appenzeller et al., "Field-modulated carrier transport in carbon nanotube transistors," *Physical Review Letters*, **89**, 126801 (2002).
4. S. Heinze et al., "Carbon nanotubes as schottky barrier transistors," *Physical Review Letters* **89**, 106801 (2002).
5. J. Appenzeller et al., "Tunneling versus thermionic emission in one-dimensional semiconductors," *Physical Review Letters*, **92**, 048301 (2004).
6. M. Radosavljevic et al., "Drain voltage scaling in carbon nanotube transistors," *Appl. Phys. Lett.*, **83**(12), 2435 (2003).
7. J. Guo et al., "A numerical study of scaling issues for schottky barrier carbon nanotube transistors," *IEEE Trans. Electron Devices*, **51**(2), 172 (2004).
8. J. Clifford et al., "Bipolar conduction and drain-induced barrier thinning in carbon nanotube FETs," *IEEE Trans. Nanotechnology*, **2**(3), 181 (2003).
9. M. Pourfath et al., "Improving the ambipolar behavior of schottky barrier carbon nanotube field effect transistors," in *Proc. ESSDERC* (2004), p. 429.
10. D. John et al., "A schrödinger-poisson solver for modeling carbon nanotube FETs," in *Proc. NSTI Nanotech* (2004), p. 65.
11. Technische Universität Wien, Austria, *MINIMOS-NT 2.1 User's Guide* (2004).