A Dynamic-Logic Frequency Divider for 5-GHz WLAN Frequency Synthesizer

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Abstract. *A dynamic-logic frequency divider for fully integrated CMOS frequency synthesizer is presented in this paper. The divider based on the dual-modulus prescaler and dynamic logic circuit is designed to reduce the power consumption, transistor-counts, and chip area. The simulation results show the proposed circuit achieved the operating frequency band from 5.15GHz to 5.825GHz for wireless local area network applications. Under 1.8V supply voltage, it consumes only 3.6mW and occupies a chip area of 0.285mm^2.*

Keywords

Divider, dynamic-logic, dual-modulus prescaler, frequency synthesizer.

1. Introduction

IEEE 802.11a and HiperLAN are standards of wireless data networks with frequency band operated from 5 to 6GHz which covers fifteen channels with a channel spacing of 20MHz [1]. The frequency synthesizers are widely used to generate local oscillation (LO) signals in modern communication systems. In order to cover the required carries and operate from input frequency of 5GHz, the division of the divider has to be programmed from 257 to 294. The operating frequency of a frequency synthesizer is limited by the frequency divider as well as the voltage-controlled oscillator (VCO). For WLAN standard, most common high-speed frequency are based on a pulse-swallow architecture [2-6]. It usually comprises of a dual-modulus prescaler (DMP), a 6-bits pulse (P) counter, and a 5-bits sallower (S) counter. Two counters generate the given division ration of divider and divide-by-value of DMP. To keep up with the high input frequency and reduce the power consumption, the DMP is a trade-off between the speed and divide-by-value. On the other hand, the architectures require two additional counters for generation of a desired division ratio. It occupies many gate-counts, large chip area, and consumes extra power. This paper proposes a new frequency divider keeping the same function as a conventional one without employing a sallower counter to consume takes extra power and unnecessary chip area.

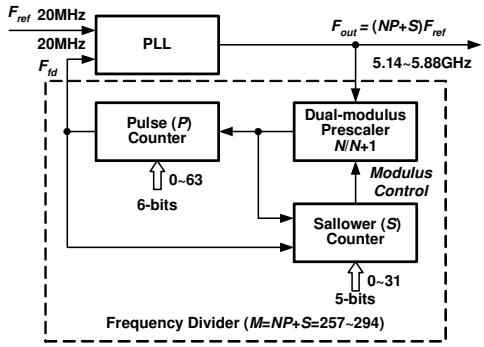


Fig. 1. Block diagram of the conventional DMP divider.

2. Frequency Divider Architecture

2.1 Pulse-Swallow Architecture

Fig. 1 shows the divider architecture based on a pulse-swallow topology. The DMP initially divides the high frequency input by $N + 1$ with the *Modulus* signal being LOW. After the sallower-counter counts S output pulses from DMP, it changes the signal *Modulus* to HIGH, and the DMP starts to divide by N. The output of DMP is also counted by the pulse-counter simultaneously. The pulse-counter resets the sallower-counter after the output pulsing. Therefore, the total division ratio is given by the following

$$M = [(N+1)S + N(P-S)] = (NP+S) \tag{1}$$

where N is the divided number of DMP, P is the number of the pulse-counter, and S is the number of the sallower-counter. For the WLAN standard, the frequencies are divided into two band groups. In low band (5.15GHz-5.35GHz), P and N are set to be 32 and 8, respectively. While S is set to be among 1 to 12, the total division ratio is from 257 to 268 with a step of 1. On the other hand, in the higher band (5.725GHz-5.825GHz), P is set to be 34, while S is set to be among 13 to 22. The total division ratio is from 285 to 294. It is noticed that the architecture in

Fig. 1 has some considerable drawbacks. The conventional frequency divider requires two additional counters for generating a given division ratio. In order to cover a wider LO frequency range, the pulse counter must expand one more bit which causes the extra chip area and the power dissipation.

2.2 Proposed Frequency Divider Architecture

The high power consumption is mainly due to the first stages of the frequency divider that often consumes half of the total power. The first stage of the divider cannot be implemented in dynamic TSPC circuit. In order to relax the speed constraints of DMP, its input frequency is first halved by a divide-by-2 prescaler with a differential source-coupled logic (SCL) [7-8]. This solution forces to reduce the reference frequency to half the channel spacing, ie.,10MHz.

The proposed topology is based on the counter-less and dual-modulus counter detector, as shown in Fig. 2. The frequency divider eliminates two counters and replaces by a divide-by-32/34 DMP_2, a dual-modulus counter detector, a sallower-counter detector, and a JK flip-flop (JK-FF). DMP_2 is connected directly to both the dual-modulus counter detector and sallower-counter detector. The outputs of two detectors are connected to *J* and *K* input of JK-FF, respectively. DMP_2 initially divides the input of DMP_1 by 32 or 34 with the signal *Band* being HIGH or LOW. After the dual-modulus counter detector counts *S* output pulses from DMP_2, it changes the signal *Modulus* to HIGH and the DMP_1 starts to count by *N*. Since *S* is smaller than *P*, the DMP_2 always counts *S* first. It is noticed that the sallower-counter detector can detect *S* by the DMP_2 without employing a sallower-counter.

According to (1), the total division ratio is modified by the following

$$M = 2[(N+1)S + N(P-S)] = 2(NP+S). \quad (2)$$

where *N* is the divided number of DMP_1, *P* is the number of the dual-modulus counter detector, and *S* is the number of the sallower-counter detector. While *N* is set to be 8, the total division ratio is from 514 to 536 with a step of 2.

3. Frequency Divider Building Block

3.1 Divide-by-8/9 Dual-Modulus Prescaler

Fig.3 shows the divide-by-8/9 DMP are realized in TSPC logic [9]. It consists of a divide-by-2/3 synchronous divider, a divide-by-4 asynchronous divider, and a control qualifier which control the division of DMP. To achieve faster operation of the high-speed divide-by-2/3 used in DMP, a TSPC D-flip-flop with an embedded NAND gate is used as shown in Fig. 4 [10].

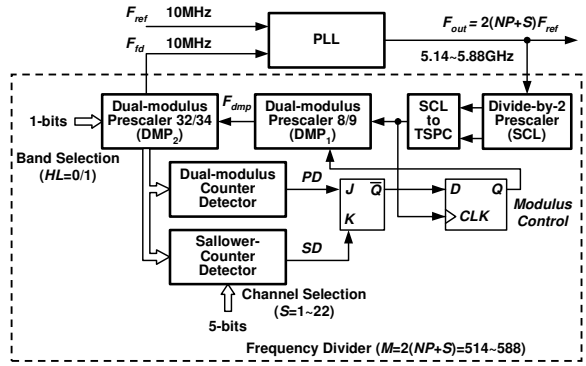


Fig. 2. Block diagram of the proposed DMP divider.

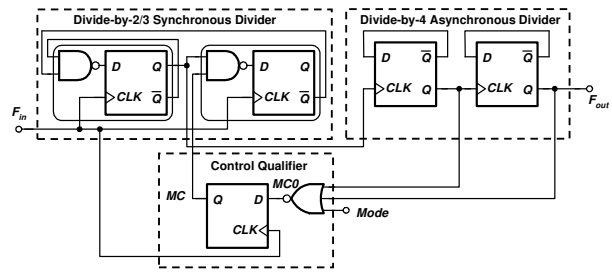


Fig. 3. Dual-modulus divide-by-8/9 DMP.

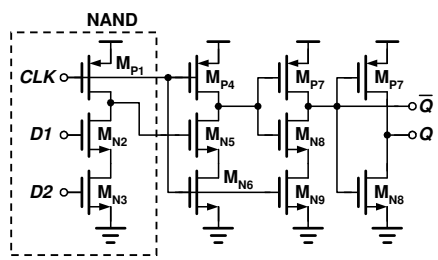


Fig. 4. Schematic of D-flip-flop with embedded NAND gate.

3.2 Divide-by-32/34 Dual-Modulus Prescaler

Fig.5 shows the proposed divide-by-32/34 DMP. It consists of a divide-by-2 divider, a divide-by-2/3 synchronous divider, a divide-by-4 asynchronous divider, and a control qualifier which control the division of DMP. The DFF of control qualifier is controlled by a positive-pulse of the first divide-by-2 stage to allow pipelining of the DMP modulus control signal.

3.3 Dual-Modulus Counter Detector

Fig. 5 shows proposed dual-modulus counter detector which comprises of four positive-edge triggered AND gates. A traditional AND circuit can help prevent excessive jitter, which would result in phase noise at the synthesizer output. DMP_2 is equal to the synchronous down counter which achieves a complete transition faster. Each stage output of the DMP_2 connected to the positive-edge triggered AND [11]. The output of the first divide-by-2 stage triggers each AND, and determines whether the AND changes. Thus, this detector that change on a given clock change almost simultaneously.

The positive-edge triggered AND gate of Fig. 6 operates as follows. When the clock signal *CLK* is LOW, two inputs are isolated from the output *OP*. When *CLK* is HIGH, node *X* is equal to the output of NAND gate. Then, the output *OP* is inversed the node *X*. In order to achieve faster operation and stabilize the node *OP*, the transistor M_9 is connected between node *X* and *OP* [12].

3.4 Sallower-Counter Detector

The proposed sallower-counter detector which is programmed by 5-bits control circuits is shown in Fig.5. It consists of five XNOR gates, and four positive-edge triggered AND gates. Similar observations can be made for the dual-modulus counter detector. The outputs of two detectors are connected to *J* and *K* input of JK-FF, respectively. Thus, two detectors that control the JK-FF on a given clock change almost simultaneously.

4. Frequency Divider Building Block

The proposed frequency divider is designed by 0.18μm CMOS process with 1.8V supply voltage.

4.1 Proposed Divide-by-32/34 DMP

The transient simulation waveforms of the DMP_2 are shown in Fig. 7. Under input clock frequency is 400MHz and the amplitude is $0.9V_{p\text{-}p}$, the output amplitude of each phase clock signal is $1.5V_{p\text{-}p}$. It can be seen from Fig. 7 that the division ratio is 34 when the input *Band* is LOW and *MC* generates a pulse. On the other hand, the division ratio is 32 when the input *Band* is HIGH and *MC* has no pulse.

4.2 Proposed DMP Divide

When an input signal with a 5.88GHz frequency is applied to the divider circuit, the simulation output waveform of the divider is shown in Fig. 8. When the division ratio of DMP_2 is 34 with the signal *Band* being LOW, the signal *Mode* is set to be LOW and the division ratio of DMP_1 is 9 until DMP_2 counts 21. When DMP_2 counts 21, it is observed that *PD* is LOW and *SD* is HIGH. Hence, the output *Modulus* of JK-FF turns to be HIGH and the division ratio of DMP_1 turns to be 8. When the DMP_2 counts 22, both the input signals of JK-FF are LOW and hold the state of JK-FF. This state will be remained until DMP_2 counts 34. When DMP_2 counts 34, *PD* is HIGH and *SD* is LOW. So JK-FF sets *Modulus* to be LOW and the division ratio of DMP_1 turns to be 9. At this moment, DMP_2 is reset and the dividing cycle repeats. The division ratio is selected by six digital bits, S_0, S_1, S_2, S_3, S_4, and *Band*. According to (1), the total division ratio is 588. In the post-layout simulation, for PVT conditions, the proposed divider achieves a maximum operating frequency of 6GHz and consumes about 3.6 mW. Fig. 9 shows the

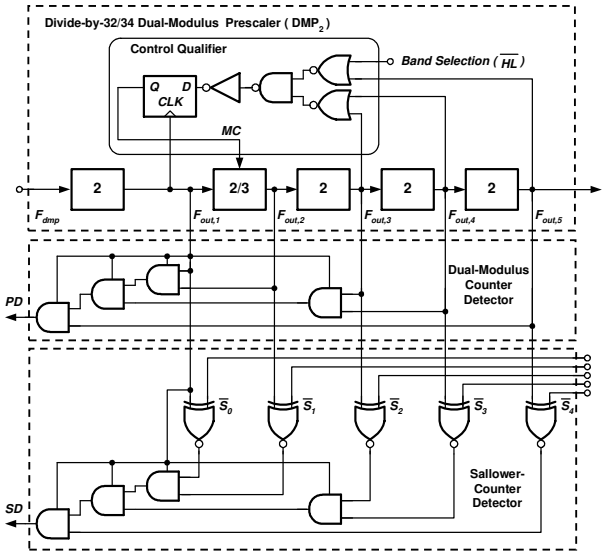
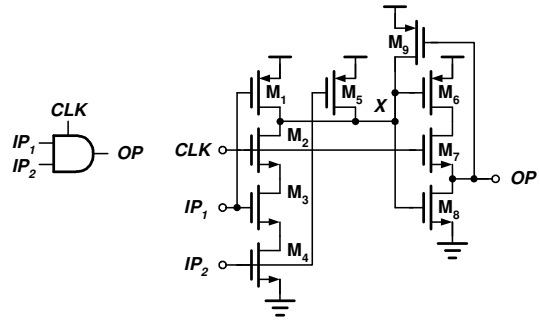


Fig. 5. Proposed divide-by-32/34 DMP, a dual-modulus counter detector, and a sallower-counter detector.



(a) (b)

Fig. 6. Positive-edge triggered AND gate.

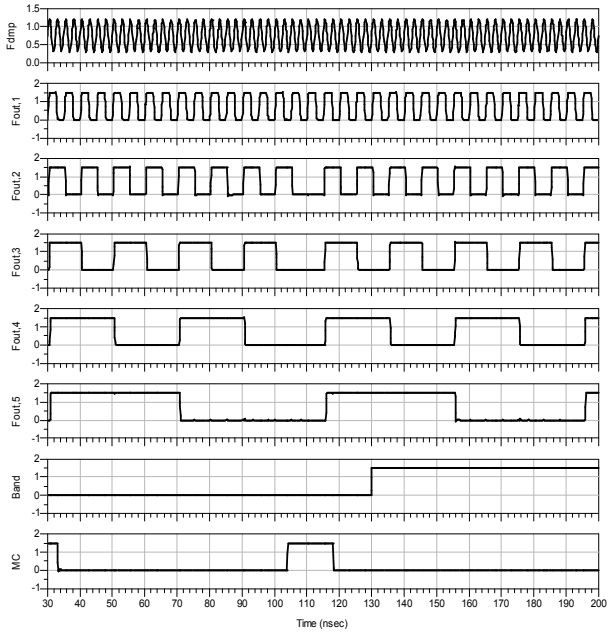


Fig. 7. Transient simulation waveforms of the proposed DMP_2.

chip area is 536 x 531 μm^2. The proposed divider is summarized in Tab. 1 with a conventional divider for comparison.

5. Conclusion

A simple architecture of the dynamic-logic frequency divider has been demonstrated in a standard 0.18μm CMOS technology. The frequency divider is designed without counters and the simulation results show the advantages in low power consumption and less chip area. The proposed frequency divider achieves the operating frequency bands form 5.15GHz and 5.825GHz in steps of 20MHz, which covers 15 channels in WLAN applications.

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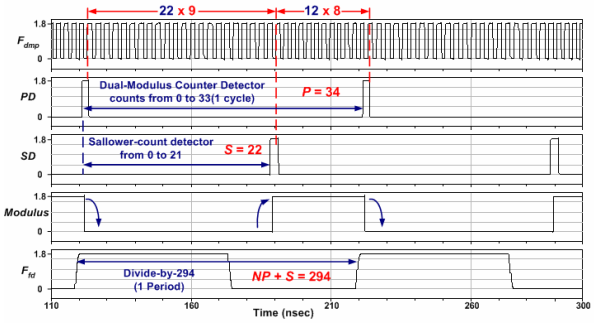

Fig. 8. Transient simulation waveforms of the proposed divider.

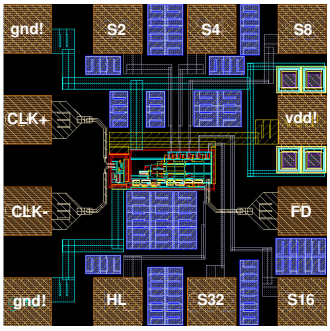

Fig. 9. Chip layout of the proposed frequency divider.

Design	[4]	[5]	[6]	Proposed
Process (μm)	0.18	0.18	0.18	0.18
Voltage (V)	1.8	1.8	1.8	1.8
Frequency (GHz)	2	3	6.3	6
Division Ratio	32/33	1920~1984	16/20	514~588
Power (mW)	4.7	5.4	6.7	3.6
Chip Area (μm^2)	300 x 400	N/A	N/A	536 x 531

Tab. 1. Summary and comparison table.