THE IDENTIFICATION AND ANALYSIS OF LATENT ESD DAMAGE ON CMOS INPUT GATES

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Abstract

Latent electrostatic discharge (LESD) damage sites are normally identified and analyzed after the damaged oxide has been transformed from a low to a high level leakage. Failure analys[i]is typically focuses only on the primary rupture site, neglecting the remaining LESD damage sites. The purpose of this work is to present a new method of analysis which allows compromised oxides to be rapidly identified and then show the existence of multiple LESD damage sites. Images from the Scanning Electron Microscope and the Atomic Force Microscope associated with the LESD damage sites are compared.

1. Introduction

In this paper, two types of gate oxide integrity defects will be discussed. The first is associated with LESD on input pins creating a walking-wounded phenomenon. The second is associated with fabricated oxide defects which can result in abnormal I_{CC} standby current values and/or functional failures with the device. Both types of defects have latency associated with them that can result in failure. The work in this paper will focus on input leakage. Several analysis tools which are *common* for the analysis of ESD, as well as fabricated oxide defects are: liquid crystal hot spot analysis, emission microscopy, and passive voltage contrast. A new method to identify compromised gate oxide has been developed and is called oxide noise signature analysis. This method allows rapid identification of compromised oxides associated with a failing device using a constant current source to bias the device, either in an I_{CC} standby mode, or by biasing directly a suspect pin. The resulting voltage on that pin is used to measure stability under constant current. If this voltage manifests itself as a particular type of audio noise, then this noise is a signature that there is compromised gate oxide.

The instabilities of oxide integrity defects will be characterized and shown to be time variant leakage failures prior to reaching TDDB (Time Dependent Oxide Breakdown). In some cases, a damaged oxide can actually be bake-recovered and/or temperature cycle recovered to a much lower leakage level, typically by a factor of 50. Analysis of the bake recovered oxide will be performed with the Emission Microscope and Passive Voltage Contrast (PVC) techniques.[1] Correlation with Scanning Electron Microscopy (SEM) and Atomic Force Microscopy (AFM) analysis will be made after deprocessing multiple damage sites.

2. Oxide Noise Signature Analysis

Oxides which have been damaged and leak, but have not been overstressed to the point of a resistive short, have a characteristic noise signature which can be identified with a simple constant current source. Using an off-the-shelf operational amplifier, (the OPO7C amplifier from Texas Instruments), and a common depletion mode field effect transistor, a simple constant current source with rapid response time can be constructed for the purpose of biasing the pin or device to be tested. Figure 1 is a schematic diagram of the Oxide Noise Signature circuit.
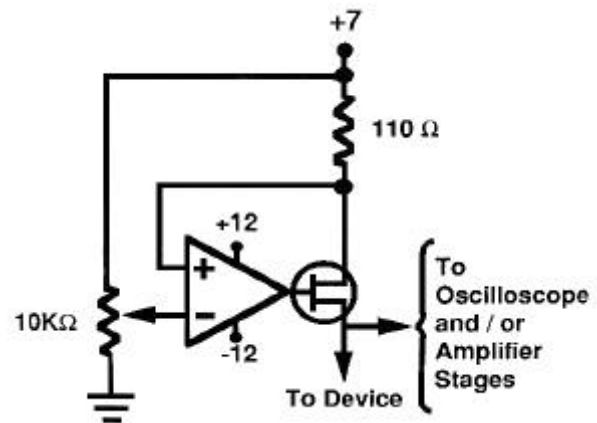

Figure 1 Schematic diagram of the constant current source for oxide noise detection.

A pin which has an oxide noise signature associated with it will exhibit anywhere from ±20 to ±200 mV of band limited noise; typically less than 20 kHz in frequency. The signal can be amplified through subsequent op/amp stages or it can be viewed directly on an oscilloscope with AC coupling. AC coupling is necessary due to the instability of the oxide, which causes fluctuations in the DC value as well as the AC components.

Damaged oxides, which have not been electrically overstressed, act very much as spark gaps. The resultant oxide noise signature (ONS) is easy to identify against the background noise as shown in photo 1.

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[1] EOS/ESD Symposium 1993 p. 109
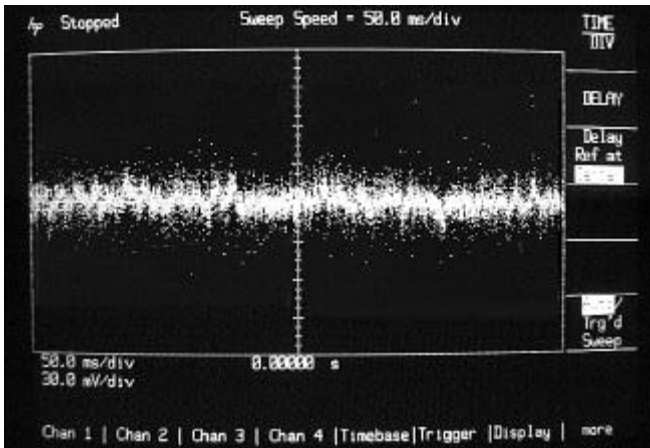
Photo 1 is from a Digital Oscilloscope connected to the pin leakage.
Notice that some of the noise peaks are as high as 90 mV
for an input pin with compromised gate oxide.

The signal was amplified with subsequent op/amp stages and fed into the external input of the slow scan camera of the SEM without synchronization. Photo 2 shows a failing input with an evident oxide noise type signature. A normal input is shown in photo 3. The vertical band in photos 2 and 3 is a 60 Hz artifact associated with shielding issues and can be ignored.


Photo 2 Typical Oxide Noise Signature associated with an input pin leakage of 220 nA at 6 Volts. Slow scan rate is 30 seconds.
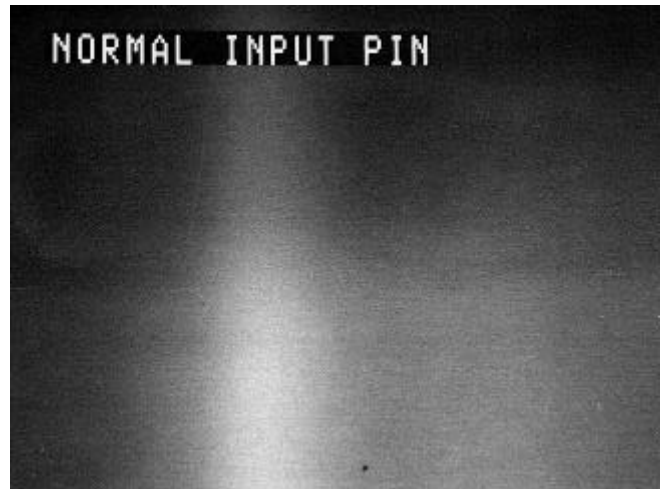

Photo 3 The Oxide Noise Signature is absent on input pins without leakage at 6 Volts. Slow scan rate is 30 seconds.

A spectrum analyzer was utilized to view the audio spectrum of this oxide noise, (see Photo 4). Notice that frequencies below 100 Hz are heavily attenuated due to AC coupling and that the spectrum rolls off gradually after 2000 Hz.

If the laboratory is equipped with OBIC (Optical Beam Induced Current) measurement techniques, or CIVA[2] (Charge Induced Voltage Alteration) the same goals may be accomplished; in the case of OBIC, by simply biasing the device with the OBIC source and measuring the change in current values as monitored on the screen.[3] Since OBIC is designed to measure minute changes in current through a current amplifier, the results are the same; the image is filled with noise. Photo 5 is an OBIC image of the noise signature. The inset is an image integrated scan of a known oxide integrity defect. Nothing was obtainable through the OBIC signal besides the noise signature.
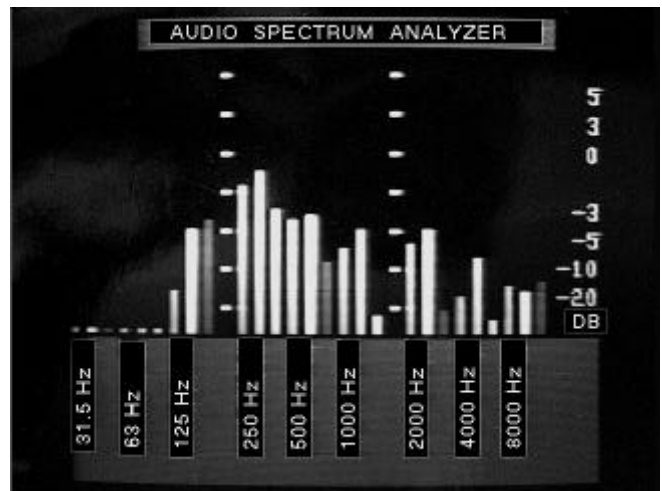
**Photo 4** Audio spectrum of the Oxide Noise Signature.
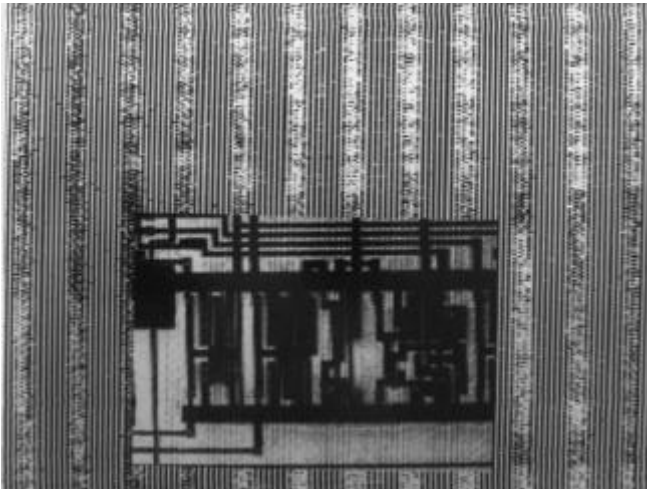
Photo 5 is an OBIC image and inset in the center is an image integrated scan of the OBIC signal over a known oxide integrity defect. Nothing was obtainable through the OBIC signal besides the noise signature.

In the case of CIVA, the existing constant current source is used to bias the pin leakage. The resulting CIVA signal consists of band limited noise and can be directly imaged on the SEM as previously shown in photos 1 and 2.

3. Characterization of LESD

The term "LESD" is used to imply that the product will pass all leakage tests within the specified parameters of the test even though low level leakage due to ESD damage is present. A number of low level leakage parts were identified to have leakage from 100 nA to 10 µA. The leakage was observed to be time and temperature variant in an unpredictable fashion and was initially believed to be ionic leakage due to bake-recovery of the parts with which had enough leakage (5 µA or more) to be detected at test. Parts that partially passed the leakage specification were obtained and characterized on the curve tracer. As shown in photo 6, this type of LESD manifests itself as low level leakage and as the voltage on the input pin is increased, the current increases exponentially.
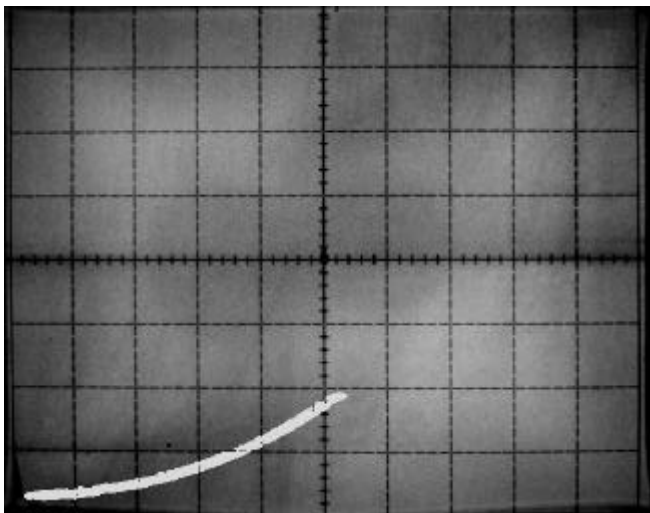
Photo 6 Curve characteristics of typical LESD.
Settings: 1 Volt/div. horizontal   50 nA/div. Vertical

To confirm this latency or walking-wounded phenomenon of the gate oxide, the voltage was gradually increased. Eventually the oxide ruptured. Typically the oxide rupture occurred anywhere from 13.5 to 16 volts as shown in photo 7.
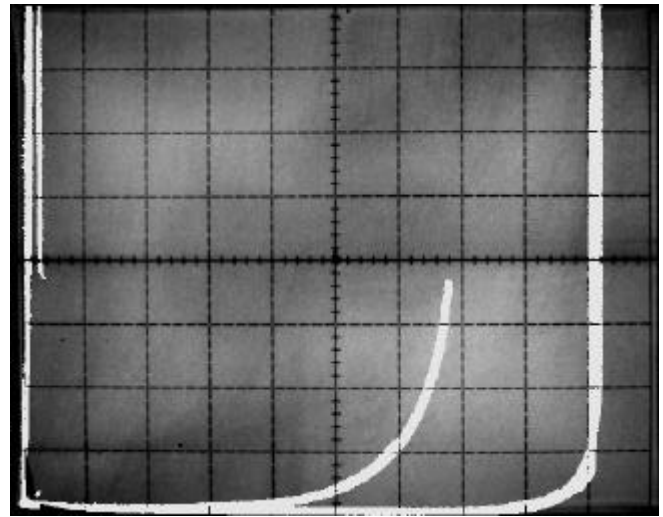
Photo 7 Curve characteristics of the latent leakage and subsequent rupture at 13.8 volts as compared to a reference pin.
Settings: 2 Volts/div. horizontal   5 µA/div. vertical

Note that the input protection does not turn on until 18 volts due to the need for superaddress programming voltages as high as 14 volts. The input protection no longer plays in the role of protecting the gate because the damage to the gate and its subsequent leakage results in failure of that gate long before the input protection turns on.[4] Once this value has been exceeded, the gate becomes a resistive short and LESD as well as oxide noise signature analysis methods are no longer applicable. Emission microscopy shows one clearly defined emission site on the gate structure whereas in reality there are typically two to five emission sites associated with a failure. When failure analysis is performed, however, only the high level leakage site is typically identified and analyzed.

The input leakage is actually a sum total of several leakage paths to substrate associated with a failing pin. The five individual input gate fingers of a latent input leakage have been Laser isolated and probed with the following results from previous work.[5]

Five isolated legs had leakage at 5 volts as follows:
leg 1=42 nA, leg 2=0 nA, leg 3=41 nA, leg 4=0 nA, leg 5=16 nA
Total = 99 nA.

Another input pin leakage was isolated and had leakage at 5 volts as follows:
leg 1=45 nA, leg 2=0 nA, leg 3=0 nA, leg 4=0 nA, leg 5=65 nA
Total = 110 nA.

4. CDM Creation of LESD

To better understand what happened to the ruptured oxide and how it is affected by stress, 17 reference parts without leakage were selected and run through a CDM (Charged Device Model) test.[6] CDM testing, pulses (or 'hits') each pin with a positive and a negative pulse five times at the following voltages: 500V, 1000V, 1500V and 2000V. In this experiment, rather than running all of the voltages and then checking for a failure, it

was decided to determine at what threshold the pins would begin to experience damage and then to stop. It was found that the damage threshold was at ±500 to ±600 volts with 1 pulse. Five pulses at ±450 volts did not result in failure. Since this was the case, ±500V was selected as the test voltage, since only some of the input pins were damaged, and it was fairly random as to which pin would be damaged. Photo 8 is a CDM waveform obtained from an input pin during a CDM event at 500 volts. These units were put through this 500V, one positive one negative pulse, and they were then checked on the curve tracer. They had leakage ranging from about 1.2 to 9 µA at 6 volts bias.
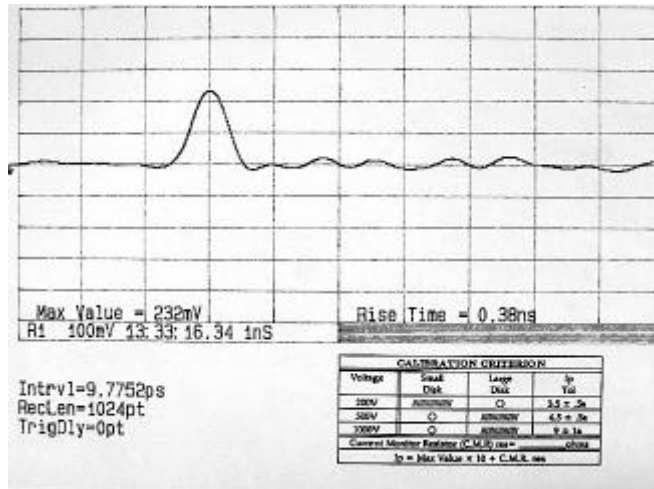
Photo 8 is a CDM waveform obtained from an input pin during a CDM event at 500 volts. Rise time = .38 nSec.

Leakage measurements were recorded for each pin and each part serialized. Part number 12 was baked for 24 hours at 225°C. Its original leakage measurement, after CDM testing, was 5.5µA. After this bake period, the same pin on part 12, now had 350 nA leakage (again measured at 6V of bias). This response was similar for greater than 95% of the pins on the parts examined as will be shown in table 1.

Regardless of whether the part was curve traced when it had microAmps or nanoAmps of leakage, the result was always the same: Reaching a voltage between 13.5 and 16 volts, the part would rupture into a short circuit on that pin, which would then be non-recoverable. See photos 7 and 9.
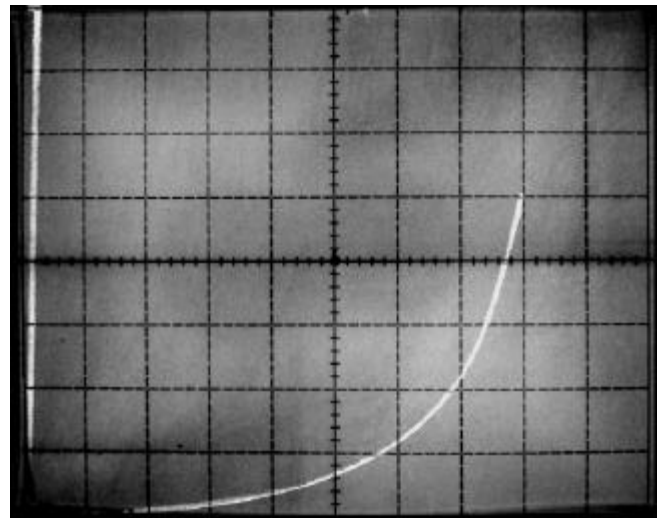
Photo 9 Curve characteristics of the latent leakage and subsequent rupture at 16 volts. This part was CDM stressed at ±700 volts 5 pulses.
Settings: 2 Volts/div. horizontal   10 µA/div. vertical

A bake recovered part (A part which has less than 5 uA of leakage after bake) is also a walking wounded candidate. If a compromised gate experiences a DC bias which exceeds 16 volts, that gate ruptures.

Part number 17 was tested a little differently. Part #17 had one pulse ±500V, then it was increased to ±700V, and then back to ±500V for 6 pulses total. The leakages were measured at 6 volts before and after a 24 hour bake at 225°C in table 1.

Table 1

| Pin #	Leakage	Leakage after a 225°C bake for 24 hours
4	10µA	2µA
5	7µA	150nA
6	7µA	160nA
7	7µA	150nA
8	7µA	120nA
9	5µA	170nA
10	7µA	150nA
11	6µA	150nA
23	7µA	6µA
27	11µA	220nA
28	7µA	160nA
29	7µA	200nA
30	9µA	180nA
31	7µA	125nA

Clearly, these pins dropped by about a magnitude of 50 in their leakage values after bake. To determine the bake time necessary to cause these pins to drop, the next experiment was performed. Another part from the CDM stress was taken and baked for 15 minutes at 225°C (effectively enough time for the part to ramp up to 225°C) and then allowed to cool. Afterwards most of the pins had dropped down into the 250 to 500 nA range. Another 15 minutes at 225°C reduced the leakage to the 150 to 220 nA range. This data indicates that the leakage seems to be related to a mechanical type stress associated with the defective gate oxide. This

mechanical stress can be viewed as being analogous to a spark gap. The spark gap theory matches the results seen both in terms of the sporadic readings on the curve tracer and the noise spectrum acquired with the spectrum analyzer when the input leakage was driven with a constant current source. The time variant nature of this type of LESD is shown in photo 10.
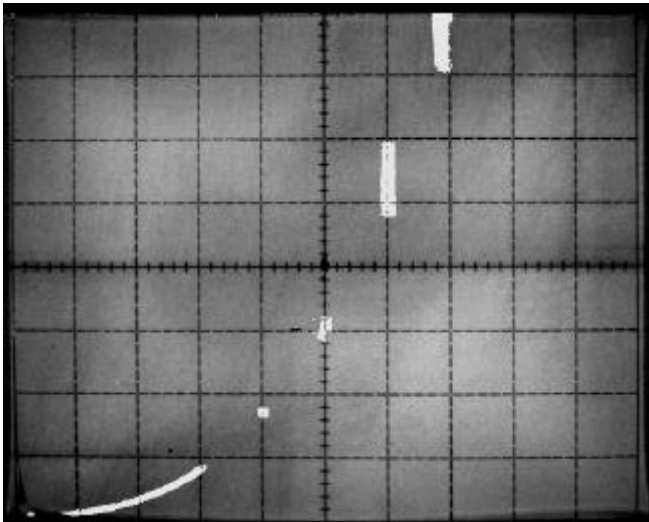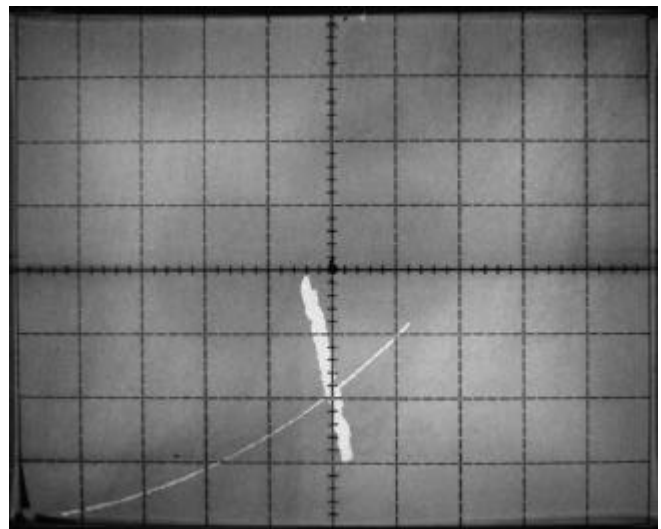

Photo 10 Curve characteristics of the time variant nature of the latent leakage at ambient. The curve tracer is set to dc+ mode. The curve was set at 4, 5, 6, and 7 volts respectively for 1 minute. The resulting vertical lines are a result of the variant leakage at each fixed voltage value. This part was CDM stressed at ±500 volts 1 pulse. Settings: 1 Volt/div. horizontal   .1 µA/div. vertical   (pin 3).

Biased temperature cycling was performed on part A, which received ±600 volts CDM stress, 1 pulse. Pin 27 was connected to the curve tracer and held at a bias of 5 volts. Temperature cycling then commenced from +130°C to -55°C (as evidenced by a vertical stripe due to changing leakage with temperature in photo 11). The exponential curve in photo 11 was obtained from the sweep taken on the device prior to temperature cycling. After the first temperature cycle, a second exponential curve was obtained (see Photo 12) and its cycling, plus to minus, is also shown. Notice that its curve is reduced from the first curve. The leakage after two temperature cycles has been reduced from 7µA down to 4µA at a 5V bias. The third temperature cycle resulted in a shorted condition associated with the pin. This was concomitant with one of the heater element cycles of the thermal forcing unit. The minimum leakage value observed prior to the short was 1.5 µA. The sensitive nature of LESD is shown in this experiment since a good control device does not fail during this test. Since the thermal forcing unit was operated from a separate power source, the proximity of the part to the thermal forcing unit was believed to have a sufficient field influence coupled with the bias to rupture the oxide.
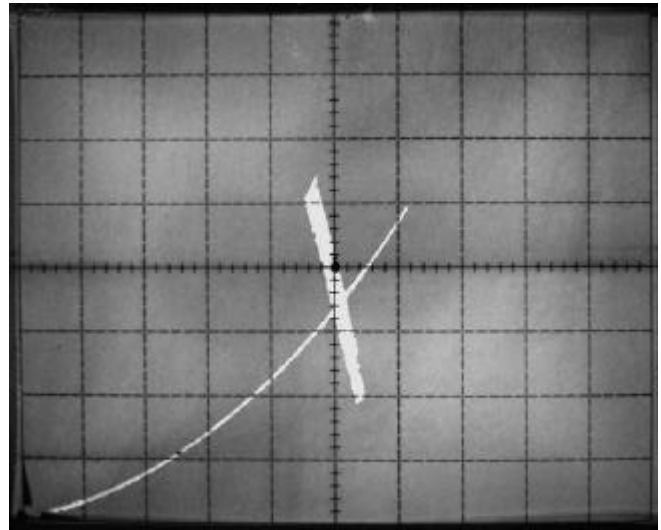
Photo 11 Curve characteristics of the temperature variant nature of the latent leakage. The curve tracer is set to dc+ mode. Pin 27 was connected to the curve tracer and held at a bias of 5 volts. One temperature cycle then commenced from +130°C to -55°C as evidenced by the vertical stripe due to changing leakage with temperature. The exponential curve is from the sweep taken on the device prior to temperature cycling. This part was CDM stressed at ±600 volts 1 pulse. Settings: 1 Volt/div. horizontal   2 µA/div. vertical


Photo 12 Curve characteristics of the temperature variant nature of the latent leakage after the second iteration of temperature cycling. The exponential curve is from the sweep taken on the device prior to the second iteration of temperature cycling. This part was CDM stressed at ±600 volts 1 pulse. Settings: 1 Volt/div. horizontal   2 µA/div. vertical

5. Failure Analysis of LESD on Input Gates

Once LESD has been identified associated with an input structure, either by use of the oxide noise signature technique or by simply using a laser cutter to sever the metal line connecting the gate to its input protection circuit, this gate can be analyzed to determine the number of leakage sites associated with that structure as well as the magnitude of leakage at each site. Device geometry was such that a major power buss was positioned over a section of the input gate and the emission sites located under that power buss. For this reason, the passivation surface was cracked gradually with a mechanical probe and metal etch was used to remove the power buss over the input structure. The leakage of the input was confirmed to remain reasonably constant around the 100 nA range at 5V.

Emission microscopy was performed and two emission sites associated with this one particular input pin were identified. The bias voltage was 10V. The reasons for this high bias voltage were that no emission sites could be identified at lower voltage ranges and this voltage value was prior to any permanent damage being done to the gate. The two emission sites had varying intensities as seen in photo 13.
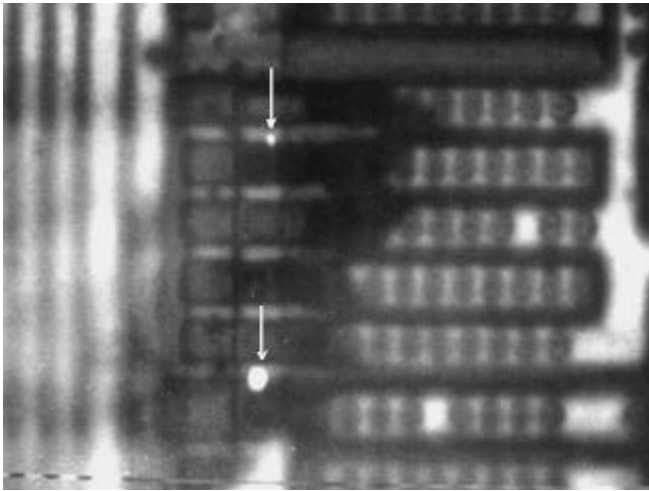

Photo 13 Two emission locations were identified on the input gate responsible for 110 nA of leakage at 5 Volts. The drive voltage was 10 volts with a CCD acquisition time of 400 seconds.

These emission sites correspond roughly to the leakage associated with each finger and will be discussed later. This emission image was taken with a Zeiss Confocal Laser Scanning Microscope and a CCD cooled camera.[7] The CCD cooled camera was utilized with an integration time of approximately 400 seconds and noise averaged for this image to be observed. (These are extremely low level emission sites). Most emission microscopes, and certainly the older infrared microscopes, are incapable of detecting such a low level signature of photon emission. This device was first deprocessed to expose the polycide and then each polycide finger was laser cut over field oxide to sever the individual fingers from the common polycide connection. The two edge fingers were mechanically probed and observed to leak, corresponding to the emission photograph (Figure 13). Using a curve tracer set in DC mode at 5V, leakage on one finger was approximately 70nA, and 30nA on the other finger. Notice this corresponds roughly to the intensity of the emission sites from photo 13. Five additional inputs were analyzed and found to yield similar results; between 1 and 3 low level emission sites were observed on the input gate structure mostly under the power buss.

6. Passive Voltage Contrast

Another method of analysis which can be used to isolate gate leakage is Passive Voltage Contrast (PVC).[8] This analysis method allows non-contact identification of gate leakage in the Scanning Electron Microscope. Three separate pins which had leakage due to CDM stress were analyzed using PVC. Passivation and metal were first removed, and BPSG was thinned over the polycide with HF acid. The remaining oxide over poly is evident in photo 14.
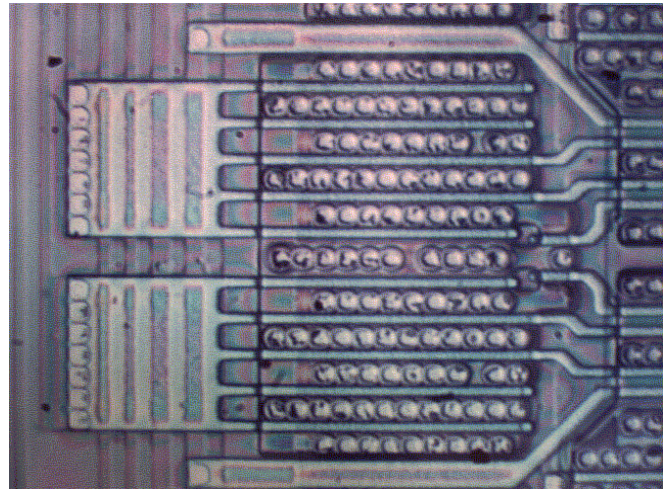
**Photo 14** Polycide gates with a thin layer of BPSG remaining on top.

Polycide was then exposed in a Technics RIE 800 etcher with CHF_3 at 6 SCCM (Standard Cubic Centimeters per Minute) and O_2 at a 1 SCCM flow rate. Five minutes at 150 watts was typical for removal of the remaining oxide layer as seen in photo 15.
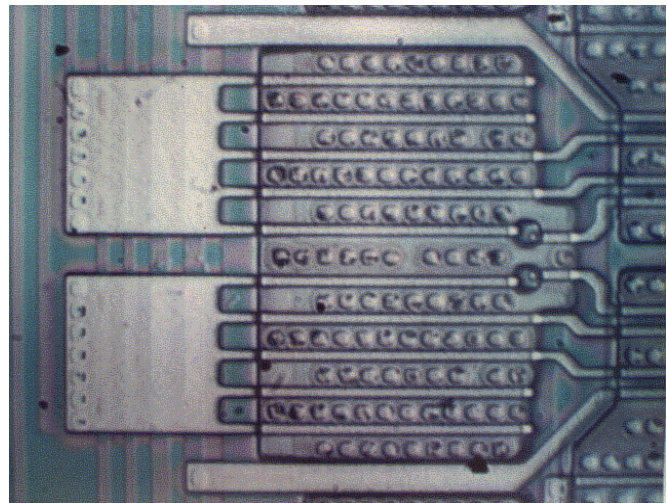
Photo 15 Polycide gates after removal of the thin layer of BPSG with a $CHF_3 + O_2$ plasma.

A laser cutter was then used to isolate the gate fingers over field oxide. The prepared sample was appropriately grounded at substrate and placed in the SEM at 2KV accelerating voltage and 60° tilt. No electrical feedthrus or fixtures were required since the electron beam provided the bias. Photos 16 and 17 are SEM PVC images of the gate leakage. The

illuminated fingers leak to substrate. Since the electron beam provides current to substrate in the sub-nanoamps range, the gates will not be damaged. SEM inspection at 10 KV and then PVC at 2 KV is typical and will not significantly alter the leakage performance if the beam current is not excessive.
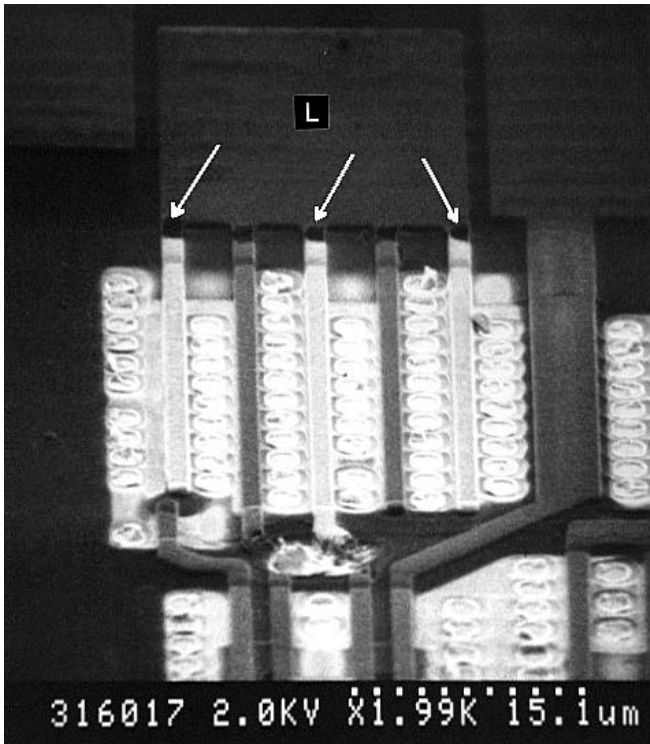
Photo 16 SEM PVC image which shows latent leakage on the two end fingers and the middle finger of the Laser isolated input structure. This gate is labeled "L".
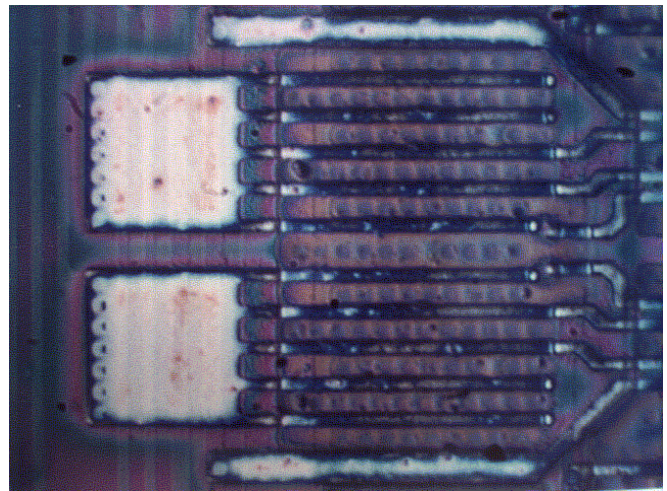
7. Ink Planarized Etch-Back of Polycide Gates

Once a failing gate structure has been identified, it must then be deprocessed to allow imaging of the damage area at the gate oxide level. Ink Resist, such as that used for hand tracing and etching copper trace PC boards, was smeared onto the surface of the device after polycide had been exposed (Photo 18) and was then oxygen etched, or ashed off, for three minutes at 150 watts of O_2 with a flow rate of 30 SCCM. The result is shown in photo 19. Note that ink still remains down in the diffusion areas, but the polycide gates are now exposed. Polycide was then removed with an RIE plasma at 50 watts using CF_4 at a 6 SCCM flow rate, N_2O at a 1.5 SCCM flow rate, and 100 seconds etch time. If the polycide was not completed removed, subsequent 30 second intervals of etchback typically removed the remaining polycide. An ultrasonic clean was used if necessary. Since the gates were not severely undercut (due to the ink protecting the diffusion areas), ultrasonics could be used without risk of damaging the edges of the gate oxide. Photo 20 shows the three exposed gate oxide input transistors. The arrows identify the visible LESD damage areas.
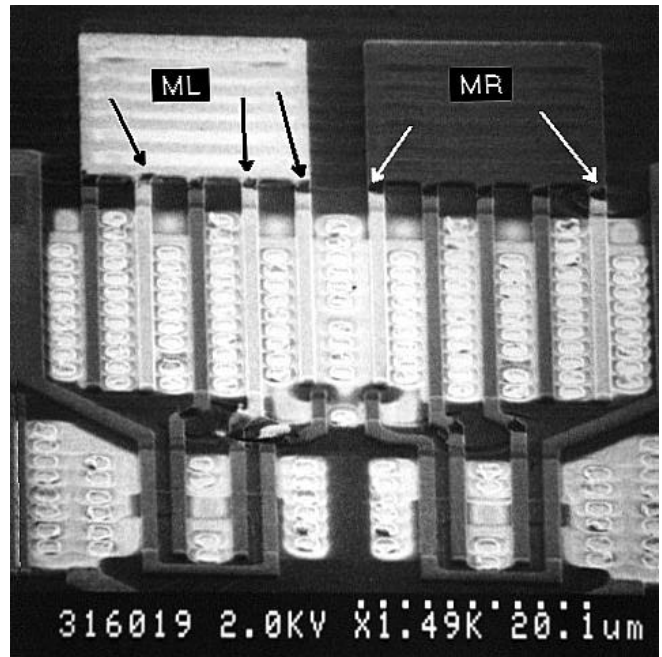
Photo 17 SEM PVC image which shows latent leakage on two adjacent gate structures labeled "ML" and "MR" respectively. "ML" has three illuminated fingers with leakage, "MR" has two.

Photos 21-24 are the corresponding SEM photographs which show from 3 to 5 LESD damage areas. Photo 21 provides detail of the damage site. Note the hole within a hole. The outside dark ring is due to some plasma undercut which removed the underlying channel radially from the rupture. The size of the inner hole ranges from .15 μm to .26 μm in the Y direction and from .12 μm to .19 μm in the X direction for various samples. Note the oxide spacer sidewalls are still present even though polycide is removed. This is due to two factors:


Photo 18 Polycide gates after ink deposition with a resist ink pen.

1. CHF3 plasma was used to expose the polycide in a reactive ion etch environment to prevent undercut to the gates.

2. The ink planarization etch back prevents undercut of these gates to also help keep the sidewall spacers intact.
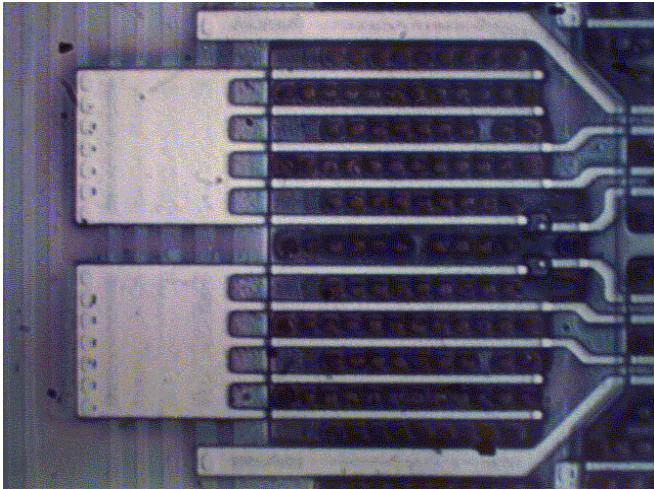

Photo 19 Polycide gates after O_2 ashing of the ink. The polycide surface is now exposed, however, the diffusions are still ink protected.
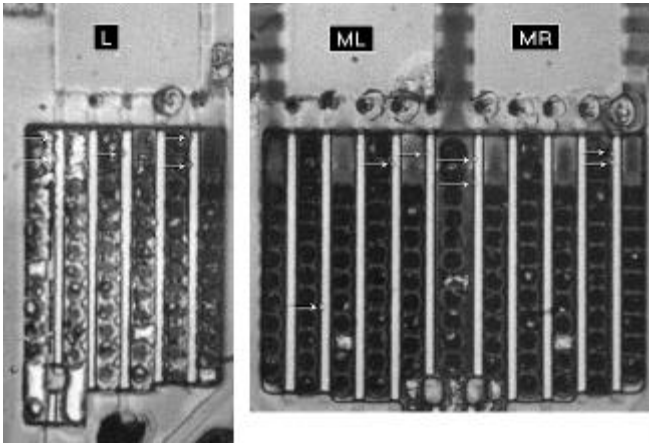
Photo 20 Optical image of the exposed gate oxide for locations "L", "ML", and "MR". The arrows identify the rupture sites.
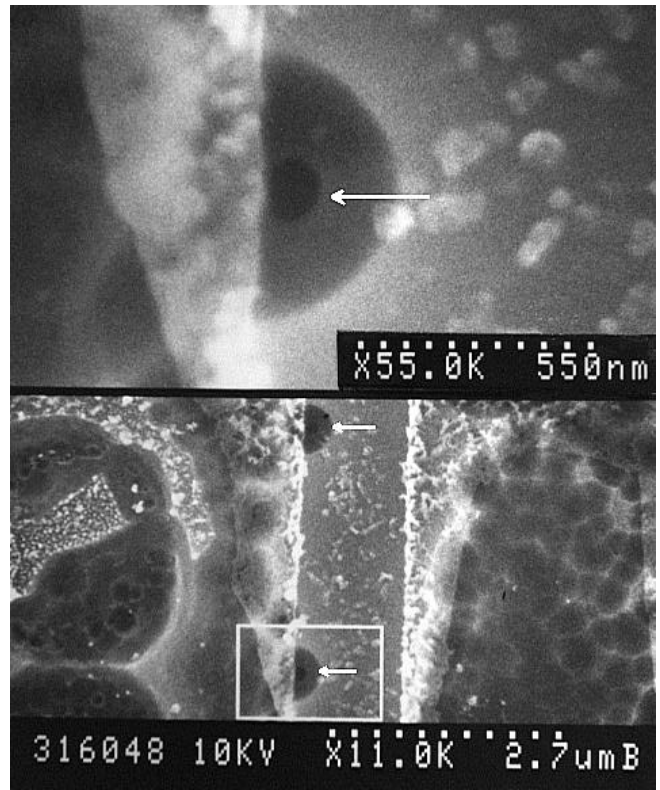

Photo 21 SEM high magnification split view of the LESD damage sites. Note the hole within a hole. The outside dark ring is due to plasma undercut which removed the underlying channel radially from the rupture. The size of the rupture ranges from .15 μm to .26 μm in the Y direction and from .12 μm to .19 μm in the X direction for various samples.
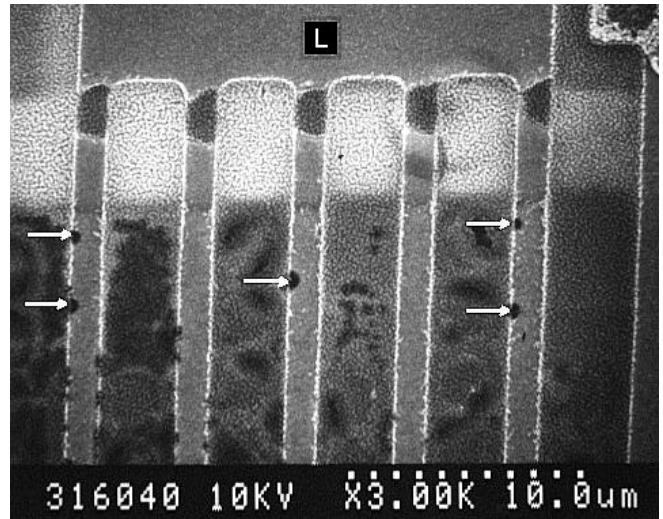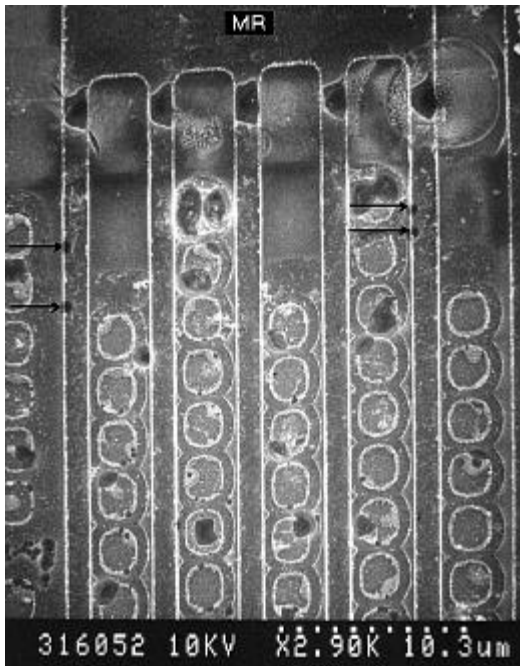

Photo 22 SEM view of the LESD damage sites associated with location "L". 5 damage sites have been identified corresponding to photo 16. Some areas have evidence of irregular gate undercut due to thinning of the ink protecting the diffusion. High magnification inspection confirmed those areas as undercut only.
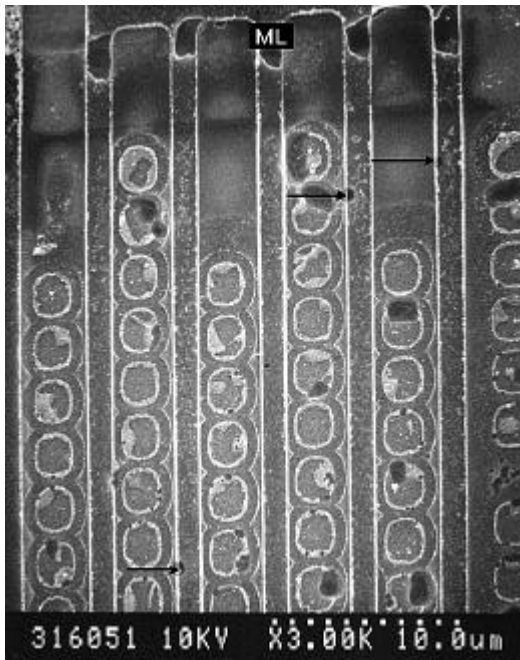
Photo 23 SEM view of the LESD damage sites associated with location "ML". 3 damage sites have been identified corresponding to photo 17. One area had evidence of irregular gate undercut on the left finger due to thinning of the ink protecting the diffusion. High magnification inspection confirmed this area as undercut only.

Photo 24 SEM view of the LESD damage sites associated with location "MR". 4 damage sites have been identified corresponding to photo 17. One area had evidence of irregular gate undercut on the second from the left finger due to thinning of the ink protecting the diffusion. High magnification inspection confirmed this area as undercut only.

8. Atomic Force Microscopy of LESD Damage

The LESD damage site from photo 21 was analyzed using a Digital Instruments Atomic Force Microscope (AFM).[9] Photos 25 and 26 are AFM views of the LESD rupture. Photo 25 shows the location of the hole associated with the oxide sidewall. Photo 26 shows the hole to be cone shaped. This is due to tip convolution as the edges of the tip enter the LESD hole. The edges of the hole were measured to be: Y = .19 μm, X = .14 μm. Notice that the etch undercut ring from photo 21 is not visible in the AFM images since the AFM reveals the true surface profile.
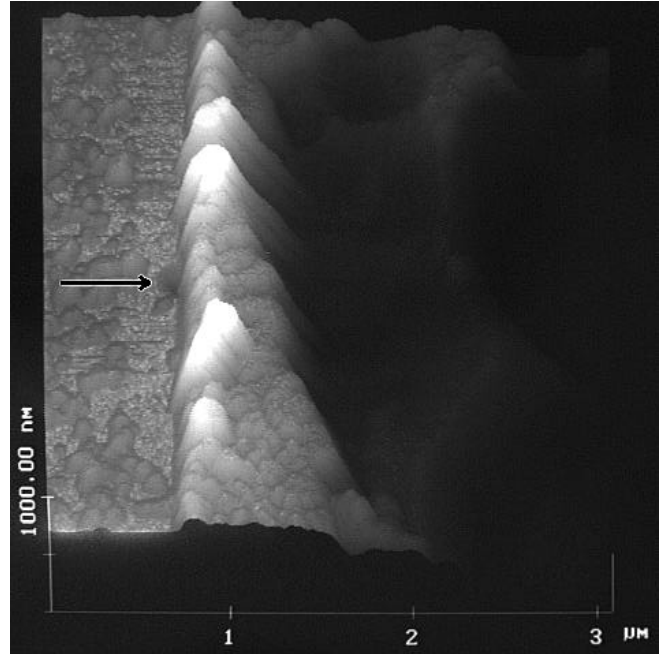
Photo 25 Atomic Force Microscope Image of an LESD damage site. Compare the appearance of the oxide sidewall to the SEM image in photo 21.

9. Conclusions

The Oxide Noise Signature method to identify the presence of oxide integrity issues on a CMOS process has been presented and used specifically for identifying latent input leakage. The Oxide Noise Signature method can also be used to identify compromised oxide associated with a functionally failing device while biased in an Icc standby mode, even if Icc standby is at or below specification. Products can be statistically sampled, without in-depth analysis, to identify gate oxide integrity issues.

LESD associated with input pins was shown to be bake recoverable by a factor of 50, however the gate rupture voltage remains reduced. Analytical methods were presented using Emission Microscopy and laser isolation for Passive Voltage Contrast to show multiple damage sites on an input gate structure. Finally the Atomic Force Microscope was used to image an LESD rupture.

support and of course, my wife Mayra for helping me assemble the manuscript.
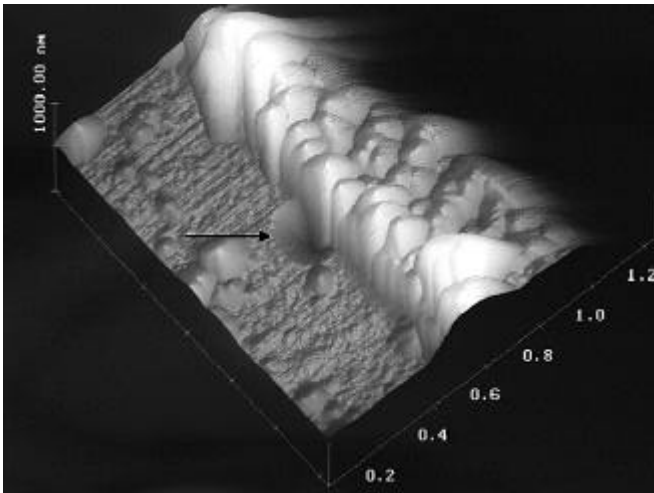
Photo 26 Atomic Force Microscope Image of an LESD damage site at increased magnification.

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