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Phase and Jitter Noise analysis of Phase Locks Loop (PLL) as Frequency Synthesiser

Aditi Sharma, Poonam Rana, Suraj Rana
M-Tech Scholar, PDM college of Engineering, Bahadurgarh
Assistant Professor, Department of ECE, PDM college of Engineering for Women, Bahadurgarh
Assistant Professor, Department of ECE, MRIEM, Rohtak

Abstract: ***In this paper, we are evaluating the performance of the phase lock loop in the presence of phase noise and jitter noise. We are analysing the performance of PLL in one application of signal processing as frequency synthesiser. All the components of PLL contribute to the noise of the system. Two type of noise are presented that affect the performance of the system that are phase noise and jitter noise. Firstly, the Phase noise is generally used for representing short term random frequency variations of a signal. Non linear oscillators naturally produce high phase noise. Secondly, Jitter is generally used to refer to the time variation of a periodic signal in relation to the clock. The phase and jitter are the critical performance parameter to analysis the performance of the PLL. Simulation Result reveals that the performance of the PLL system is affected more by jitter noise compared to that of phase noise. Extensive simulation result is presented to demonstrate the effectiveness of the proposed techniques.***

Keywords: **Phase lock loop (PLL), Jitter noise, phase noise, frequency synthesiser.**

I. INTRODUCTION

Phase lock loop find its applications in many fields of engineering such as digital signal processors [1] for clock generation and as frequency synthesizers [2] in RF communication systems [7] for clock extraction and generation of a low-phase-noise local oscillator signal from an on-chip voltage-controlled oscillator (VCO) which might have a higher open-loop noise performance. PLLs [8] are also used to maintain a well defined phase and hence frequency relation between two independent signal sources. Higher clock rates in many applications such as video, audio, and data processors, requires increasingly higher performance from the clock synthesizers used to drive them. In clock recovery [3] applications, such as data communications and disk drive read channels, as well, higher speeds require better performance from the VCOs and the overall timing recovery phase-locked-loop itself. Phase locked loop (PLL) is one of the most inevitable necessities in modern day electronic systems. It finds widespread applications in generation and synchronization of well timed clocks, recovery of signal from noisy communication channel, FPGA's, communication systems, frequency-synthesiser [4][5], trans-receivers [6]. Since a PLL can be incorporated in a single chip, it is highly preferred. In this paper, we are evaluating the performance of the phase lock loop in the presence of phase noise and jitter noise. We are analysing the performance of PLL in two application of signal processing as frequency synthesiser and coherent modulation. All the components of PLL contribute to the noise of the system. Two type of noise are presented that affect the performance of the system that are phase noise and jitter noise. Firstly, the Phase noise is generally used for representing short term random frequency variations of a signal. Non linear oscillators naturally produce high phase noise. Secondly, Jitter is generally used to refer to the time variation of a periodic signal in relation to the clock. The rest of the paper is organized as follows: In Section II, phase lock loop (PLL) system is explained in detail. In section III, mathematical analysis of phase lock loop system is presented with the application of frequency synchronizer. In Section IV, present the noise analysis of phase and jitter noise in PLL system. Section V, presents the performance analysis of frequency synthesiser in the presence of jitter noise. Finally, a conclusion is made base on this study.

II. PHASE LOCK LOOP

A PLL is an example of a control system using negative feedback which tracks the phase changes that are within the bandwidth of the PLL. A PLL also multiplies a low-frequency reference clock, to produce a high-frequency clock. The phase-locking [9][10] is done after many iterations of comparing the reference and feedback signals. The goal of the PLL is to match the reference and feedback signals in phase. The state at which both the frequencies match is known as the locked state. After this, the PLL continues to compare the two signals but since they are in lock mode, the PLL output is constant.

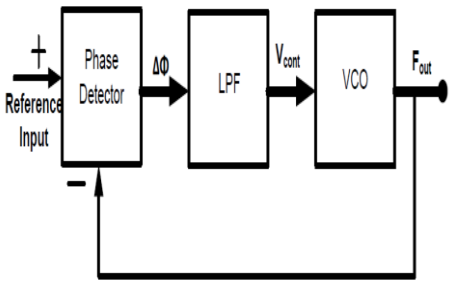

Fig. 1 block diagram of PLL

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A phase detector is a circuit whose average output voltage is proportional to the phase difference Δϕ, between two inputs. In the ideal case relation between average output voltage and input phase difference is linear, crossing the origin for Δϕ=0 as shown in fig. 2.

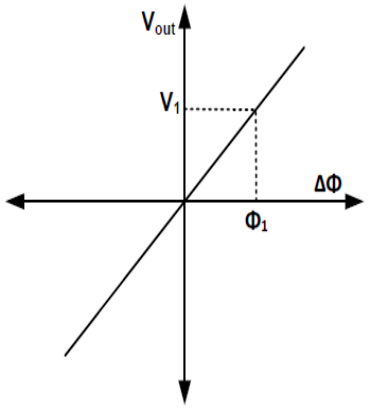

Fig. 2 Phase detector characteristics

Called the gain of PD is the slope of line, K_{PD}, which is expressed in V/rad. The output of PD is then passed through a low pass filter, so as to remove the high frequency content in PD output voltage. This is required because; the control voltage of oscillator must remain quit in steady state [11]. Filter also provides a memory for the loop in case lock is momentarily lost due to large interference transient. This filtered control voltage is then applied to the input of Voltage Controlled Oscillator. Control voltage forces the VCO to change the frequency in the direction that reduces the difference between input frequency and output frequency. If two frequencies are sufficiently close, the PLL feedback mechanism forces the two PD input frequency frequencies to be equal and the VCO is locked with incoming frequency. This is called as locked state of PLL [12].

III. MATHEMATICAL MODELING OF PLL

A linear model of PLL can be constructed mathematically by considering figure 3, which shows the linear model of type I PLL. Low pass filter is assumed to be of first order for simplicity.

The PD output contains a dc component equal to $K_{PD}(\Phi_{out} - \Phi_{in})$ as well as high frequency components which are filtered by the LPF. PD is simply modelled as a subtracter whose output is amplified by K_{PD}. The overall PLL model consists of the phase subtractor, the LPF transfer function $1/(1+ s/\omega_{LPF})$, where ω_{LPF} is the 3 dB bandwidth and the VCO transfer function K_{VCO}/s. Here, Φ_{in} and Φ_{out} are the excess phases of input and output waveforms, respectively.

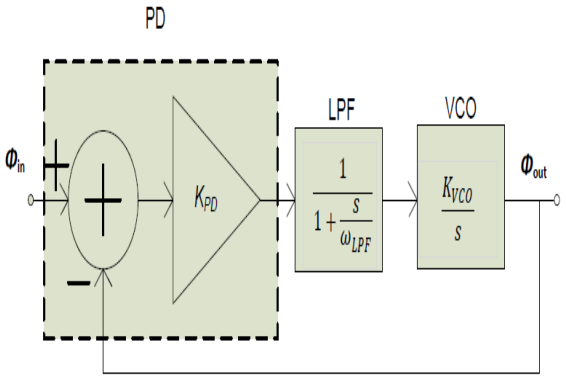

Fig. 3 Linear model of PLL

The open loop transfer function is given by

$$H(s)|_{open} = \frac{\Phi_{out}}{\Phi_{in}}(s)|_{open} \quad (1)$$

$$= K_{PD} \cdot \frac{1}{1+\frac{s}{\omega_{LPF}}} \cdot \frac{K_{VCO}}{s} \quad (2)$$

From (2) closed loop transfer function can be obtained as

$$H(s)|_{closed} = \frac{K_{PD}K_{VCO}}{\frac{s^2}{\omega_{LPF}}+s+K_{PD}K_{VCO}} \quad (3)$$

Here $H(s)|_{closed}$ is simply denoted by Φ_{out}/Φ_{in}. Further, since the frequency and phase are related by a linear operator, the transfer function of (3) can be expressed as

$$\frac{\omega_{out}}{\omega_{in}}(s) = \frac{K_{PD}K_{VCO}}{\frac{s^2}{\omega_{LPF}}+s+K_{PD}K_{VCO}} \quad (4)$$

This is second order transfer function of PLL. Using the control theory approach the "natural frequency" and "damping ratio" are given by

$$\omega_n = \sqrt{\omega_{LPF}K_{PD}K_{VCO}} \quad (5)$$

$$\zeta = \frac{1}{2}\sqrt{\frac{\omega_{LPF}}{K_{PD}K_{VCO}}} \quad (6)$$

The step response is given by

$$\omega_{out}(t) = \left[1 - \frac{1}{\sqrt{1-\zeta^2}}e^{-\zeta\omega_n t}\sin\left(\omega_n\sqrt{1-\zeta^2}t+\theta\right)\right]\Delta\omega u(t) \quad (7)$$

Where ω_{out} denotes the change in output frequency and

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$$\theta = \sin^{-1}\sqrt{1-\zeta^2}$$

Settling speed of PLL is of great concern in most applications. Equation (7) thus, shows that the exponential decay determines how fast the output approaches its final value, provided that $\zeta\omega n$ is maximized. Using equation (5) and (6), yields,

$$\zeta\omega_n = \frac{1}{2}\omega_{LPF} \tag{8}$$

This result shows the critical tradeoff between settling speed and ripple on the VCO control line. If we reduce the cut-off frequency of filter, greater high frequency components are suppressed but at the same time pull in time increases.

IV. NOISE ANALYSIS OF PLLS

For a first order loop, no exploit filter H(s) exists and the PD is usually implemented using an analog multiplier or an XOR gate [12]. Assuming no divider, the closed loop phase transfer function of the 1st order loop with a PD gain of Kp volts/rad. can be expressed as

$$\frac{\phi out(s)}{\phi in(s)} = \frac{K}{K+s} = \frac{1}{1+\frac{s}{\omega loop}} \tag{9}$$

where the loop bandwidth, K=KpKv. The loop bandwidth is defined as the -3 dB frequency of the closed loop transfer function. The block diagram of the 1st order loop with noise sources is shown in Fig. 4. Assuming an ideal phase detector, the two noise sources in the circuit are the VCO and the reference input. The phase noise at the output can be calculated using superposition. Assuming a noiseless input, the effect of VCO phase noise can be calculated using the transfer function from n(s) to $\varphi_{out}(s)$, which is

$$\frac{\phi out(s)}{n(s)} = \frac{Kv}{KpKv+s} \tag{10}$$

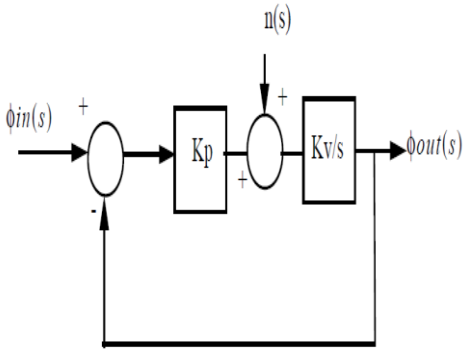

Fig. 4 Block diagram PLL with noise sources

The output phase noise due to VCO phase noise only can be expressed as,

$$S\phi out(\omega) = \frac{No}{2}\left|\frac{\phi out(s)}{n(s)}\right|^2 = \frac{NoKv^2}{2\left(Kp^2Kv^2+\omega^2\right)} \tag{11}$$

and

$$S\phi out(\omega) = \left|\frac{Kv}{j\omega}\right|^2 Sin(\omega) = Kv^2\frac{No}{2\omega^2} \tag{12}$$

Comparing equation (11) and (12), it is evident that the phase noise of the PLL output is the same as the phase noise of the VCO for offset frequencies larger than w_{loop}. This is because the PLL is unable to react fast enough to fast random changes in the VCO output and hence they directly appear on the output. At low offset frequencies, the PLL compensates the slow random variations produced by the VCO noise at the output by adjusting the VCO control voltage and thus suppresses the VCO noise. These effects are shown in Fig. 5.

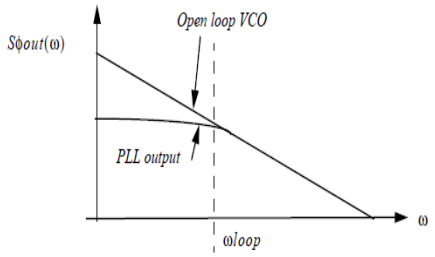

Fig. 5 Output phase noise spectrum with a noiseless input

Assuming a noiseless VCO, the response of the loop to the phase variations in the input is considered. The input is usually another oscillator which will have its own phase noise characteristics. Taking into account only the phase noise in the $1/f^2$ region, its power spectrum can be written as,

$$S\phi in(\omega) = \frac{\alpha}{\omega^2} \tag{13}$$

The power spectrum at the output can be easily calculated as

$$S\phi out(\omega) = \frac{\alpha Kp^2Kv^2}{\omega^2\left(Kp^2Kv^2+\omega^2\right)} \tag{14}$$

If the two noise sources in the PLL are combined we obtain the phase noise plot of Fig. 6. The plot reveals a fundamental property of the PLL: its phase noise is dominated by the input source noise at frequency offsets

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below the loop bandwidth and by the VCO noise at frequency offsets above the loop bandwidth. Thus a PLL having a noisy VCO and a clean reference input should be designed to have a large loop bandwidth. But the loop bandwidth is inversely related to the PLL settling time [6]. Consequently, if the loop bandwidth is large, the PLL takes little time for locking and has a large noise reduction of the internal VCO noise, but cannot have a good suppression of the external input noise.

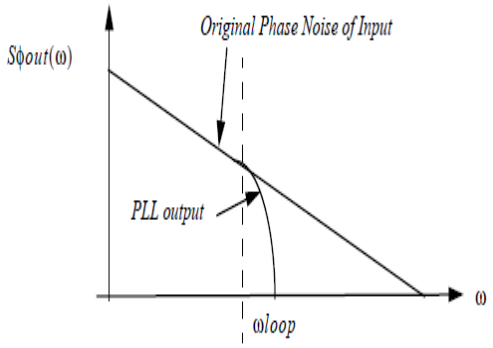

Fig. 6 Output phase noise spectrum with a noise less VCO

V. SIMULATION RESULTS

In this Section, we are analysing the performance of the phase lock loop in frequency synthesis application in the presence of phase noise.

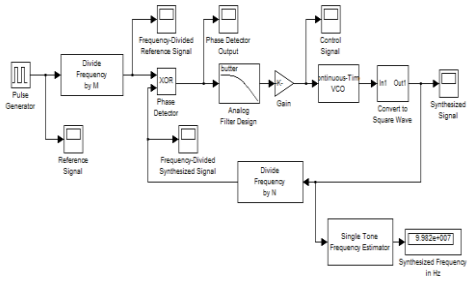

Fig. 7 Frequency synthesis of phase lock loop in the presense of noise

Here, we are performing the frequency synthesis of PLL. Simu link block diagram of PLL as frequency synthesis is shown in fig. 7. Fig. 8 depicts the reference signal to the input of the PLL block as frequency synthesis. Fig. 9 demonstrates the response of the control signal. Fig. 10 shows the performance of the frequency synthesis.

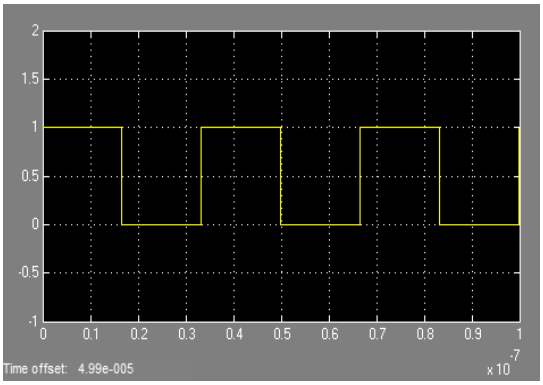

Fig. 8 Reference Signal to the input of PLL

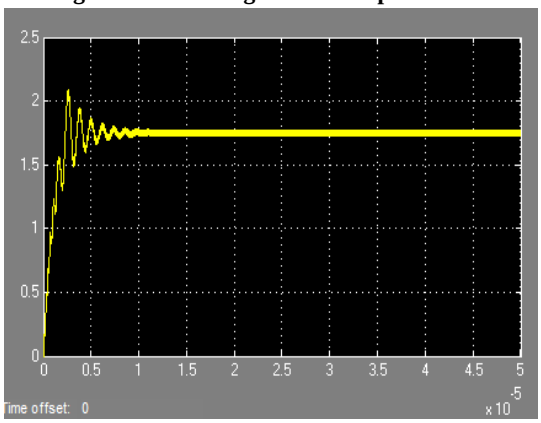

Fig. 9 Control signal of frequency synthesiser in the presence of Noise

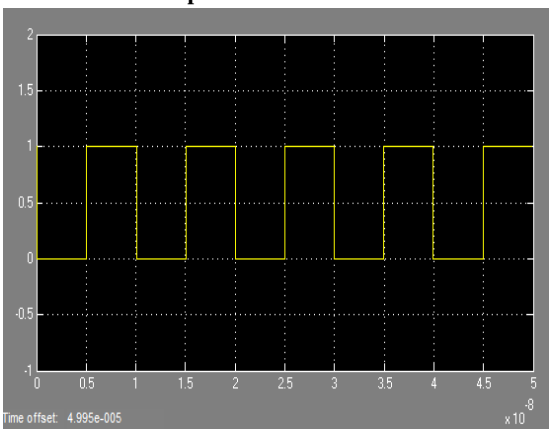

Fig. 10 Synthesis signal of the frequency synthesiser in the presence of phase noise

VI. CONCLUSIONS

In this paper, we are evaluating the performance of the phase lock loop in the presence of phase noise and jitter noise. All the components of PLL contribute to the noise of the system. Two type of noise are presented that affect the performance of the system that are phase noise and jitter noise. Simulation Result reveals that the performance of the PLL system is affected more by jitter noise compared to that of phase noise. Extensive simulation result is presented to demonstrate the effectiveness of the proposed techniques.

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