Research Journal of Applied Sciences, Engineering and Technology 5(10): 2957-2963, 2013
ISSN: 2040-7459; e-ISSN: 2040-7467

Submitted: September 15, 2012 Accepted: October 31, 2012 Published: March 25, 2013

Designs and Implementations of Low-Leakage Digital Standard Cells Based on Gate-Length Biasing

Jindan Chen and Jianping Hu
Institute of Circuits and System, Ningbo University, Ningbo 315211, China

Abstract: In this study, a minimum set of low-power digital standard cells for low-leakage applications are developed and introduced into SMIC (Semiconductor Manufacturing International Corporation) 130 nm CMOS libraries, which include basic logic gates such as inverter, NAND, NOR, XOR, XNOR and flip-flop. The inverter, NAND, NOR and flip-flop standard cells based on the gate-length biasing technique are proposed to achieve low Energy Delay Product (EDP). The XOR and XNOR standard cells are optimized based on transistor-level. All circuits are simulated with HSPICE at a SMIC 130nm CMOS technology by a 1.2V supply voltage. The proposed several standard cells attain large leakage reductions. A mode-10 counter is verified with the proposed standard cells by using commercial EDA tools. The leakage and total dynamic power dissipations of the mode-10 counter using the proposed standard cells provide a reduction of 21.27 and 3.06%, respectively. The results indicate the proposed standard cells are a good choose in low leakage applications.

Keywords: Digital standard cells, gate-length biasing techniques integrated circuits, low-leakage designs

INTRODUCTION

Technology scaling increases the density and performance of integrated circuits, resulting in large power dissipations. With the growing uses of portable and wireless electronic systems, energy-efficient designs have become more and more important in VLSI chips (Agarwal *et al.*, 2004). The total energy consumption in a CMOS circuit includes mostly two components: switching energy due to charging and discharging for loads and static energy dissipation that is caused by leakage currents of MOS devices. Before the CMOS process is scaled into deep sub-micro process, dynamic energy loss has always dominated power consumption, while leakage dissipation is little. The aggressive scaling of device dimensions and threshold voltage has significantly increased leakage current exponentially, which attracts extensive attentions.

There are several leakage sources in nanometer CMOS processes: sub-threshold leakage current, gate leakage current and band-to-band tunneling leakage current. In three leakage sources, the sub-threshold leakage is the dominant contributor to total leakage at 130 nm and is forecast to remain so in the future, because it increases exponentially with threshold voltage (V_{th}) (Fallah and Pedram, 2005). Many leakage reduction techniques have been proposed recently at various design levels, such as MTCMOS (Multi-Threshold CMOS) power-gating technique (Kao and Chandrakasan, 2001), DTCMOS (Dual Threshold CMOS) (Zhang *et al.*, 2011), VTCMOS (Variable Threshold CMOS) (Peiravi and Assai, 2008) and GLB (Gate-Length Biasing) (Gupta *et al*., 2006) have been proposed in recent years and achieved considerable energy savings.

Low power, high speed and small area are three main objectives in IC design. Today's advanced designs require a careful balancing of many competing challenges. PDP (Energy Delay Product) metric provides a good compromise between speed and delay, which is written as:

$$EDP = E \times t_{\text{delay}} \quad (1)$$

Cell-based design flow has been widely used for digital chip designs with commercial EDA tools. In order to realize a low-power chip, standard cell libraries and IP (Intellectual Property) cores should be constructed with low-power design techniques. Many power reduction techniques have been proposed for standard cell libraries. Semicustom design methodologies were proposed with MTCMOS power-gating standard cells (Kim and Shin, 2007. The authors presented low-leakage standard cell based ASIC design methodologies for both static CMOS and domino logic (Jayakumar and Khatri, 2007). The transistor-level DTCMOS was also used for low-leakage standard cells (Nagarajan *et al.*, 2009).

For a typical technology with a sub-threshold slope of 100mV/decade, each 100mv reduction in V_{th} will cause an order of magnitude increase in leakage currents (Wang *et al*., 2006). In short channel devices, with

Corresponding Author: Jianping Hu, Institute of Circuits and System, Ningbo University, Ningbo 315211, China

increasing of the gate length, the threshold voltage increases, so that the leakage decreases exponentially and delay increases linearly. The Gate-Length Biasing (GLB) technology increases the channel length of transistors to alter the threshold voltage and reduces leakage exponentially in both active and standby modes, while delay increases only linearly with the increasing of the gate length (Hu and Wang, 2011). It is reported that small biases in channel length of transistor can afford significant leakage savings with small performance impact (Heo and Shin, 2007).

In this study, a minimum set of low-leakage digital standard cells are developed, which include basic logic gates such as inverter, NAND, NOR, XOR, XNOR and low-leakage power flip-flop. These standard cells are optimized to achieve low Energy Delay Product (EDP). The layout design, abstract and standard-cell characters of these standard cells are also described. In order to show energy efficiency of the proposed standard cells, a mode-10 counter is verified with the proposed standard cells by using commercial EDA tools. The results indicate the proposed standard cells are a good choose in low power design.

LOW-POWER DESIGNS OF THE MINIMUM SET OF STANDARD CELLS

Basic logic gate cells with gate-length biasing: The basic gates such as inverter, NAND and NOR are important elements in digital circuits, since they are largely used. However, basic logic gate standard cells used in most current CMOS processes such as SMIC 130 nm are mostly based on standard CMOS logic. We increase the gate-length of basic logic gates including inverter, NAND and NOR from 130 nm to 250 nm by 10 nm step. HSPICE simulations are carried out for the basic standard cells with Gate-Length Biasing technology. The leakage dissipation and delay of the inverter are shown in Fig. 1.

With increasing of the gate length, the leakage power decreases exponentially and delay increases linearly. Therefore, it is possible that the best EDP is achieved by using channel length biasing technology. The EDP of the inverter, NAND and NOR cells are shown in Fig. 2. The results show that the basic standard cells with the GLB technology have lower EDP than the SMIC one with the standard gate-length. The inverter, NAND and NOR cells have the best EDP when their gate length is 0.18, 0.19 and 0.20 um, respectively. The inverter cell provides an EDP reduction of 23.7%, thought its delay is slightly larger than the SMIC one.

Low power XOR and NXOR circuits: In commercial standard-cell library such as the SMIC, the XOR circuit is typically realized based on a TG logic structure with 12 transistors, as shown in Fig. 3a. The XOR and XNOR structures with 10 transistors used in this study are shown in Fig. 3b (Wang and Hu, 2011). Because of

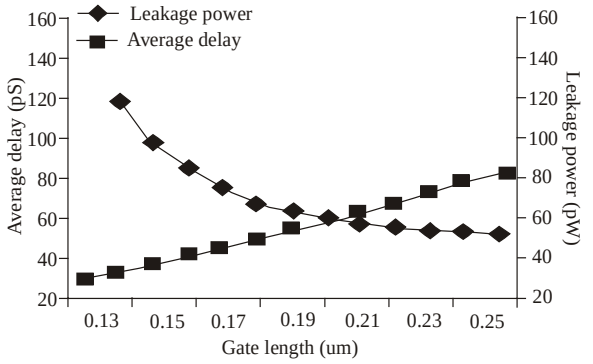


Fig. 1: Leakage power dissipation and delay of the inverter standard cell

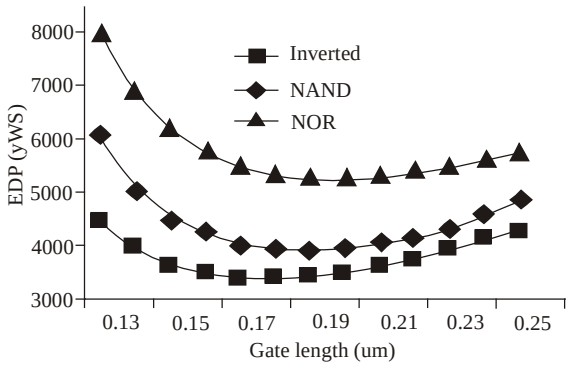
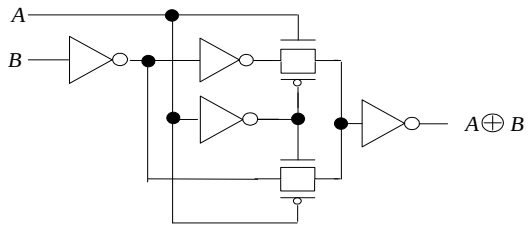
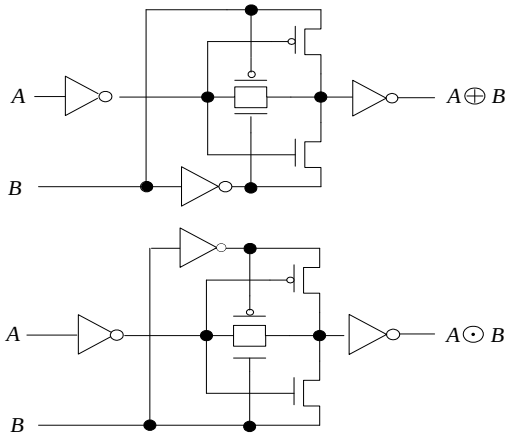


Fig. 2: EDP of the inverter, NAND and NOR standard cells



(a) XOR circuit of the SMIC



(b) XOR and XNOR structures used in this work

Fig. 3: XOR and XNOR circuits for the SMIC 130nm standard-cell library

Table 1: EDP comparisons of two XOR standard-cells

Cells	Energy loss per switching (fJ)	Propagation delay (ps)	EDP (pJs)
SMIC XOR	41.28	78.3	3.232224
The proposed XOR	26.96	89.1	2.402136

Table 2: Leakage power of three flip-flop cells (nW)

DFFQX1	TGMS	TGMS-GLB
1.13	0.99	0.92

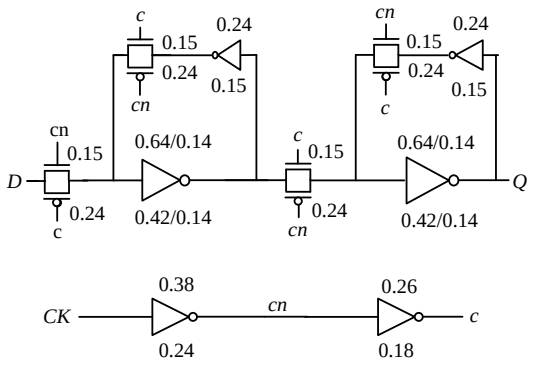


Fig. 4: Flip-flop standard cell based on Transmission Gate Master-Slave Structure with Gate-Length Biasing (TGMS-GLB)

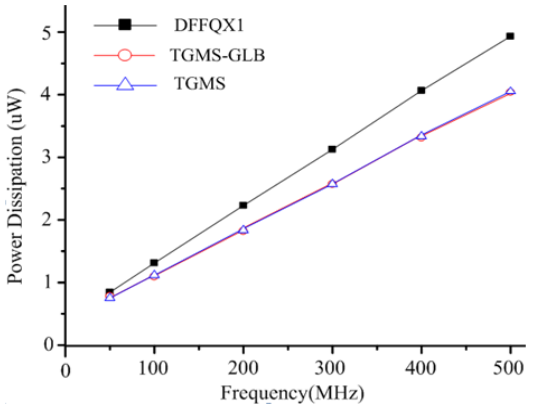


Fig. 5: Power dissipations of the three flip-flop cells

their simple structures, it is expected that they have lower power than the SMIC 130nm one.

The energy delay product of the two XOR cells is shown in Table 1. The results show that the XOR has lower EDP than the SMIC one. The XOR has 53% energy saves and provides an EDP reduction of 34%, although its delay is slightly larger than the SMIC one.

Low-leakage flip-flop with gate-length biasing: A flip-flop is important element in digital circuits. The C^2MOS flip-flop (DFFQX1) is used in the SMIC 130 nm standard-cell library. A low-leakage power flip-flop standard cell based on Transmission Gate Master-Slave structure (TGMS) with GLB technology is used to achieve low energy delay product in this study, as shown in Fig. 4 (Hu and Wang, 2011). The gate-length in the TGMS flip-flop is increased to 140nm (TGMS-GLB). HSPICE simulations have been carried out for the three flip-flops cells (DFFQX1, TGMS and TGMS-GLB).

The power dissipations of the proposed flip-flop cell have been comprised with the other two ones, as shown in Fig. 5.

Figure 5 show that the low-leakage flip-flop cell with GLB has lower energy consumption than the SMIC one. Compared with the SMIC standard cell, the low-leakage flip-flop cell has 19% energy saves.

The leakage dissipations of the three flip-flop standard cells are shown in Table 2. TGMS-GLB attains a power reducing of 19% compared with the DFFQX1.

LAYOUT DESIGNING AND POST-LAYOUT SIMULATIONS

Basic logic gate cells using GLB: The layout of the proposed basic logic gate standard cells is shown in Fig. 6, which include inverter, neither NAND, NOR, XOR and XNOR with GLB. The metal lines are placed horizontally at the top and the bottom for the power supply (VDD) and ground (VSS). All of the layout heights of the standard cells are 3.69um that is the same as 130nm SMIC ones.

The leakage power dissipations of the two inverter standard cells are shown in Table 3 by using post-layout simulations. The inverter cell with GLB technology (INVX1_R) has a leakage reduction of 41.61%, compared with SMIC one (INVX1_SMIC13).

The leakage power of NAND and NOR standard cells are shown in Table 4. In Table 4,

Table 3: Leakage power of inverter standard cell using post-layout simulations (pW)

Input	0	1	Average
INVX1_R	62.75	48.82	55.78
INVX1_SMIC13	71.52	96.31	83.91

Table 4: Leakage power of NAND and NOR standard cells using post-layout simulations (pW)

Input	00	01	10	11	Average
NAND2X1_SMIC13	31.65	112.51	129.83	132.47	101.61
NAND2X1_R	22.40	64.95	71.19	78.75	59.32
NOR2X1_SMIC13	242.92	87.31	107.48	21.55	114.81
NOR2X1_R	131.24	48.9	48.29	20.34	62.19

Table 5: EDP comparisons of two XOR standard cells using post-layout simulations

Cell	Energy loss per switching (fJ)	Delay (ps)	EDP (pJs)
SMIC XOR	60.08	99.9	6
The proposed XOR	36.12	130	4.69

Table 6: The leakage power of two XOR cells using post-layout simulations (pW)

Cell	AB = 10	AB = 00	AB = 01	AB = 11	Average
SMIC XOR	641.14	701.11	841.75	563.23	686.8075
The proposed XOR	587.11	550.12	734.52	630.01	625.44

NAND2X1_SMIC13, NOR2X1_SMIC13 are 130nm SMIC NAND and NOR cells, respectively and NAND2X1_R, NOR2X1_R are the proposed NAND and NOR cells with the GLB technology, respectively. Compared with the 130nm SMIC standard cells, the leakage power of the proposed NAND and NOR cells with the GLB technology are reduced greatly.

The EDP of the SIMC and proposed XOR cells is compared in Table 5 by using post-layout simulations. The results show that the proposed XOR cell is better optimized than the SMIC one. The leakage power dissipations of the SIMC and proposed XOR cell are shown in Table 6. The leakage of the proposed XOR standard cell is lower than SMIC one expect for the state of AB = "11".

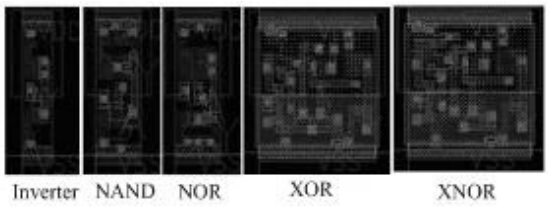


Fig. 6: The layouts of the proposed basic logic gate standard cells for SMIC 130 nm

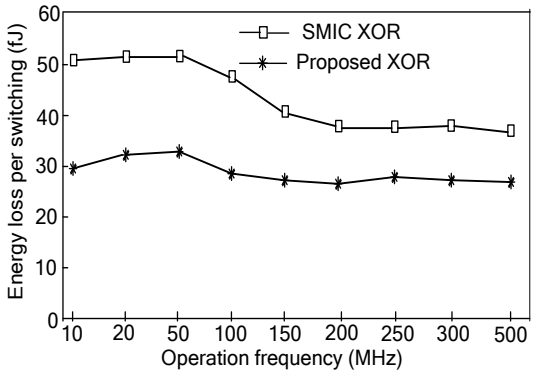


Fig. 7: Energy consumption comparisons of the two XOR cells using post-layout simulations

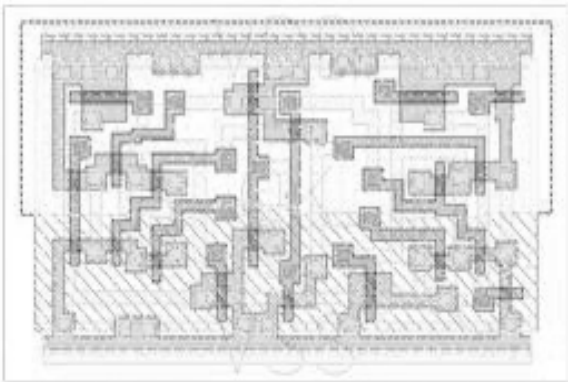


Fig. 8: The layout of TGMS-GLB

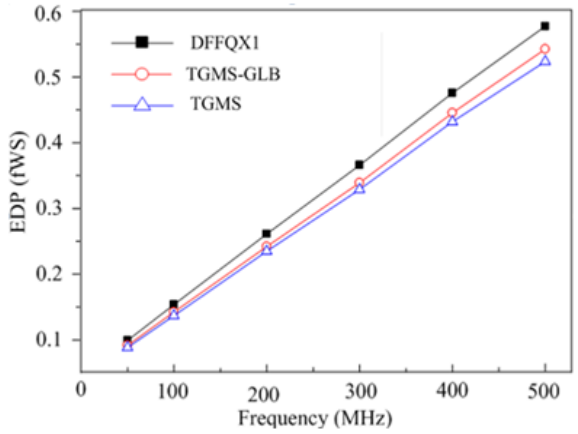


Fig. 9: EDP comparisons of the three flip-flop cells using post-layout simulations

Figure 7 shows the energy consumption comparisons of the XOR cells per switching from 10MHz to 300MHz. The proposed XOR cell performs lower energy consumption than the SMIC one in all operation frequencies.

Gate-length biasing flip-flop: The layout of the low-leakage flip-flop cell with GLB is shown in Fig. 8. The metal lines are placed horizontally at the top and the bottom for the power supply (VDD) and ground (VSS). The proposed low-leakage flip-flop with GLB (TGMS-GLB), Transmission Gate Master-Slave flip-flop without GLB (TGMS) and SMIC flip-flop (DFFQX1) have the same layout areas with 6.9μm×3.69μm.

The Energy Delay Product (EDP) of the three flip-flop cells are shown in Fig. 9 by using post-layout simulations. The results show that the low-leakage flip-flop cell with GLB has lower EDP than the SMIC one. Compared with the SMIC standard cell, the low-leakage flip-flop cell provides an EDP reduction of 11.6%.

STANDARD CELL DESIGNS

In this section, the design flow of the standard cells is presented. Taken an example, the standard-cell generation for the low-leakage flip-flop with GLB (TGMS-GLB) is presented in detail. The standard-cell design flow is shown in Fig. 10. The GDS database is generated by using the stream out function of IC5141. Then, the auto place and route (P&R) library is created using this GDS database. The layouts of the standard cells are verified by using the Calibre tool and spice netlists are generated from their layouts. The synthesis library is generated by using the liberty NCX and HSPICE.

After the layout design, the abstract view should be created in Library Exchange Format (LEF) for standard

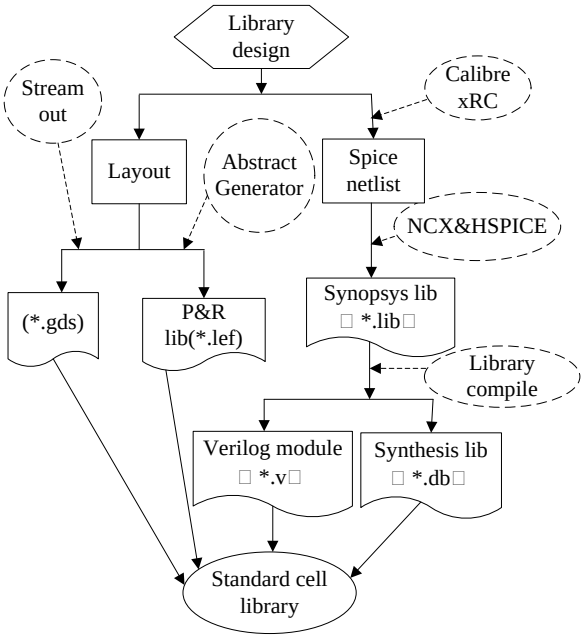


Fig. 10: Design flow of the standard cells

```
MACRO TGMS_GLB
  CLASS CORE ;
  FOREIGN TGMS 0 0 ;
  ORIGIN 0.0000 0.0000 ;
  SIZE 6.9000 BY 3.6900 ;
  SYMMETRY X Y ;
  SITE SMC13SITE ;
  PIN CK
    DIRECTION INPUT ;
    USE CLOCK ;
    PORT
    LAYER METAL1 ;
    RECT  3.345 1.700 3.555 1.990;
  END
  END CK
  PIN D
     DIRECTION INPUT ;
     … …
  END D
  PIN Q
     DIRECTION OUTPUT ;
     … …
     END
  END Q
PIN VDD
     DIRECTION INOUT ;
     USE POWER ;
     … …
     END
  END VDD
  PIN VSS
     DIRECTION INOUT ;
     USE GROUND ;
     … …
     END
  END VSS
END TGMS_GLB
```

Fig. 11: LEF tech files of the low-leakage flip-flop standard cell

cells. The generated abstracts are based on physical layout and logical data, process technology information. It is used in place of full layouts to improve the performance of place-and-route tools, such as Cadence Encounter. The LEF (Library Exchange Format) tech file can be read by the place-and-route tools. Therefore, LEF tech files should be generated for standard cells. The LEF tech file of the flip-flop standard cell is show in Fig. 11.

From the LEF file, we can see that all the all Pins are abstracted. In the LEF file, the size of the flip-flop cell is defined as 6.9 μm×3.69 μm. To perform characterization, Liberty NCX is used to run circuit

```
set input_library ../typical_1v2c25.lib
set output_library typical_1v2c25_out.lib
set model_file ../model.typ
set netlist_dir ../netlists
set simulator_exec ~/hspice/linux/hspice
set templates true
set output_templates true
set input_template_dir config
set timing true
set power true
set ccs_power false
set compact false
set ccs_timing false
set nlpm true
set nldm true
set variation_leakage false
```

Fig. 12: Template files of the liberty NCX

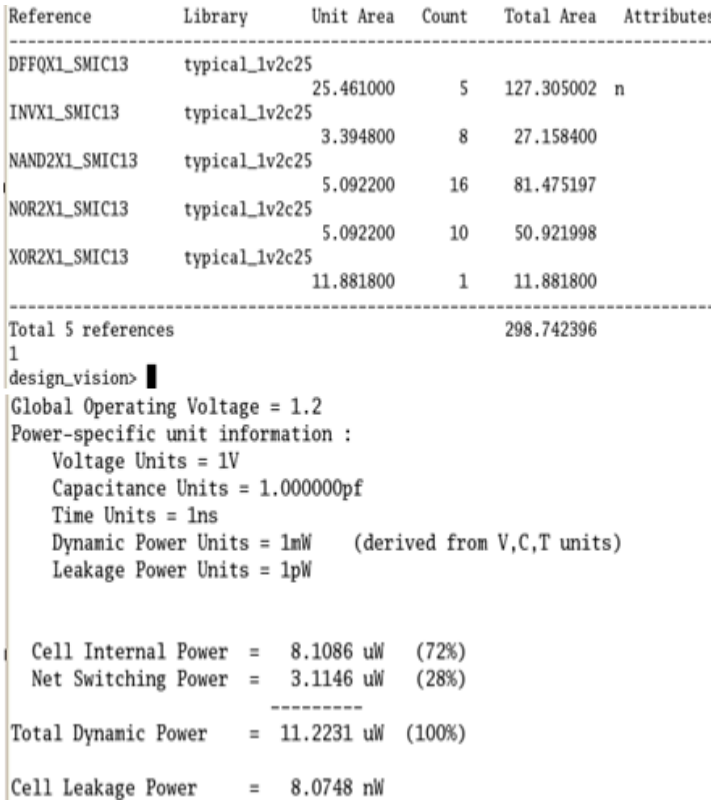
simulations for the library cells to determine the cell behavior. It writes out a description of the cell characteristics in the Liberty format (.lib). The library can then be used for timing, power and noise analysis with various tools such as Design Compile and Prime Time. In addition, Liberty NCX can convert existing libraries from one format to another. For a characterization task, the template file must specify the SPICE model file name, the SPICE net list directory and the SPICE simulator executable, as shown in Fig. 12. The input and output library names should be also specified.

After the characterization, we can get a library in the liberty format (.lib) that can be used for timing and power analysis with various tools such as Design Compile. We can use the Library Compile tool from Synopsys capture this liberty (.lib) file and translates them into Synopsys internal database (.db) format for synthesis.

MODE-10 COUNTER USING THE PROPOSED STANDARD CELLS

In order to estimate power information, a mode-10 counter is synthesized by using Design Compile. Figure 13 and 14 show the two synthesis results by using the SMIC 130 nm standard cells and the proposed standard cells, respectively.

As shown in Fig. 13 and 14, the area of the two results is the same and the leakage power and the total dynamic power of the mode-10 counter using the proposed standard cells provide a reduction of 21.27 and 3.06%, respectively. Although the dynamic power dissipation of the proposed standard cells only has a little reduction, they can achieve large total power savings because of their low leakages.

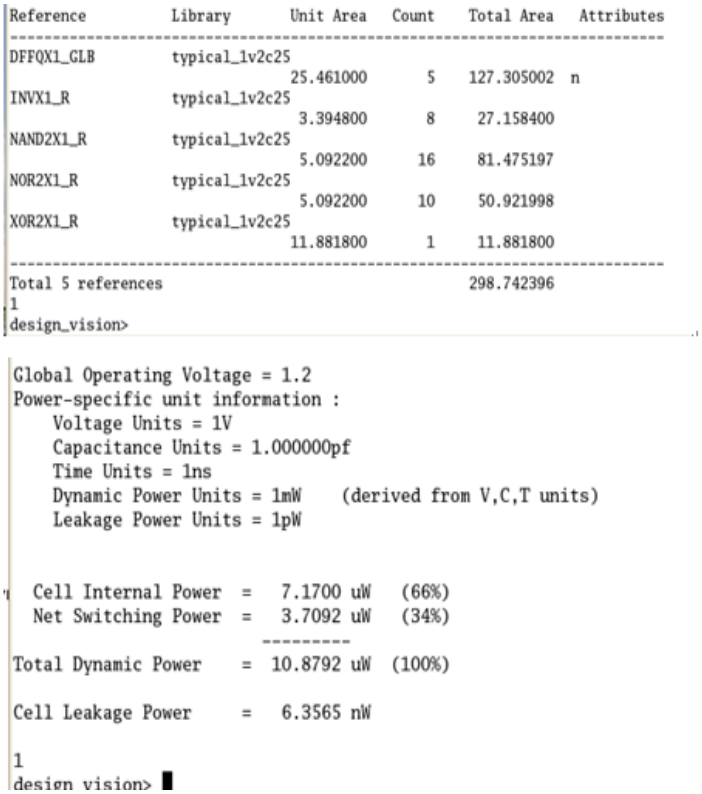


```
Reference          Library       Unit Area   Count    Total Area   Attributes
--------------------------------------------------------------------------------
DFFQX1_SMIC13      typical_1v2c25
                                 25.461000       5    127.305002  n
INVX1_SMIC13       typical_1v2c25
                                  3.394800       8     27.158400
NAND2X1_SMIC13     typical_1v2c25
                                  5.092200      16     81.475197
NOR2X1_SMIC13      typical_1v2c25
                                  5.092200      10     50.921998
XOR2X1_SMIC13      typical_1v2c25
                                 11.881800       1     11.881800
--------------------------------------------------------------------------------
Total 5 references                                    298.742396
1
design_vision> 
Global Operating Voltage = 1.2
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  =   8.1086 uW   (72%)
  Net Switching Power  =   3.1146 uW   (28%)
                         ---------
Total Dynamic Power    =  11.2231 uW  (100%)

Cell Leakage Power     =   8.0748 nW
```

Fig. 13: Design compile synthesis results of the mode-10 counter using the SMIC 130nm standard cells



```
Reference          Library       Unit Area   Count    Total Area   Attributes
--------------------------------------------------------------------------------
DFFQX1_GLB         typical_1v2c25
                                 25.461000       5    127.305002  n
INVX1_R            typical_1v2c25
                                  3.394800       8     27.158400
NAND2X1_R          typical_1v2c25
                                  5.092200      16     81.475197
NOR2X1_R           typical_1v2c25
                                  5.092200      10     50.921998
XOR2X1_R           typical_1v2c25
                                 11.881800       1     11.881800
--------------------------------------------------------------------------------
Total 5 references                                    298.742396
1
design_vision>

Global Operating Voltage = 1.2
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  =   7.1700 uW   (66%)
  Net Switching Power  =   3.7092 uW   (34%)
                         ---------
Total Dynamic Power    =  10.8792 uW  (100%)

Cell Leakage Power     =   6.3565 nW

1
design_vision>
```

Fig. 14: design compile synthesis results of the mode-10 counter using the proposed standard cells

CONCLUSION

Technology scaling increases the density and performance of integrated circuits, resulting in large power dissipations. Cell-based design flow has been widely used for digital chip designs with commercial EDA tools. In order to realize a low-power chip, low-power standard cell libraries are important.

In this study , a minimum set of low-power standard cells have been developed, which include basic logic gates such as inverter, NAND, NOR, XOR, XNOR and flip-flop. The proposed inverter, NAND, NOR and flip-flop standard cells are optimized to achieve low energy delay product (EDP) by using the gate-length biasing technique. The proposed XOR and XNOR standard cells are optimized based on transistor-level. The proposed several standard cells attain large leakage reductions. A mode-10 counter is verified with the proposed standard cells by using commercial EDA tools. The leakage and total dynamic power dissipations of the mode-10 counter using the proposed standard cells provide a reduction of 21.27 and 3.06%, respectively. The results indicate the proposed standard cells are a good choose in low power design.

ACKNOWLEDGMENT

This study was supported by the Key Program of National Natural Science of China (No. 61131001), National Natural Science Foundation of China (No. 61271137 and No. 61071049).

REFERENCES

Agarwal, A., C.H. Kim, S. Mukhopadhyay and K. Roy, 2004. Leakage in nano-scale technologies: Mechanisms, impact and design considerations. Proceeding of the 41st Annual Design Automation Conference, ACM-IEEE, New York, USA, pp: 6-11.

Fallah, F. and M. Pedram, 2005. Standby and active leakage current control and minimization in CMOS VLSI circuits. IEICE T. Elec., E88-C(4): 509-519.

Gupta, P., A.B. Kahn, P. Sharma and D. Sylvester, 2006. Gate-length biasing for runtime-leakage control. IEEE T. Comput. Aid. D., 25(8): 1475-1485.

Heo, S. and Y.S. Shin, 2007. Minimizing leakage of sequential circuits through flip-flop skewing and technology mapping. J. Semiconduc. Tech. Sci., 7(4): 215-220.

Hu, J.P. and J. Wang, 2011. Standard cell design of a low-leakage flip-flop with gate-length biasing. IEEE 9th International Conference on ASIC (ASICON), 25-28 Oct., Ningbo, China, pp: 361-364.

Jayakumar, N. and S.P. Khatri, 2007. A predictably low-leakage ASIC design style. IEEE T. VLSI Syst., 15(3): 276-285.

Kao, J. and A. Chandrakasan, 2001. MTCMOS sequential circuits. Proceeding of IEEE European Conference on Solid State Circuits, Neuchâtel, pp: 332-335.

Kim, H.O. and Y. Shin, 2007. Semicustom design methodology of power gated circuits for low leakage applications. IEEE T. Circuit Syst., 54(6): 512-516.

Nagarajan, C.S., L. Yuan, G. Qu and B.G. Stamps, 2009. Leakage optimization using transistor-level dual threshold voltage cell library. Proceeding of 10th International Symposium On Quality Electronic Design, Washington DC, USA, pp: 62-67.

Peiravi, A. and M. Assai, 2008. A novel circuit design technique to minimize sleep mode power consumption due to leakage power in the sub-100 nm wide gates in CMOS technology. World Appl. Sci. J., 4: 617-625.

Wang, J. and J.P. Hu, 2011. Low power designs of XOR and NXOR standard cells. Lect. Note Elec. Eng., 165: 947-954.

Wang, A., B.H. Calhoun and A.P. Chandrakasan, 2006. Sub-Threshold Design for Ultra Low-Power Systems. Springer-Verlag, New York.

Zhang, W.Q., L. Su, Y. Zhang, L.F. Li and J.P. Hu, 2011. Low-leakage flip-flops based on dual-threshold and multiple leakages reduction techniques. J. Circuit Syst. Comput., 20(1): 147-162.