

# ASK COMPATIBLE CMOS RECEIVER FOR 13.56 MHZ RFID READER

Nissar Mohammad Karim<sup>1</sup>, Mohd. Alauddin Mohd. Ali<sup>1,2</sup>, Mamun Bin Ibne Reaz,  
Selina Abdul Samad

Institute of Microengineering and Nanoelectronics, Department of Electrical,  
Electronic and Systems Engineering, Universiti Kebangsaan Malaysia, Bangi,  
Selangor D.E., Malaysia.

**Key words:** ASK, RFID, Receiver, 13.56 MHz, ISO/IEC 14443, CMOS.

**Abstract:** This study concerns about a high frequency companionable receiver architecture for RFID application, which is capable of dealing with most of the previous inadequacies. In this paper, an assessment of different receiver systems is shown and a simulated design of an integrated receiver for 13.56 MHz RFID Reader is proposed for 0.18 $\mu$ m CMOS technology. The design is mainly composed of amplifier, detector and digitizer. The system uses fewer components than that of other CMOS based RFID receivers and consumes a power of 0.325 mWatt at 1V biasing. Synthesized Results show smaller ripple (<0.0002%) than that of existing systems.

## ASK kompatibilen CMOS sprejemnik za 13.56 MHz RFID bralnik

**Ključne besede:** ASK, RFID, sprejemnik, 13.56 MHz, ISO/IEC 14443, CMOS

**Izveček:** Prispevek obravnava novo arhitekturo visokofrekvenčnega sprejemnika za RFID aplikacijo, ki odpravlja večino prejšnjih pomanjkljivosti. V tem članku je presojamo različne sprejemne sisteme in simuliramo koncept integriranega sprejemnika za 13.56 MHz RFID čitalnik izvedenaega z 0.18 $\mu$ m CMOS tehnologijo. Sistem je sestavljen iz ojačevalnika, detektorja in digitalizatorja. Naprava uporablja manj komponent kot RFID sprejemnik na osnovi CMOS tehnologije ter porabi 0.325 mWatt moči pri napetosti 1V. Rezultati pokažejo manjši šum (<0.0002%) kot pri obstoječih sistemih.

### 1 Introduction

Radio Frequency Identification (RFID) system has been heralded as a technology fit for the 21st century, offering variety of applications. In modern time, there has been an escalating impact on the expansion of RFID technology for the localization and the identification of objects. RFID is a broadly used technology, which employs radio signals for the identification of people or objects. Its utility is to facilitate data to be transmitted into devices, which is interpreted by an RFID reader. Among the three focal constituents of RFID, reader is one which transmits the signal and processes the received data from the tag. Processing and receiving of data is carried out by the receiver. To do this, RFID reader needs to extract the message signal from the carrier and to digitize the resulting data. Our research goal is to design 13.56 MHz compatible receiver for RFID reader. For the design of a complimentary-metal-oxide-semiconductor (CMOS) based 13.56 MHz RFID receiver, one of the basic requirements is to follow ISO/IEC 14443 standardization.

According to ISO/IEC 14443 standardization, a design of an RFID receiver is proposed in this study. The carrier signal from the RFID tag will be 13.56 MHz with a subcarrier frequency of 847.5 KHz. The modulation index has to be either ASK(Amplitude Shift Keying) 10% or ASK 100%. On the other hand, low ripple, faster settling time and low power

consumption are vital criterions in designing the system. So, the ultimate design challenge is to implement a receiver, which is compatible with ISO/IEC 14443 standardization, consumes less power, uses fewer components and shows low ripple.

From the recent literatures, we found, there were few researches on RFID receiver for high frequency (1MHz~20MHz) RFID operation. Though, till now, there are scopes to reduce ripple in detection and improve the performance in power consumption. Choi *et al.*, 2006 is one of those who accentuated on multi tag recognition and anti-collision protocols rather than focusing on detection and power consumption /2/. N.Roy *et al.*, 2006 delineated a mixed mode system by combining both digital and analogue components, which also overlooks the power criteria /3/. Meill'ere *et al.*, 2006 delineated a CMOS based 13.56 MHz RFID reader, whereas the receiver consists of rectifier, amplifier and comparator /4/. But, the number of MOSFETs used here is higher than those of the other receiver systems. The proposed demodulator by Y.Liu *et al.*, 2007 focused on FPGA implementation of receiver/5/ and like /2/, it did not consider the issue of detection. C. Mutti *et al.*, 2007 compared different detection algorithms, but this work was more towards theoretical implementation rather than real time nature /6/. One of the significant research execution was done by Alegre *et al.*, 2008 where a detector was designed, which can be

also used as a part of an RFID receiver [7]. This research is noteworthy because of its low ripple at the output. System designed by Seo *et al.*, 2008 showed an RFID reader, compatible for different standardization, though regarding ripple and settling time, it stated nothing [8]. From the literature review, we found that most of the researches went through either FPGA (Field Programmable Gate Array) implementation or theoretical execution. From the preceding literature review, we can say that, only few of these papers went through the practical design of receiver for 13.56 MHz RFID reader. So, our aim is to design a CMOS based RFID receiver which attunes with ISO/IEC 14443 standardization, employs fewer components, consumes less power and confirms less ripple.

## 2 Proposed Methodology

Fig 1 depicts the block diagram of the proposed receiver, which is mainly comprised of an amplifier, a detector, and a digitizer. The ASK modulated signal, coming from the tag has a carrier frequency of 13.56 MHz with a subcarrier frequency of 847.5 KHz. The OpAmp( Operational Amplifier) used in the amplifier, takes the ASK signal and boosts it up. The boosted up signal is then sent to the detector, which detects the peak and free the wave from the carrier. The digitizer compares the signal coming from the detector, with a reference voltage and shapes the wave. The output of the digitizer is set to a digital OR gate, which completely digitizes the wave. In the upcoming sections we are going to discuss the whole system in details.

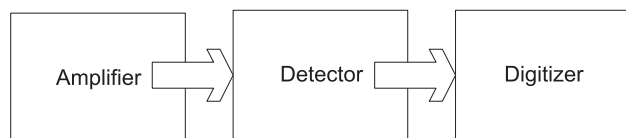


Fig 1 Block Diagram of the Proposed Receiver

### 2.1 Amplifier

We used amplifier in the receiver circuit to increase the power of the RF signal. It takes the signal from the tag via an antenna and a bypass capacitor. The bypass capacitor C1 is used here to illuminate the DC component. This capacitor is connected with the positive terminal of the OpAmp[9], whereas the OpAmp is constructed by transistors (M1-M10). The OpAmp mainly consists of three different components; which are 1. Differential Amplifier Block 2. Single Ended Conversion Block and 3. Gain Stage. The 1st block contains a differential pair (M4,M5), a current mirror (M1,M3,M7,M8) and a current source (M2). Current source is aided by active resistors (M1 and M6) to generate reference current for the current mirror. For obtaining high voltage gain, we used the current mirror. M4 and M5 are those inputs, which are used for inverting and non-inverting mode respectively. Capacitor C0 is used to ensure stability for the feedback. The Single Ended Con-

version Block produces a single output and gives necessary gain for the Gain Stage. The gain stage is comprised of M3 and M10. The high output resistance of these two transistors brings a large gain. The OpAmp works in non-inverting mode. In case of non-inverting amplification in OpAmp, the gain can be given as,

$$G = 1 + R1 / R2 \quad (1)$$

In equation (1), R1 is the feedback resistance and R2 is connected with ground and R1. The values of the resistors are set in such a way that, the gain gets attuned at a compatible range, which can give a proper amplification of power for the detector. Fig 2 shows the schematic of the amplifier.

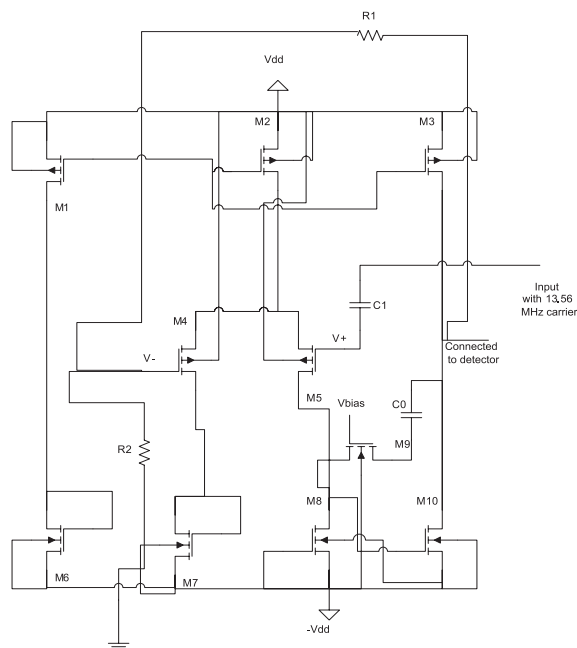


Fig 2 Schematic for the Amplifier

Table 1 shows the type, width and length of the MOSFETs used in the amplifier, where M2 works as a current source and its' width (W) and length (L) are set in such a way that the reference current coming from M2 is 50 μA. At the same time, same amount of current passes through M1, as the W and L of M1 is equal to that of M2. To obtain a higher current (twice of reference current) at M3, the width must be double than that of M2. The W/L ratio for M7 and M8 is set identical to obtain a mirror of the input current at output. M3 and M10 have a higher W/L ratio which helps to obtain a higher gain.

### 2.2 Detector

The detector illuminates the carrier and keeps only the message signal in an analogue form. The circuit mainly contains a PMOS M11, a resistor R3 with two capacitors C2 and C3 respectively as depicted in Fig 3. C3 acts as a bypass capacitor. Source and gate of the PMOS M11 are shorted together, which forms a p-n junction. Its drain is connected to resistor R3 and Capacitor C3.

Table 1 Type, Width and Length Of The MOSFETS

MOSFET	Type	Width(μm)	Length(μm)
M1	p-type	35.64	0.96
M2	p-type	35.64	0.96
M3	p-type	72	0.96
M4	p-type	7.44	0.96
M5	p-type	7.44	0.96
M6	n-type	1.56	3.12
M7	n-type	5.28	0.96
M8	n-type	5.28	0.96
M9	n-type	2.64	2.16
M10	n-type	21.12	0.96

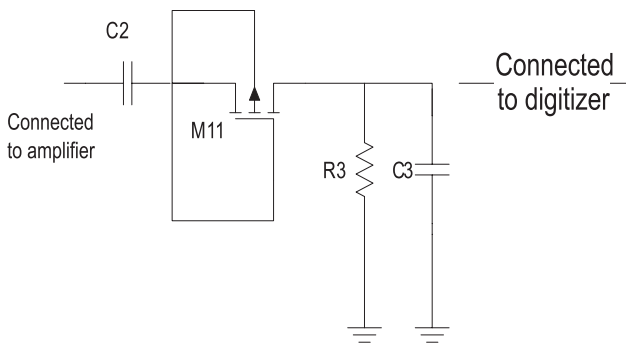


Fig 3 Schematic for the detector.

The configuration of detector is similar to a conventional envelope detector with a change in width (*W*) and length (*L*) for PMOS. To obtain a high drain current, *W/L* ratio is kept high. As *W/L* ratio is directly proportional to the drain current, when there is a high frequency input signal, the rectification and detection process become more accurate. On the other hand, the output of the detector is connected with an amplifier. Amplifier needs a high input current to be boosted up. Increasing *W/L* will give high output current for the detector. This can be explained by

$$I_{ds} = uC_{ox}(W/L)[(V_{gs} - V_t)V_{ds} - (V_{ds}/2)V_{ds}] \tag{2}$$

When

$$0 < V_{ds} < V_{gs} - V_t,$$

Where,

- $I_{ds}$  = Drain Current,
- $u$  = Mobility (Carrier),
- $C_{ox}$  = Oxide Capacitance,
- $V_{gs}$  = Gate to Source Voltage,
- $V_t$  = Threshold Voltage,
- $V_{ds}$  = Drain to Source Voltage

From (2), it can be stated that  $I_{ds}$  is directly proportional to *W/L* ratio. Hence, increasing *W/L* will increase the drain current, which also provides high input current for the amplifier.

### 2.3 Digitizer

The digitizer compares the detected signal with respect to a reference voltage and passes the signal to an OR gate. In our proposed design, we employed an OpAmp(constructed of *M1-M10* in Fig 4) to execute the function of comparator, whereas the reference voltage was set with an inverting terminal of the OpAmp. The non-inverting terminal receives the signal coming from the detector. The endpoint of the comparator is affixed with an input of an OR gate. When the compared value is higher than that of reference voltage, the comparator gives a high signal. On the other hand, the comparator shows a lower signal; when the compared value is lower than that of reference voltage. The output generated from the comparator is sent to the OR gate to smooth the signal. The *W* and *L* of the transistors are equal to that of amplifier.

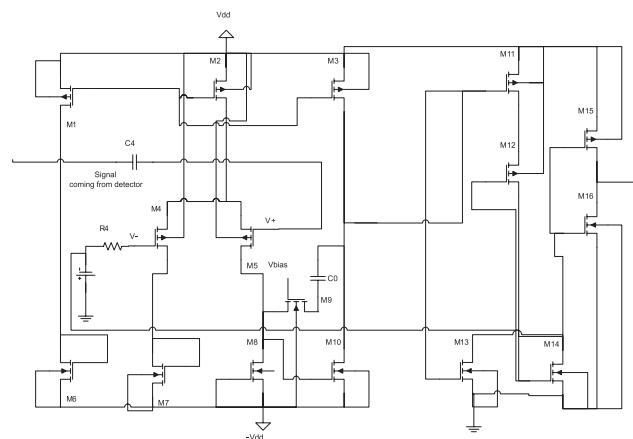


Fig 4 Schematic for the Digitizer

### 3 Results and Discussions

Mentor Graphics EldoSpice is used to simulate the proposed circuit in 0.18 μm CMOS technology, with one poly and two metal layers. Thick oxide layer is used to shield the transistors from high current. Each transistor is enclosed within its own individual deep well. The proposed

receiver is designed with the following component values:  $C_0=100$  fF,  $C_1=10$  nF,  $C_2= 1000$ nF,  $C_3=1$ nF,  $R_1= 1$ K,  $R_2= 1$ K and  $R_3= 10$ K. Fig 5 shows the chip micrograph with an active area of 0.440200 mm<sup>2</sup> (Including bonding pads).

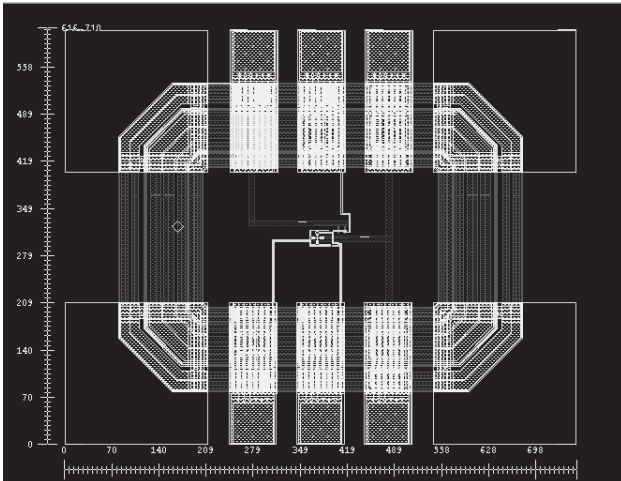


Fig 5 Chip Micrograph

The system is evaluated by using ASK modulated signal with a square-wave baseband and sine wave carrier signal. Fig 6(a) and 6(b) shows the representation for input and output voltage waveforms respectively. In simulation, it has been considered that the input waveform has 0.2V amplitude, 13.56 MHz carrier and 200 KHz baseband signal.

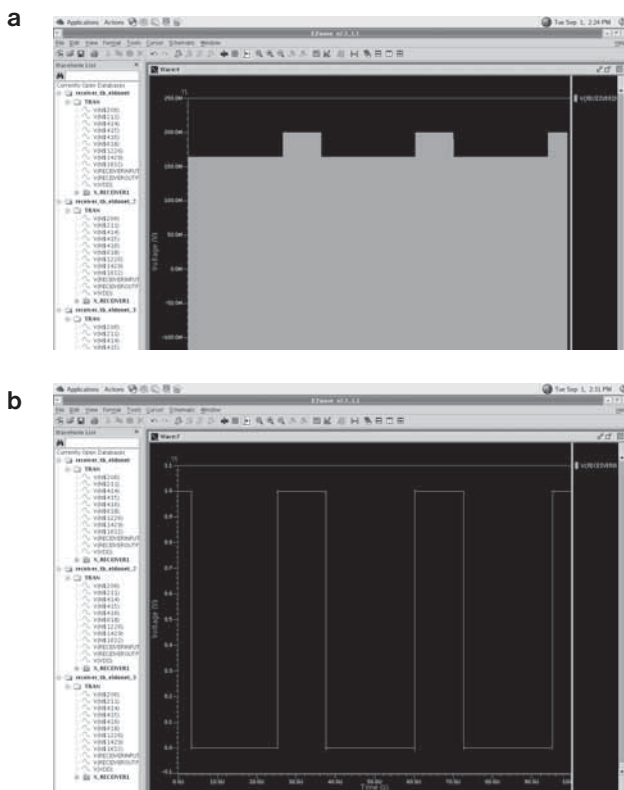


Fig 6 (a) Modulated Waveform (b) Receiver Output.

When this signal is used as an input, the output signal obtains a ripple of 0.005%. The ripple is appraised by taking the ratio of ripple voltage and dc voltage of the output waveform as shown in equation (3), where  $r$  stands for ripple,  $V_r$  is the ripple voltage and  $V_{dc}$  is the dc voltage.

$$r = \frac{V_r}{V_{dc}} \quad (3)$$

(3)Fig 7 shows the transfer characteristics, where noise (in dbc) vs. frequency graph is plotted. From this graph it is visible that at a very low frequency noise is high. As the frequency increases, the noise decreases. The frequency compatibility for the system is 5 KHz to 20 MHz.

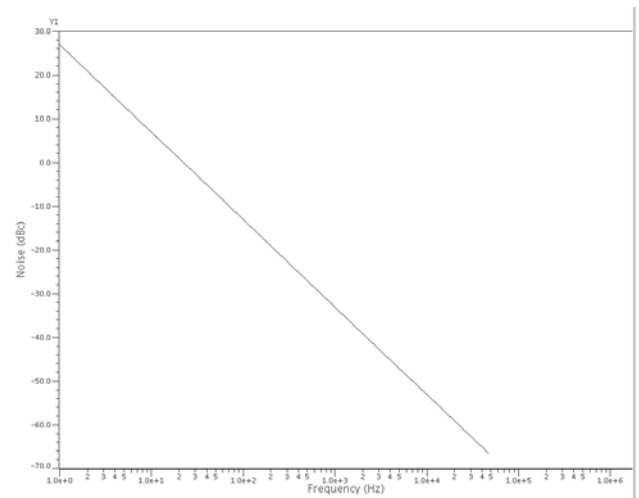


Fig 7 Noise Vs Frequency Graph

The receiver can extract the baseband signal from the carrier signal at 10% modulation index consuming 0.325 mWatt power. The total power consumption can be explained by equation (4),

$$P_{tot} = P_s + P_d + P_{SC} \quad (4)$$

Here,

$P_s$  = Static Power Consumption =  $n(\text{Leakage Current} \times \text{Supply Voltage})$

$P_d$  = Dynamic Power Consumption =  $C_L V_{dd}^2 f_r$

$P_{SC}$  = Short Circuit Power Consumption =

Where,  $n$  = Number of MOSFETs,  $C_L$  = Load Capacitance,  $V_{dd}$  = Biasing Voltage,  $f_r$  = Repetition Frequency,  $\mu$  = Effective Surface Mobility,  $C_{ox}$  = Oxide Capacitance,  $V_t$  = Threshold Voltage.

Based on these facts and accessible data, Table 2 has been constructed which portrays the comparison between this work and the prior works in which our implemented demodulator shows better performance and accomplishes the requirements of ISO 14443 standardization.

Table 2 Comparison of the Prior Works

Source	Modulation Index(%)	Carrier (MHz)	Data Rate (Kbps)	Number of MOS	Power Consumption	Ripple Voltage at HF
Meill`ere <i>et al.</i> [6]	100	13.56	106	>40	5.3 mWatt	-
Alegre <i>et al.</i> [7]	100	10	-	>50	2.49 mWatt	0.3%
Seo <i>et al.</i> [8]	10, 100	13.56	106	>30	-	>1%
This Work	10	0.5 -13.56	106	21	0.325 mWatt	0.00019%

#### 4 Conclusion

In this paper, an integrated receiver structure has been proposed for the use in a 13.56 MHz RFID reader. At 13.56 MHz frequency, the design shows less ripple and faster settling time than that of existing systems. Experimental results from the post-layout simulation are with good agreement on modulation index, frequency and data rate. So, it can be concluded that, the proposed system gives high-quality performance in terms of ripple and power consumption by following the standardization of ISO/IEC 14443.

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Nissar Mohammad Karim<sup>1</sup>, Mohd. Alauddin Mohd. Ali<sup>1,2</sup>, Mamun Bin Ibne Reaz, Selina Abdul Samad

Institute of Microengineering and Nanoelectronics,  
Department of Electrical, Electronic and Systems  
Engineering, Universiti Kebangsaan Malaysia,  
Bangi,Selangor D.E., Malaysia.  
nissarkarim@yahoo.com

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