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Temperature and voltage dependences of the capture and emission times of individual traps in high-k dielectrics

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ABSTRACT

Quantized threshold voltage (VTH) relaxation transients are observed in nano-scaled field effect transistors (FETs) after bias temperature stress. The abrupt steps are due to trapping/detrapping of individual defects in the gate oxide and indicate their characteristic emission/capture times. Individual traps are studied in n-channel SiO_2/HfSiO FETs after positive gate stress to complement previous studies performed on SiO(N). Similarly to single SiO(N) traps, strong thermal and bias dependences of the emission and capture times are demonstrated. The high-k traps have a higher density but a reduced impact on VTH due to their separation from the channel.

1. Introduction

As the dimensions of metal oxide semiconductor field effect transistors (MOSFETs) shrink toward the nanometer scale, the discrete behavior of individual defects is revealed. Quantized threshold voltage V_{TH} transients after bias temperature stress have been observed in deeply scaled MOSFETs due to the emission and capture of *individual* carriers in gate oxide traps [1–4]. This phenomenon has been explored to study the statistical properties of single traps in MOSFETs [5–7] after bias temperature stress. A new technique named time dependent defect spectroscopy (TDDS) has been developed and successfully applied on SiO(N) p-channel (pFETs) [6,7] and n-channel FET (nFETs) [5] after negative and positive gate stress, respectively.

In this work, we first present a statistical comparison of the discrete threshold voltage shifts in a larger number of SiO(N) nFETs and, technologically more relevant, SiO_2/HfSiO nFETs after positive bias stress. Even though the trap density in HfSiO is larger, they have a reduced impact on the total threshold voltage shift due to their larger separation from the channel. Next, a set of individual traps in a single SiO_2/HfSiO nFET is analyzed. Similarly to the SiO(N) traps, the emission and capture times of high-k traps show strong thermal and bias dependences.

2. Experimental

In our experiment a DC signal was applied to the gate of nFETs with 1.8 nm-SiO(N) or 0.8 nm-SiO_2/1.8 nm-HfSiO gate dielectrics. The drawn gate dimensions for both cases were $L \times W = 70 \times 90\ nm^2$. A stress signal V_{STRESS} was applied for a stress time t_{STRESS}. Afterward, the relaxation transient was measured at V_{RELAX} for a relaxation time t_{RELAX}. The drain voltage V_D was 0.1 V. During this entire process the source current I_S was registered and transformed into a V_{TH} shift via a reference I_S–V_G curve of the device taken prior to stress [8]. The V_{RELAX} was chosen close to the threshold voltage V_{TH} of the device so that ΔI_S varies strongly with respect to the absolute value of I_S. Keithley 2602 source-measure units were used for this experiment.

3. Statistical comparison of SiO(N) and SiO_2/HfSiO nFETs

Fig. 1 shows the typical relaxation transients obtained on (a) SiO(N) and (b) SiO_2/HfSiO stacks under the gate oxide electric field of 13 MV/cm for 240 ms. The V_{TH} transients show a discrete behavior due to electron emission from individual traps [2]. As opposed to the clean V_{TH} relaxation traces obtained in SiO(N) nFETs, the high-k stacks present a higher level of noise. When the V_{TH} step heights are displayed in a complementary cumulative plot normalized to the number of traces (see Fig. 2), it is observed that the number of steps, i.e., traps, after identical stress conditions (the

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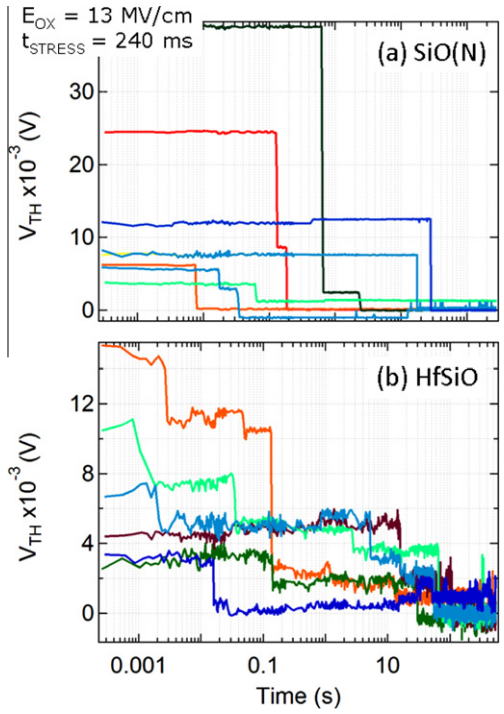

Fig. 1. Typical relaxation transients obtained in different (a) SiO(N) and (b) SiO_2/HfSiO stacks. Larger noise due to the higher trap density in the high-k dielectric (see Fig. 2) is observed in the HfSiO nFETs with respect to the clean SiO(N) traces.

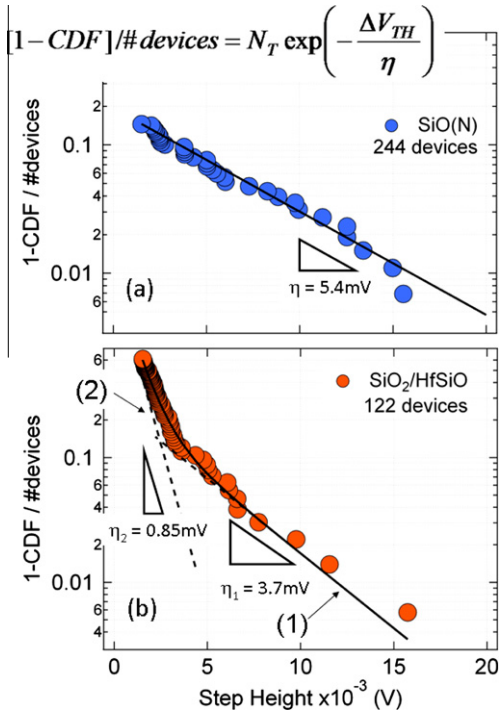

Fig. 2. Complementary cumulative distribution functions (CCDF) normalized to the number of devices of V_{TH} step heights larger than 1.5 mV for (a) 244 SiO(N) and (b) 122 SiO_2/HfSiO nFETs. Note that the number of traps is larger for SiO_2/HfSiO stacks than for SiO(N) devices. Complementary CDF for SiO(N) follows an exponential distribution [9] with average value $\eta = 5.4$ mV. For the SiO_2/HfSiO stacks, the data can be fitted to a bimodal exponential distribution with $\eta_1 = 3.7$ mV and $\eta_2 = 0.85$ mV. The number of steps per device N_{T2} is 10 times larger than N_{T1}.

electric field and time) is larger for the HfSiO stacks than for the SiO(N) stacks. Indeed a significant number of SiO(N) devices did not show any step. The step heights for SiO(N) shown in Fig. 2a

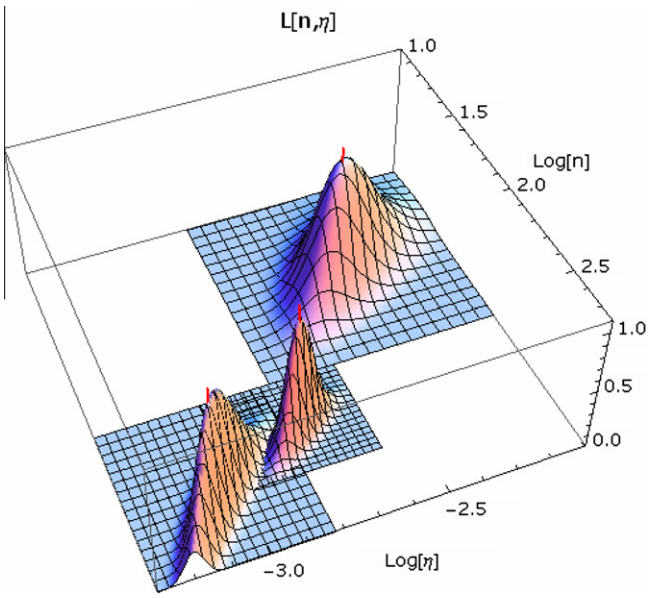

Fig. 3. 3D plot of likelihood functions in terms of (n, h) pairs shows distinctive power of ΔV_{TH} step statistic between null hypothesis of a single distribution mode and alternate hypothesis of two modes. The midde shape shows the likelihood region for a single common (n, h) pair, the two others that for each of the two bimodal distribution components. The mutual overlap between the three regions is almost nonexistent, revealing bimodality with very high significance.

follow an exponential distribution [9] with an average value η of 5.4 mV and a trap density $N_T = 0.19$ trap/device. However, a clearly *bimodal* distribution can be observed for HfSiO. Each mode can be fitted by means of the maximum likelihood method using two exponential distributions with $\eta_1 = 3.7$ mV and $N_{T1} = 0.3$ trap/device and $\eta_2 = 0.85$ mV and $N_{T2} = 2.6$ trap/device, respectively. Fig. 3 shows the likelihood functions assuming a monomodal distribution and a bimodal distribution for the step heights detected in the high-k stack. The no overlap among the regions strengthens the bimodality assumption with a high level of significance. Distribution 1 (η_1) is similar to SiO(N), both in η and in magnitude N_T. We therefore argue that this is due to defects in the SiO_2 layer. Since the η value is related to the centroid (x_0 distance from the gate) of the trapped electrons in the dielectric [4,10], i.e., $\eta \propto x_0$, distribution 2 corresponds to the defects in the high-k dielectric (η_2). Also it is worth noting that the number of steps per device N_{T2} is 10 times larger than N_{T1}. This indicates a higher density of traps in the high-k dielectric. However, the impact on the total V_{TH} is reduced since η_2 is significantly lower. Therefore, the large density of high-k traps with a small impact on the V_{TH} explains the larger noise level observed in the high-k stack (Fig. 1b).

4. Individual traps in a single SiO_2/HfSiO nFET

Fig. 4 shows three typical relaxation curves taken on a single SiO_2/HfSiO nFET. Under the conditions of the experiment, the selected device has four active traps with V_{TH} step heights lower than 4 mV. From the bimodal distribution shown in Fig. 2b, the probability of observing a high-k trap with a V_{TH} step height of 2 mV or lower is significantly larger than for SiO_2 traps. This suggests that there is a high probability that the traps observed in Fig. 4 are located in the high-k material.

As in the case of SiO(N) devices [5], every high-k trap has its characteristic emission time and V_{TH} shift, which form the 'fingerprint' of the defect (see Fig. 5a). However, the extracted clusters are not as compact as those observed in SiO(N) due to the higher level

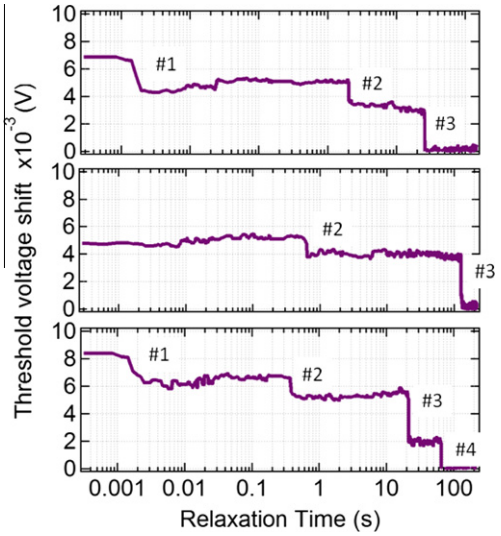

Fig. 4. Three typical V_{TH} transients after applied V_{STRESS} = 1.8 V (E_{OX} = 7 MV/cm) for 189 ms at 25 °C to a single high-k device. Up to four traps were active under the conditions of the experiment in this device. Note that their step heights are lower than 4 mV. Based on the bimodal distribution of Fig. 2b, we argue that the majority of these traps are in the high-k layer.

of noise present in the high-k stack. Note that all four clusters in Fig. 5a shift to shorter emission times with increasing temperature (Fig. 5b). Trap #1 shifts out of the experimental window, while a new trap #5 appears. Fig. 6a shows the histogram of the emission times t_e of the trap #3 for two t_{STRESS} values. As expected for Markov processes [7,11], the emission times can be fitted to an exponential distribution in order to obtain the characteristic emission time τ_e. Similarly to SiO(N) [5], the emission time τ_e is independent of the stress time. Fig. 6b displays the Arrhenius plot of the characteristic emission time τ_e. It presents a strong thermal activation with E_A = 0.48 eV. Fig. 7 shows that the intensity of the cluster associated with trap #3 increases with stress time up to the saturation level determined by the characteristic emission (τ_e) and capture (τ_c) times at V_{STRESS} as shown in the equation of Fig. 7 [11]. These characteristic times are strongly temperature (Fig. 7a) and voltage (Fig. 7b) dependent. The reduction of the occupancy with temperature is related to a higher activation energy of τ_e with respect to τ_c. The P_C increase with V_{STRESS} is due to the decrease of τ_c with increasing V_{STRESS}.

Interestingly, in Fig. 5b, a new trap (trap #5) that causes a negative V_{TH} shift appears in the TDDS spectrum at high temperature. We hypothesize that this effect is due to electron discharge from the dielectric to the gate during stress [12]. Therefore, electron emission takes place during stress condition and electron capture occurs during relaxation. As we will see in the following, this trap follows analogous kinetics as the other four (#1–4). Fig. 8 shows the intensity of cluster #5 as a function of the stress time for different temperatures. The emission probability increases with t_{STRESS} and can be described by the equation given in Fig. 7 after exchanging the capture and emission times. Again, this process is clearly thermally activated as shown in the Fig. 9. In the inset of Fig. 9, the histogram of the capture times shows that the capture process can also be described by an exponential distribution. The activation energy obtained from the fit of the data to an Arrhenius law is 0.8 eV. The activation energies found in this study are close to the values obtained in SiO(N) pFETs after negative stress [6,7], and those of SiO(N) nFETs after positive stress [5].

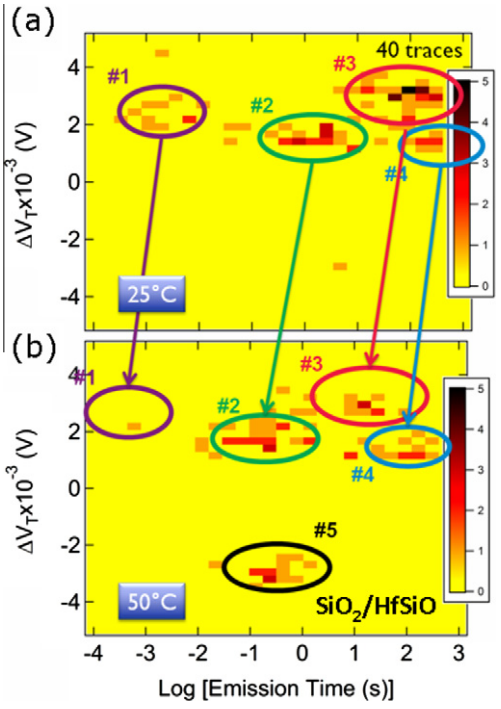

Fig. 5. TDDS spectra [6,7] of a single SiO_2/HfSiO stack at two temperatures extracted from 40 recovery traces under the bias and timing conditions of Fig. 4. At 25 °C (a), four homogenous clusters appear indicating the presence of four active traps under the conditions of the experiment. At 50 °C (b), a new cluster emerges (trap #5), which remarkably produces a negative V_{TH} shift. All the clusters shift to shorter emission times with temperature. Trap #1 even shifts out of the experimental window.

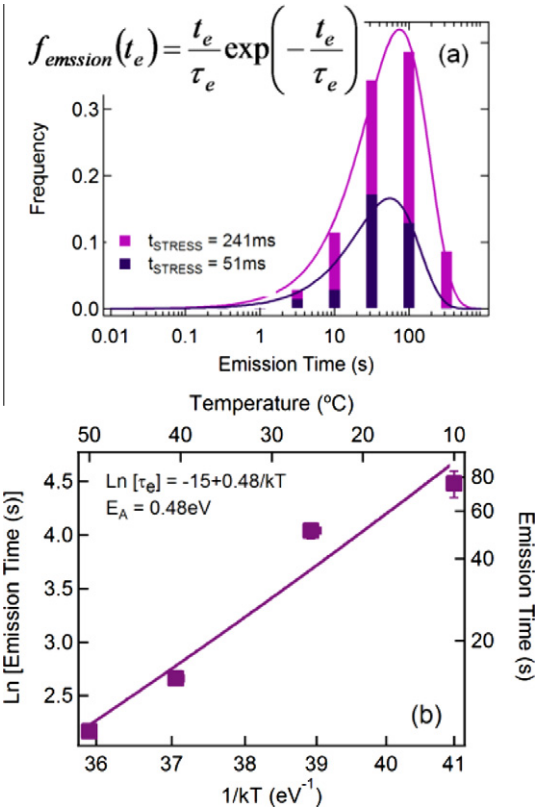

Fig. 6. (a) Histogram and (b) Arrhenius plot of the emission times t_e under the condition of Fig. 4. The histogram when plotted on the logarithmic scale matches with the theoretical expression shown in the inset [11]. Note that the emission times are independent of the stress time (a) but strongly dependent on temperature (b).

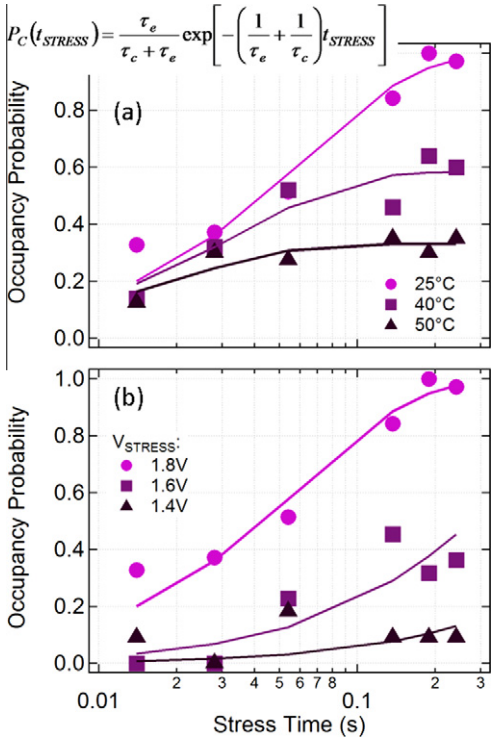

Fig. 7. (Symbols) Trap occupancy probability P_C of trap #3 vs. t_{STRESS} at conditions of Fig. 4 for different (a) temperatures and (b) V_{STRESS}. P_C increases with t_{STRESS} up to a saturation level dictated by the characteristic τ_e and τ_c times. These times depend strongly on temperature and V_{STRESS}. (Lines) Fit to the data according to the equation shown in the inset [11].

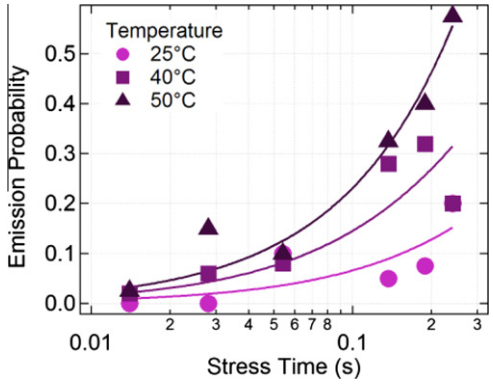

Fig. 8. Emission probability P_E of trap #5 vs. t_{STRESS} for the stress conditions of Fig. 4 for different temperatures. Emission increases with stress time and temperature. (Lines) Fit to the data according to the equation shown in the inset of Fig. 7 after exchanging τ_e and τ_c times.

5. Conclusion

We have shown that SiO_2/HfSiO nFET traps are located both in the SiO_2 and in the high-k dielectric. High-k traps have a reduced impact on the V_{TH} shift after stress but produce a high level of noise in the source current. We have demonstrated that the statistical properties of individual traps in SiO(N) and HfSiO dielectrics after positive stress follow analogous kinetics as described by Markov processes.

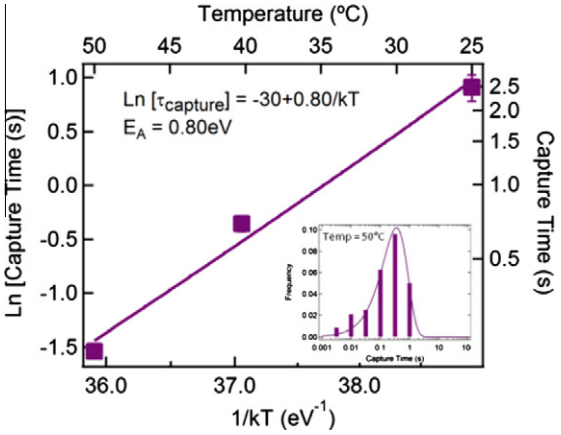

Fig. 9. Arrhenius plot of the electron capture time during relaxation. Inset shows that this process follows identical statistics as the emission times in Fig. 6.

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