Edited by T. Grasser and S. Selberherr - September 2007

Strain Induced Drain-Current Enhancement Mechanism in Short-Channel Bulk Ge-pMOSFETs with Different Channel and Surface Orientations

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Abstract

Self-consistent full-band Monte Carlo (with multi-subbands) device simulations were performed to clarify the mechanism of drain-current enhancements for uniaxially strained bulk Ge-pMOSFETs with different channel/surface orientations. Unlike any conventional mobility studies, our device simulation enables us to probe fundamental roles of source-injection and channel backscattering in the practical bulk-MOSFET device structures with optimized channel/surface selections.

1 Introduction

Recently, germanium has been considered as an alternative material to overcome the scaling limit of conventional Si-pMOSFETs[1, 2]. Some theoretical studies have already been reported mostly for ideal UTB Ge-channel DG-MOSFETs[3, 4]. This paper, however, presents precise device simulation analysis for short-channel "bulk-type Ge-pMOSFETs" intending more practical comparative study with Si-MOSFETs by means of the essential features of MOSFETs, i.e., source injection velocity and backscatterings, for understanding strain-effects on source-drain current (I_{sd}) in the Ge-MOSFETs far more in-depth than a simple mobility notion. Using a newly developed full-band Monte Carlo (MC) device simulation program considering confinement quantum effects[5] for Ge-pMOSFETs, uniaxially stressed $\langle 110 \rangle$- and $\langle 100 \rangle$-channel devices have been simulated under a low or high drain-bias (V_{d}) condition.

2 Simulation Method

Based on our previous work[5], strained Ge-pMOSFETs were modeled by using the empirical pseudo-potential full-band–structure calculations and one-particle Monte Carlo procedure for I_{sd} calculation[6] (Fig. 1). Identical device geometry and doping structure are assumed for both Si and Ge calculated devices with channel-length (L_{ch}) of 30 nm and gate-dielectrics of EOT = 1.2 nm. Three valence bands of heavy-hole (HH), light-hole (LH), and split-off (SO) hole band are considered. The intra- and inter-subband/valley scatterings by acoustic- and optical-phonon interactions are incorporated into this simulation program. Since Ge has smaller density-of-states and lighter

hole mass compared with Si (Fig. 2), a quasi-Fermi energy in the Ge-devices tends to be higher than in the Si-devices at the source/drain regions of the same doping concentration. Thus, we applied different gate-biasing (V_g) for the Ge-devices ($V_g = -0.78\,\mathrm{V}$) as for intending reasonable comparison to the Si-devices ($V_g = -1.0\,\mathrm{V}$) with the same channel carrier concentrations.

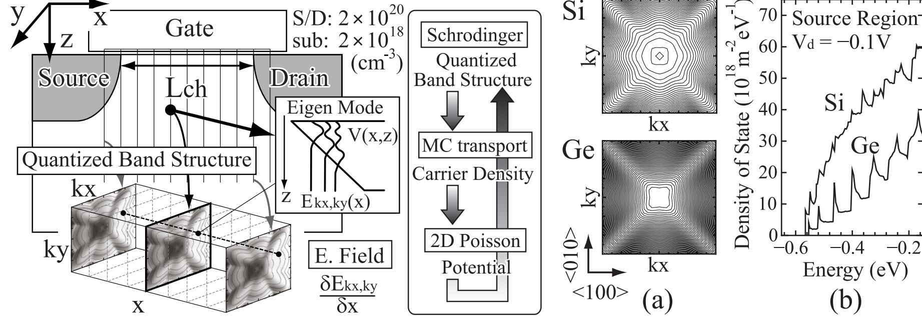

Figure 1: Simulated device structure. Quantized band structures are obtained by solving 1D Schrödinger equation with the empirical pseudo potential Hamiltonian along the z-direction at each x-mesh point. Plane wave approximation is applied for the y-direction.

Figure 2: (a) Quantized band structure $E_{kx,ky}(x)$ (lowest HH subband) contour map with 10 meV energy spacing. (b) The total density-of-states including all subbands of HH, LH and SO bands.

3 Results and Discussion

Strain-Induced I_{sd} Enhancement Mechanism: Under low V_d condition ($V_d = -0.1\,\mathrm{V}$), strain-induced I_{sd} shows similar characteristics for both Si- and Ge-pMOSFETs with (001)-surface channel, while the Ge-device shows about 100 % higher I_{sd} at zero-stress (Fig. 3). Our MC-simulation reveals that the source-injection velocity, v_{inj}, plays a dominant role for I_{sd} enhancement characteristics both in Si- and Ge-cases (Fig. 4), however a pronounced difference can be seen in backscattering kinetics (Fig. 5 (a)). Backward/forward current ratio, $I_{back}/I_{forward}$, at the bottleneck point, which is relevant to the backscattering rate, is less sensitive to the applied stress, especially in the Ge-case where $I_{back}/I_{forward} < 0.4$ which is smaller than in the Si-case ($I_{back}/I_{forward} \sim 0.6$). This efficient carrier transport in the Ge-pMOSFETs is supported by the longer mean-free-path, λ_{mfp}, (Fig. 5 (b)) which is attributed to the smaller scattering rate (density-of-states) and the higher hole velocity (small mass). Thus, because of the sufficiently long λ_{mfp}, $I_{back}/I_{forward}$ is shown to be not altered by the applied stress in the Ge-case, in contrast to the Si-case with a shorter λ_{mfp}.

Channel-Direction Anisotropy: Under higher V_d-condition ($V_d = -0.5\,\mathrm{V}$), I_{sd} for the unstrained $\langle 100 \rangle$-channel is about 10 % larger than that for $\langle 110 \rangle$, while this relation becomes reversed under the high-compressive stress of over 0.5 GPa (Fig. 6). The I_{sd} anisotropy in the unstrained channel originates from the difference in the average

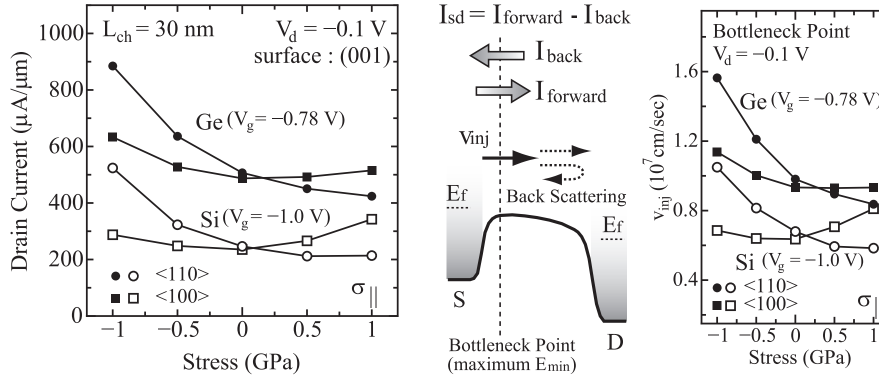

Figure 3: Simulated I_{sd} of $\langle 110\rangle$ (circular symbols) and $\langle 100\rangle$ (square symbols) channel device ((001)-surface) at $V_{\mathrm{d}} = -0.1\,\mathrm{V}$. Plus and minus signs for the stress axis represent tensile and compressive values, respectively.

Figure 4: v_{inj} is defined by the averaged positive velocity at the bottleneck point where E_{min} becomes maximum. Stress dependence of v_{inj} showing similar tendency to that of I_{sd} (Fig. 3).

carrier velocity at the channel region caused by the strong drain electric field, which concentrates holes in higher momentum region along the channel direction where the effective mass anisotropy becomes significant (Fig. 2 (a)). In fact, v_{max} in the unstrained $\langle 100\rangle$-channel is about 30 % higher than that in the $\langle 110\rangle$-one, while v_{inj} in those devices remains comparable (Fig. 7). However, I_{sd} efficiently increases when the v_{inj} becomes higher in “strained channel” as mentioned in the previous section. Thereby, as seen in Fig. 7, larger I_{sd} for “strained” $\langle 110\rangle$-channel is supported by the v_{inj} increase with compressive stress over 0.5 GPa, in contrast to the $\langle 100\rangle$ case which has even higher v_{max} under any stress condition but not for the v_{inj}.

Surface Orientation Dependence: Figure 8 shows calculated I_{sd} as a function of applied uniaxial stress for the devices with various surface orientation and channel direction. I_{sd} increases in the order of (110)-, (111)-, and (001)-surface for the same applied stress value, while the stress-induced–I_{sd}-change depends not much on the surface orientation but highly on the channel direction. Hence, the maximum I_{sd} was found to be in the $\langle \bar{1}10\rangle$-channel direction devices on the (110)-surface with compressive uniaxial stress applied.

4 Conclusion

Full-band Monte Carlo Ge-pMOSFET simulations presented here help us to understand strain-induced drain-current enhancement mechanism under the various channel/strain conditions. These comparative analyses with Si-MOSFETs enable us to optimize Ge-MOSFET structure more practical level for the future device design and performance scaling.

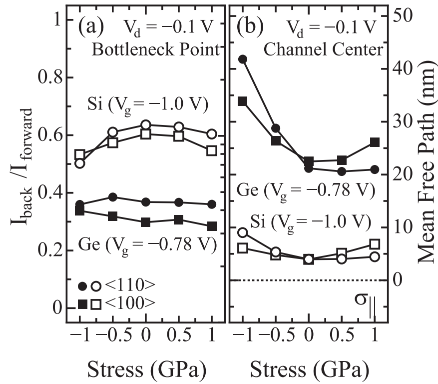

Figure 5: (a) Stress dependence of the backscattering indicator, $I_{\text{back}}/I_{\text{forward}}$, at the bottleneck point. (b) Mean-free-path (λ_{mfp}) at the center of the channel.

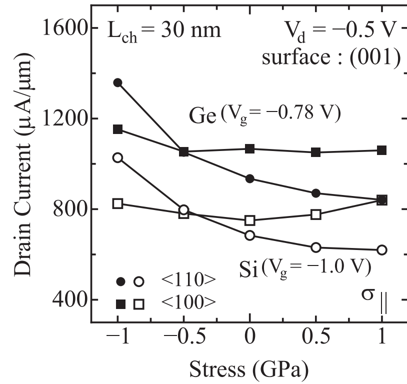

Figure 6: I_{sd} at $V_{\text{d}} = -0.5\,\text{V}$ as a function of the applied stress. I_{sd} for $\langle 110 \rangle$ overcomes that for $\langle 100 \rangle$ with compressive stress over 0.5 GPa.

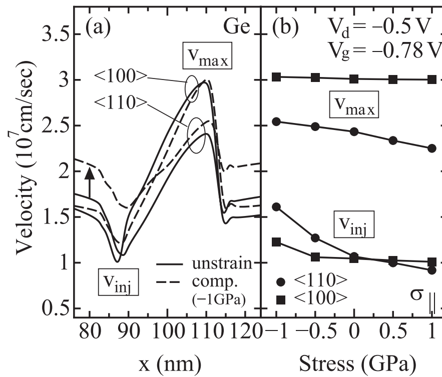

Figure 7: (a) Average velocity profile for the positive velocity carriers at $V_{\text{d}} = -0.5\,\text{V}$. (b) The maximum carrier velocity, v_{max}, and the injection velocity, v_{inj}, as a function of the applied uniaxial stress.

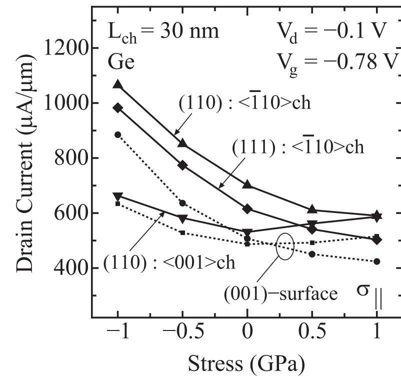

Figure 8: I_{sd} comparison for different surface/channel orientations at $V_{\text{d}} = -0.1\,\text{V}$. Dotted lines are I_{sd} for (001)-surface same as in Fig. 3.

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