A 5 GHz Direct Digital Synthesizer MMIC with Direct Modulation and Spur Randomization

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***Abstract*— This paper presents a low power, ultra high speed and high resolution SiGe DDS MMIC with 24-bit phase and 10-bit amplitude resolution. The DDS MMIC has the capabilities of direct frequency and phase modulations with 24 bit and 12 bit resolution, respectively. It is the first reported mm-wave DDS with direct digital frequency and phase modulation capabilities. Utilizing a 13-bit built-in ultra high speed pseudorandom binary sequence (PRBS) generator, the DDS MMIC can perform least significant bit (LSB) dithering for spur randomization. With more than twenty thousand transistors, the DDS MMIC includes a 24-bit ripple carry accumulator for phase accumulation, a 12-bit ripple carry adder for phase modulation, an LSB dithering block for spur randomization and a 10-bit segmented sine-weighted DAC for phase to amplitude mapping and digital to analog conversion. The DDS core occupies 3.0×2.5 mm^2 and consumes 4.7 W power under a single 3.3 V power supply. The Nyquist band SFDR is measured as 38 dBc with 469.360351 MHz output under 5.0 GHz maximum clock (FCW = 0x180800). With 1.246258914 GHz output frequency (FCW = 0x3FCFE7), the narrow band SFDR is measured as 82 dBc. The DDS MMIC is packaged and tested in LCC-68 cavity.**

***Index Terms*— digital-to-analog converter (DAC), direct digital synthesizer (DDS), direct digital frequency synthesizer (DDFS), sine-weighted digital-to-analog converter, Rom-less DDS, frequency modulation (FM), phase modulation (PM)**

I. Introduction

The high speed direct digital synthesizer (DDS) is a key component for the next generation radar and communication systems. Chirp modulation is widely used in radars to achieve high range resolution, while pulsed phase modulation (PM) can provide anti-jamming capability. The requirement of low power consumption, high output frequency, fine frequency resolution, fast channel switching and versatile modulation capability is difficult to implemented by the conventional PLL-based frequency synthesizers due to internal loop delay, low resolution, modulation problems and the limited tuning range of the voltage controlled oscillator (VCO). The increasing availability of ultra high speed SiGe process allows a DDS to operate at mm-wave frequency. However, none of the mm-wave DDS developed so far provides the desired modulation capability [1]–[3]. To achieve very high speed, all the existing DDS MMICs used pipeline accumulators that can work only with a constant input frequency control word (FCW), and thus no frequency modulation (FM) can be done [1]–[5]. To implement direct frequency or phase modulation, carry look ahead (CLA) or ripple carry adder (RCA) architectures have to be used with penalty of reduced speed. At low or medium speed, the CLA speeds up the adder operation by using additional logic for carry calculation. However, for high speed implementation with fast technology (e.g.,< 0.13 μm), adder delay is mainly dominated by the wire delays. Compared to a CLA adder, the RCA has a simple ripple architecture, which can be laid out in cascaded format one bit after another, leading to very compact layout with short wire interconnection between stages. After many simulations and experiments, we chose RCA architecture for the 5.0 GHz, 24-bit accumulator and 12-bit modulator implementation. This DDS MMIC represents the first mm-wave DDS with direct frequency and phase modulation capabilities.

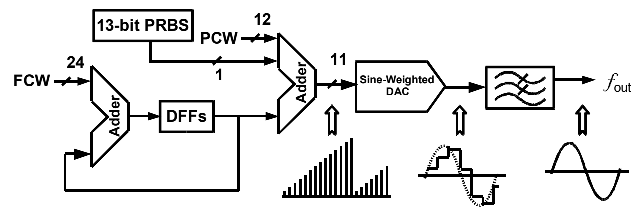

Fig. 1. Block diagram of 24-bit ROM-less DDS

II. Circuit Implementation

This DDS adopts a ROM-less architecture which combines both the sine/cosine mapping and digital-to-analog conversion together in a sine-weighted DAC. The block diagram of the 24-bit 5.0 GHz ROM-less DDS is shown in Fig.1. The major parts of the ROM-less DDS are a 24-bit phase accumulator, a 12-bit full adder, a 10-bit sine-weighted DAC and a 5.0 GHz pseudorandom binary sequence (PRBS) generator for spur randomization through the LSB phase control word (PCW) dithering. The 24-bit phase accumulator output is truncated to 12 bits and modulated with the 12-bit PCW. After phase modulation, the output is truncated again, and the highest 11 bits are fed into the sine-weighted DAC [5]. The sine-weighted DAC maps the 11 bit linear phase word to the digital amplitude and generates the analog waveform.

A. 24-bit Ripple Carry Adder/Accumulator

Because a pipeline accumulator can only handle a fixed FCW, RCA or CLA adders must be used to implement the direct modulation. In this design, a 24-bit RCA is used to implement 24-bit accumulator. The 24-bit RCA is composed of 24 1-bit full adders carefully layed out in a compact manner. The output of the carry out logic stays at the top CML level,

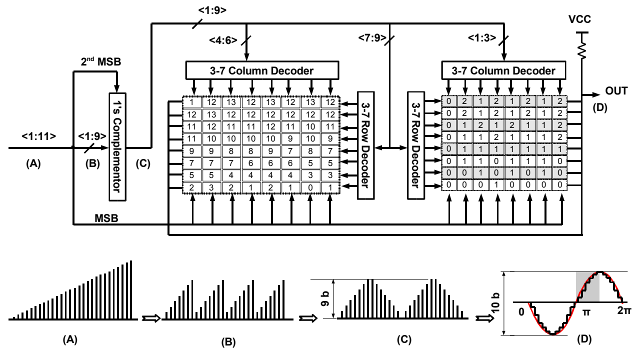

Fig. 2. Block diagram of 10-bit segmented sine-weighted DAC

and no level shifter is needed to convert the signal level for the critical path. Therefore the longest delay from input to output of the 24-bit RCA is 24 carry-out CML delays. The simulated 1-bit carry out delay in the 0.13 μm SiGe process is about 2.7 ps. Thus, the total delay for the 24-bit cascaded logic is about 64.8 ps, and the 5.0 GHz operating frequency can be achieved even with some wire delays. Although a 24-bit CLA adder needs only 14 level CMLs, level shifters and long wires must be inserted between the logic. For a 0.13 μm SiGe process, simulations and experiments show that long wires contribute much more delays than the logic gates, and the CLA adder cannot run as fast as the RCA for a 24-bit adder due to the delay needed for CLA logic. Another benefit of the RCA is that wire delay can be minimized since the carry in can be directly connected to the carry out of the previous bit, leading to a compact layout in a cascaded format. For direct phase modulation (PM), another 12-bit RCA was implemented.

B. 10-bit Segmented Sine-weighted DAC

The structure of the sine-weighted DAC is shown in Fig.2. The total phase word going to the sine-weighted DAC is 11 bits. The two most significant bits (MSB) are used to determine the quadrants of the sine wave. The MSB output of the phase word is used to provide the proper mirroring of the sine waveform about the π phase point. The 2nd MSB is used to invert the remaining 9 bits for the 2nd and 4th quadrants of the sine wave by a 1's complementor, and the outputs of the complementor are applied to a 9-bit sine-weighted DAC core to form a quarter of the sine waveform. Because of the π phase point mirroring, the total amplitude resolution of the sine-weighted DAC is 10 bit.

To reduce the complexity of the sine-weighted DAC, segmentation has been employed [5]. The 9-bit sine-weighted DAC core is divided into a 6-bit thermometer decoded coarse sine-weighted DAC and eight 3-bit thermometer decoded fine sine-weighted DACs. The first 6 bits of the complementor outputs control the coarse DAC, and the highest 3 bits also address the selection of the fine DACs. The lowest 3 bits of the complementor outputs determine the output value of each fine DAC. The bit division between 6-bit coarse DAC and 3-bit fine DACs is based on the trade-off of static and dynamic accuracies, chip area and power consumption. As shown in Fig.2, the left current source array is for the coarse DAC. The coarse DAC current source array provides 512 unit current sources. The right current source array is for the fine DACs. Each row of the fine DAC current source array forms the current sources of one fine DAC. Every fine DAC has about 8 unit current sources used to interpolate the coarse DAC. The unit current of both coarse and fine DACs is set at 26 μA. The largest current in the current source is 338 μA, which is composed of 13 unit current sources. For layout, considering the current source matching, each current source is split into four identical current sources which carry a quarter of the whole current. To further improve their matching, all the current source transistors, including coarse DAC and fine DACs, are randomly distributed in the whole current source matrix.

C. 13-bit 5.0 GHz Pseudorandom Binary Sequence Generator

In the process of discrete phase accumulation and phase truncation, spurs will be introduced in the DDS output spectrum. To reduce spurs, frequency or phase dithering offers a simple means to randomize the spur energy. Phase dithering can be accomplished by adding a small random number to the phase value at each clock cycle with a small penalty of elevated noise floor and increased phase noise. This process adds a constant phase to the accumulator output that will not affect the DDS output frequency. While there is a phase error at any instantaneous moment, the average phase value is correct, leading to correct output waveform with spur energy randomized over the Nyquist band. As shown in Fig.1, the 1-bit random number generated by the 5.0 GHz PRBS is added to the output of the accumulator through the carry in of the first bit of the 12-bit PM RCA. Fig.3(A) shows the architecture of the 5.0 GHz PRBS. It is implemented by a 13-bit 5.0 GHz Fibonacci linear feedback shift register (LFSR). Simulation results of the LFSR output waveform is shown in Fig.3(B). The output bit stream pattern will not repeat until $2^{13} - 1 = 8191$ cycles. With high speed CML differential flip-flops (DFF), the LFSR can work above 5.0 GHz.

III. Experiment Results

Figs.4-8 illustrate the measured DDS output spectra and waveforms for different output and clock frequencies. All measurements were done using LCC-68 packaged parts without calibrating the losses of the cables and PCB tracks. Fig.4 represents a 469.360351 MHz DDS output with a 5.0 GHz clock input with FCW = 0x180800. The measured output power is approximately -2.12 dBm and the measured SFDR is approximately 38 dBc. Since FCW = 0x180800, the output frequency is given by

$$\frac{FCW}{2^N} \times f_{clk} = \frac{\text{0x180800}}{2^{24}} \times 5.0\ GHz = 469.360351\ MHz$$

Narrow band dynamic specifications and close-in spectrum purity are critical for radar and communication systems. Fig.5 gives the plot of the measured SFDR versus the output

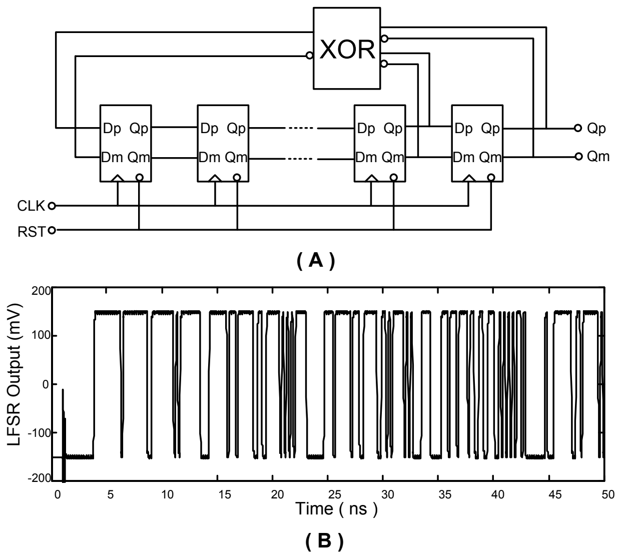

Fig. 3. Pseudorandom binary sequence generator and simulated output (A) 13-bit 5.0 GHz Fibonacci linear feedback shift register; (B) simulated result with 5.0 GHz clock.

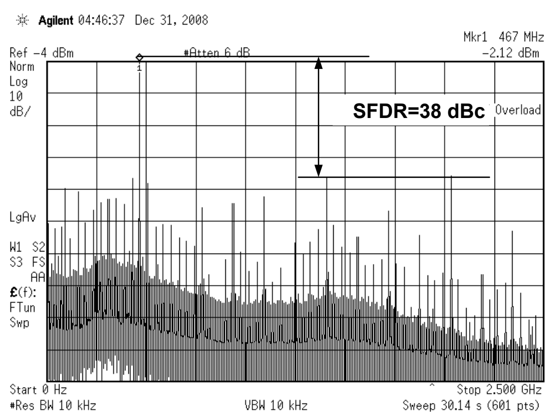

Fig. 4. Measured DDS output with 469.360351 MHz output and the maximum 5.0 GHz clock (FCW = 0x180800), showing 38 dBc Nyquist band SFDR.

frequency under a 5.0 GHz clock frequency within a 50 MHz bandwidth. It demonstrates about 45 dBc worst-case SFDR. In addition, the DDS have many sweet spots, in which its output spectrum purity and its dynamic performance are much better than other frequency bands. Fig.6 gives an example of 1.246258914 GHz output frequency (FCW = 0x3FCFE7) under 5.0 GHz clock frequency, the narrow band SFDR is measured as 82dBc.

Fig.7 demonstrates the operation of the DDS with a chirp modulation output. With a 300 MHz clock input, a 24-bit 300 MHz ramp from 0x000000 to 0x00AD9C is fed to the FCW input. The output sweeps from 18 Hz to 397.367947 kHz. In this DDS, CMOS logic was used to provide the modulation data inputs. The chirp modulation speed is limited by the speed of the data source that was provided by an Agilent pattern generator through the PCB board. A maximum of 2.5 GHz

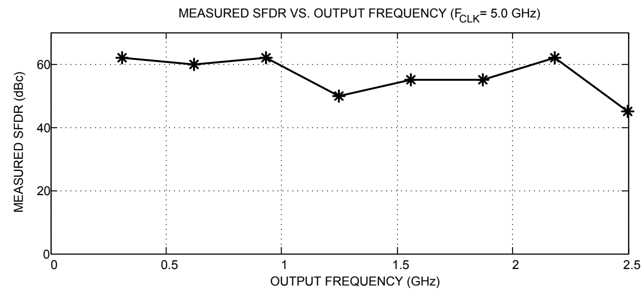

Fig. 5. Measured narrow band SFDR versus output frequency with 5.0 GHz clock frequency.

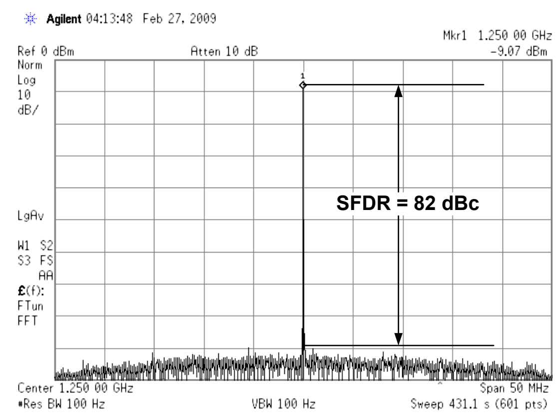

Fig. 6. Measured DDS output with 1.246258914 GHz output and the maximum 5.0 GHz clock (FCW = 0x180800), showing 82 dBc narrow band SFDR.

chirp modulation can be reached if the modulation ramp were generated inside the DDS chip. Fig.8 shows the measured DDS output with FCW = 7, phase modulated by a step of ΔPCW = 0x800 causing a 180° phase shift. The output frequency is 1.251 kHz with a 3.0 GHz clock.

Table I compares mm-wave DDS MMIC performances. Compared to the InP DDS MMICs, this SiGe DDS greatly improves the amplitude resolution and power efficiency. Compared to the SiGe DDS MMICs, this DDS is the first mm-wave DDS that provides 24-bit frequency and 12-bit phase modulations. Some commercial DDS components have the FM and PM capabilities, but they operate less than 1.0 GHz clock frequency. This DDS consumes 4.7 W power under a single 3.3 V power supply. The die photo of the SiGe DDS MMIC is shown in Fig.9. This DDS design is quite compact with an active area of 3.0×2.5 mm^2 and a total die area of 3.7×3.0 mm^2

IV. Conclusion

This paper presented a 24-bit 5.0 GHz SiGe DDS MMIC design with 24-bit frequency and 12-bit phase modulations, implemented in a 0.13 μm SiGe BiCMOS technology with f_T/f_{max} of 200/250 GHz. The DDS achieves a maximum clock frequency of 5.0 GHz. To improve the output spectral purity, a 13-bit 5.0 GHz built in pseudorandom binary

TABLE I
MM-WAVE DDS MMIC PERFORMANCE COMPARISION

Technology f_T/f_{max} [GHz]	InP 137/267 [1]	InP 300/300 [2]	InP 300/300 [3]	SiGe 100/120 [4]	SiGe 200/250 [5]	SiGe 200/250 [this work]
Phase resolution [bit]	8	8	8	9	11	24
Amplitude resolution [bit]	7	7	5	8	10	10
Frequency modulation [bit]	None	None	None	None	None	24
Phase modulation [bit]	None	None	None	None	None	12
Spur randomization	None	None	None	None	None	1-bit
Max clock [GHz]	9.2	13	32	9.6	8.6	5.0
SFDR [dBc]	30	26.67	21.56	30	40	45 (narrow)
Power consumption [W]	15	5.42	9.45	1.9	4.8	4.7
Die area [mm^2]	8.0 × 5.0	2.7 × 1.45	2.7 × 1.45	3.0 × 3.0	4.0 × 3.5	3.7 × 3.0

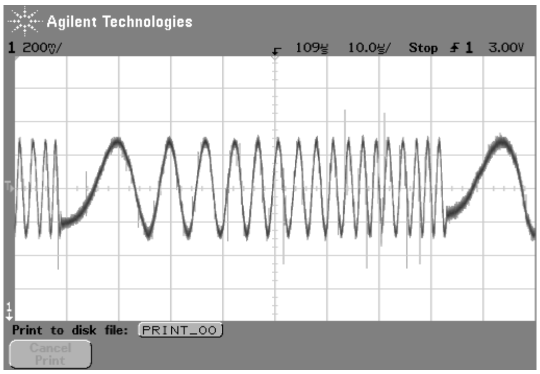

Fig. 7. Measured DDS chirp modulation output with FCW sweeps from 1 to 0x005AD9C and 300 MHz clock.

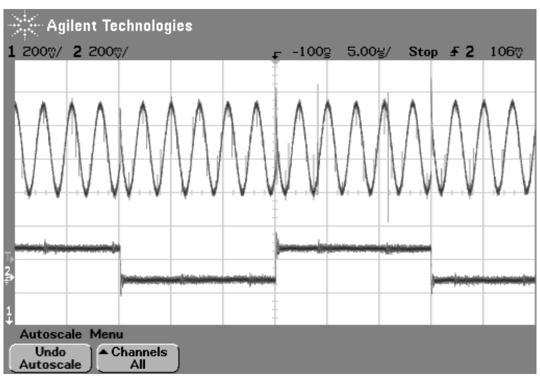

Fig. 8. Measured DDS output with FCW = 7 phase modulated by a phase step of ΔPCW = 0x800 causing a 180° phase shift. The output frequency is 1.251 kHz with a 3.0 GHz clock.

sequence (PRBS) generator is utilized, which performs least-significant bit (LSB) dithering for spur randomization. The measured worst case SFDR is 45 dBc under a 5.0 GHz clock frequency and within a 50 MHz bandwidth. The best Nyquist band SFDR is 38dBc with 469.360351 MHz output under a 5.0 GHz clock frequency. The power consumption of the MMIC including added modulation blocks is 4.7 W under a single 3.3 V power supply. This DDS MMIC is the first mm-wave DDS reported so far that has direct digital frequency and phase modulation capabilities.

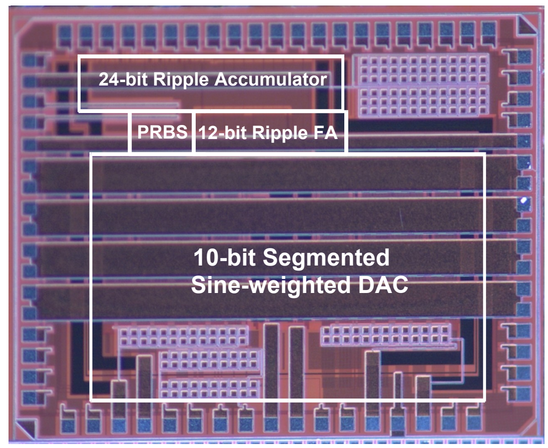

Fig. 9. Die photo of the 24-bit ROM-less DDS.

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