RELIABILITY CONSIDERATIONS FOR USING PLASTIC-ENCAPSULATED MICROCIRCUITS IN MILITARY APPLICATIONS

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ABSTRACT

The quality and reliability of plastic-encapsulated microcircuits (PEMs) manufactured today are closely equivalent, and in some ways superior, to their hermetic counterparts. The key to reliable use of PEMs in military applications is gained by matching the capabilities of PEMs to the application environment. The intent of this paper is to address the guidelines for achieving these ends by summarizing the strengths and limitations of PEMs relative to hermetic packages, discussing the associated failure mechanisms and reliability data, and outlining the best practices for both the production of PEMs and their use in the system application.

INTRODUCTION

The debate concerning the merits of using plastic-encapsulated microcircuits (PEMs) in place of hermetically sealed microcircuits (HSMs) in defense systems has been going on for more than a decade. For the past two years, the shrinking defense budget has increased the pressure to reduce program costs, thereby increasing the focus on the economic benefits of using commercial PEMs. Over the past decade PEM technology, manufacturing, and quality have advanced to the point where PEMs will yield reliability levels equivalent (and in some ways superior) to their hermetic counterparts in many applications. The military should be able to share in the benefits of PEMs, such as potential lower cost, greater product variety, smaller size, lighter weight, and mechanical ruggedness.

PEMs will provide the desired reliability in military applications if the application is correctly understood in relation to the strengths and limitations of PEMs, and the industry's best practices are employed by both the supplier and user. The intent of this paper is to address the means for achieving these ends. It is to be acknowledged that the quantitative bounding of all of the variables affecting a given application, enabling a definitive envelope for total risk elimination, does not exist. The material presented is based on available data, best collective engineering knowledge, and long experience as a major supplier of both commercial PEMs and military HSMs.

ADVANTAGES AND LIMITATIONS OF PEMs

Lower cost is normally the chief advantage cited for the use of PEMs over HSMs, especially as the number of inputs/outputs increases. However, this cost savings is only realized if the product is manufactured in a high volume commercial/industrial flow, and will diminish rapidly if additional tests and screens are added, as is typical of military HSMs. A common error in cost analysis is to project military PEM cost savings based on, for example, multimillion automotive volumes. PEMs are manufactured at 20X the volume of HSMs. A benefit to this is that these high volumes are accomplished through automation (as opposed to the more hand-oriented manufacturing of HSMs), which greatly reduces handling damage and process variability. PEMs, having a solid molded construction, are mechanically more rugged and weigh substantially less than HSMs. PEMs employing surface mount technology (SMT) offer a significant advantage over HSMs in terms of reduced size and weight. SMT is the predominant choice for most system applications today. *Therefore, more than a cost benefit can be realized with the careful selection of PEMs.* The most often cited concern about PEMs is their non-hermetic nature and permeability to moisture. Although this will be covered in more detail in a later section, it is stated here that major advancements in PEM technology have been made over the past decade, such that moisture induced failure mechanisms are not a major issue in most applications today. A composite listing of the advantages and limitations of PEMs relative to HSMs are presented below.

Advantages of PEMs Relative to HSMs:

- Potential lower cost
- Continuous product improvement programs
- Greater product variety
- Mechanically more rugged
- Lighter weight
- Available in smaller/thinner packages (SMT)
- TCE more closely matches that of most PCBs
- More automated assembly methods
- Higher volume and more cost effective production
- Qualification requirements generally more stringent than Mil-Std-883
- Reliability monitoring generally more frequent than Mil-Std-883
- More suppliers resulting in greater competition
- Ongoing demands for higher quality and reliability levels by commercial users

Limitations of PEMs Relative to HSMs:

- Non-hermetic package
- More limited temperature range
- Higher thermal resistance
- More rigorous controls needed for PCB assembly
- More sensitive to thermomechanical stresses
- Absorbed moisture in SMT packages during PCB assembly must be considered
- Not compatible with short production runs or non-standard processing
- Not compatible with inflexible baselining

FAILURE MECHANISMS OF PEMs AND HSMs

Appendix Table A1 lists the major package related failure mechanisms identified for both plastic and hermetic ICs. These mechanisms are sourced from both field return and reliability test data. The table shows that there are as many failure mechanisms for HSMs as there are for PEMs. Some mechanisms are common to both while others are unique to each package type. An important observation is that hermetic packages are more susceptible to mechanical stresses, whereas plastic packages are virtually immune to such stresses. Therefore, centrifuge, vibration, and impact shock are rarely, if ever, specified in the qualification of PEMs. However, there are three mechanisms unique to plastic packages, which warrant further discussion: moisture ingress, SMD package cracking, and thin film metal deformation/cracked passivation.

Moisture Ingress:

The ingress of moisture and contaminants, primarily through the plastic-to-lead frame interfaces of PEMs, can cause electrolytic corrosion of the aluminum interconnect metallization or parametric degradation. The rate of corrosion is a function of the bias voltage, presence of moisture, chip temperature, and conductivity of the penetrating electrolyte [1-3]. Probably the most prevalent and potent ionic contaminant associated with corrosion is chloride [1-7]. Therefore, precautions need to be taken to minimize or eliminate sources of chloride and other halides during the manufacture of PEMs, as well as during their assembly onto printed circuit boards (PCBs). Moisture in the absence of a reactive contaminant will not cause corrosion [8]. This is borne out by the multitude of accelerated humidity test data generated on PEMs. These test methods act to saturate the package with moisture in a relatively short period of time and include Temperature-Humidity-Bias (THB), HAST (Highly Accelerated Stress Test), and Autoclave or Pressure Cooker. The likelihood of this mechanism occurring in field use today is minimal based on advances in cleaner processing, passivation integrity, mold compound purity and adhesion, and leadframe construction. Also considered an important factor is the education of the user relative to the elimination of halides and other highly ionic materials during PCB assembly.

SMD Package Cracking "Popcorn Effect":

Cracking of certain Surface Mount Device (SMD) packages can occur during board assembly solder reflow operations (i.e., vapor phase, IR, and wave solder), due to stresses created from the sudden vaporization of absorbed moisture in the package [9, 10]. Such cracking creates a path for the possible ingress of moisture and contaminants, which can impact long term reliability. The internal shear stresses encountered can also affect bond wire integrity, particularly at the corners of the die, where the stress is greatest. This phenomenon is a function of the solder process temperature excursion, package moisture content, package dimensions, and mold compound adhesion. The effects have been observed mostly on large, high pin count packages, for which the current prevention is a dehydration bake, followed by shipment in dry-pack containers. Work is ongoing in the industry relative to the development of molding compounds which provide more resistance to this mechanism.

Thin Film Metal Deformation/Cracked Passivation:

Under temperature cycle conditions, thermomechanical shear stresses are set up between the molding compound and the die surface passivation/metallization, due to the differences in thermal coefficient of expansion (TCE) of the materials. The stress is negligible at the center of the die and increases exponentially from the center to the outer corners and edges [11,12]. Therefore, larger die experience greater stress in these areas than smaller die. Also the stress exerted on the passivation increases in relation to the increase in width and expansion of the underlying metallization lines [13,14]. Under severe temperature cycle extremes, the mold compound can exert enough stress on the die surface to fracture the surface passivation, after which the force is transmitted to the underlying metallization, causing it to deform or shear. Also, in multilevel metal systems the interlevel metal dielectric film can crack, causing a short between metal layers. Solutions include improved metal layout rules to reduce stress on the passivation at the corners and edges of the die, more planarized die surfaces to minimize the scrubbing action of the mold compound, die coatings in ultra sensitive devices, and low stress mold compounds. Reduced temperature cycle ranges may be necessary in some cases.

COMPARISON OF PLASTIC AND HERMETIC RELIABILITY DATA

Industry data comparing hermetic and plastic microcircuits on standard reliability tests have generally shown PEMs to be equivalent to hermetic parts [15,16]. This is supported with regard to reliability data generated on commercial, non-burned-in devices for the following process technologies: CMOS Metal Gate (CD4000 Series), CMOS Silicon Gate (CD74HC/HCT Series), and Bipolar ICs. These technologies are assembled in 8 to 20 lead Dual-in-Line and Small Outline packages, incorporate mostly single level metal on approximately 60-150 mil^2 die, and were chosen as vehicles for reliability comparison because they have a substantial amount of data on many identical device types in both hermetic (CERDIP) and plastic (PDIP and SO) over the same time frame (Jan. 1987 - Jul. 1994). The data by package type for the combined technologies are summarized in Tables 1 and 2 and Figures 1 - 3. It is shown that plastic and hermetic parts are basically comparable on these microcircuit families, relative to the overall FIT (failures in time) rates and DPM (defects per million) values exhibited on the tests shared by both.

Accelerated moisture test results for PEMs on the same product families are shown in Table 3. The DPM values for these types of moisture stresses, especially with regard to aluminum corrosion, do not indicate a basic moisture related issue. For obvious reasons, hermetic parts are not routinely subjected to these tests. However, it has been reported that hermetic CERDIPs can develop serious problems on 85/85 THB due to leaching of lead ions from the sealing glass [17].

TABLE 1 - HTOL FAILURE RATES AT 55°C, 60% UCL

PACKAGE	SAMPLE	FITs
Hermetic (CERDIP)	117,991	7.9
Plastic (PDIP)	342,252	8.2
Plastic (SO)	27,103	1.0
Combines data (1/87-7/94) on CMOS and Bipolar ICs. Extrapolation to 55°C from HTOL stress temperatures (≥125°C) is based on activation energies for individual failure mechanisms. FITs = failures in 10^9 device hours.		

TABLE 2 - TEMPERATURE STRESS TESTING

TEST	PACKAGE	SAMPLE	DPM
Temp Cycle -65° to +150°C 1000 Cycles	CERDIP	10,643	380
	PDIP	27,417	440
	SO	12,234	0
Thermal Shock -65° to +150°C 1000 Cycles	CERDIP	11,369	350
	PDIP	36,229	200
	SO	12,650	0
High Temp Storage +150°C 1000 Hours	CERDIP	13,940	0
	PDIP	31,594	32
	SO	16,220	0
Combines data (1/87-7/94) on CMOS and Bipolar ICs. DPM = defects per million			

TABLE 3 - MOISTURE TESTING PLASTIC PACKAGE

TEST	PKG	SAMPLE	DPM	
			TOTAL	EMA
THB 85°C/85% RH V_{DD}=6-18V 1000 Hours	PDIP	33,266	900	100
	SO	4,718	0	0
HAST 145°C/85% RH V_{DD}=6-18V 20 Hours	PDIP	127,144	300	60
	SO	2,885	0	0
Autoclave 121°C/100% RH 15 PSIG 192 Hours	PDIP	54,149	400	60
	SO	16,624	200	200
Combines data (1/87-7/94) on CMOS and Bipolar ICs. DPM = defects per million, EMA = Electrolytic Metal Attack				

RELIABILITY TESTS COMMON TO PLASTIC AND HERMETIC
COMBINES DATA FROM JAN 1987 - JUL 1994
FOR CMOS AND BIPOLAR ICs
(VALUES SHOWN AT STRESS CONDITIONS)

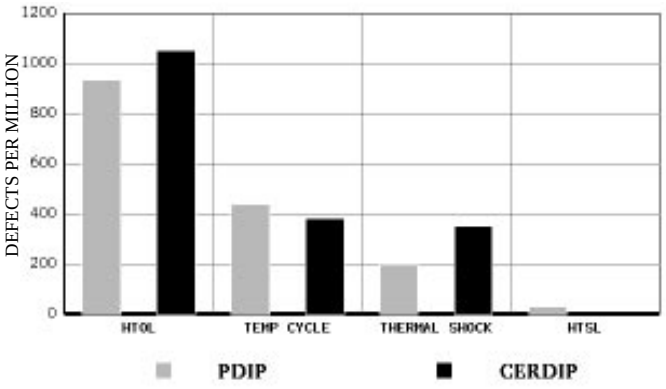

FIGURE 1

HTOL FAILURE MODES

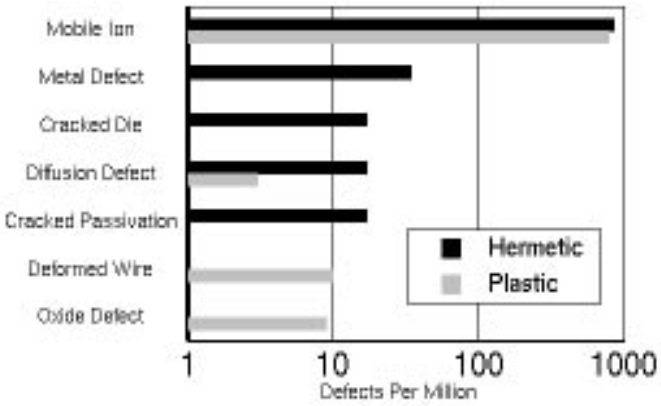

FIGURE 2

THERMAL STRESS TEST FAILURE MODES

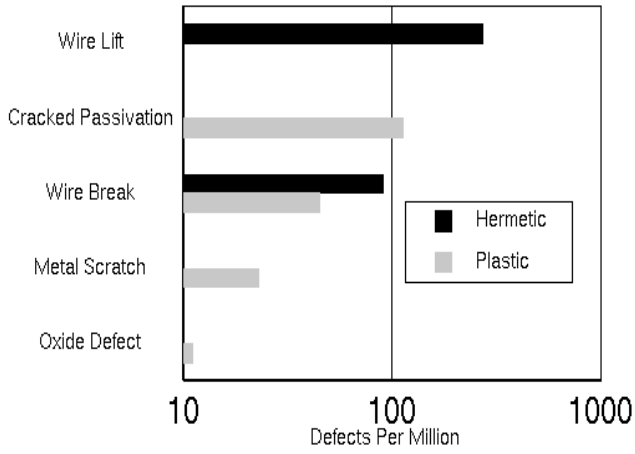

FIGURE 3

APPLICATIONS ENVELOPE FOR PEMs

Temperature:

Ambient operating temperatures specified for PEMs fall within the range of -55°C to +125°C, with some rated at these outer extremes. Individual devices may require more reduced ambient temperatures, depending on electrical characteristics, power dissipation, or specific package constraints. Other ranges typically specified are: -40°C to +125°C, -40°C to +85°C, and 0°C to +70°C. The maximum junction temperature for PEMs is +150°C. High temperature operating life (HTOL) performed on PEMs is usually conducted at ambients of 125°C to 150°C for a minimum of 1000 hours. In some cases, PEMs can be stressed at 175°C for shorter durations, as shown in Appendix Table A3. Operation of PEMs in dry ambients, within device ratings, generally yield results comparable to hermetic parts, as discussed previously.

The storage temperature range usually specified for PEMs is -65°C to +150°C. As mentioned previously, certain devices may require reduced storage temperatures, depending on temperature cycle limitations, or other package constraints. Routine 1000 hour storage data collected at +150°C on PEMs show no issues (Table 2). Temperatures exceeding the glass transition temperature (*Tg*) - typically 155°C to 165°C - of most mold compounds may result in leaching out impurities over time, particularly from the flame retardants, which may not otherwise occur. In addition, the TCE of the mold compound increases dramatically above the *Tg* threshold. Therefore, it may be inappropriate to extrapolate test results obtained above 150°C down through the *Tg* [18]. The primary failure mechanism associated with high temperature storage is Au-Al intermetallic degradation, which results in weakening the Au wire attachment to the Al bond pad. Reference [19] reports an activation energy of 0.8 eV for this mechanism in the presence of the mold compound, from which the Arrhenius acceleration factors can be derived. It has also been reported that this mechanism is unlikely to occur under 150°C, the upper storage limit of PEMs, as the Au-Al reaction threshold is above 150°C [17].

The acceleration factors for temperature cycle often used are based on the Coffin-Manson relationship [12], which equates the acceleration factor to the absolute change in temperature at stress divided by that at use, all raised to the power n. Although n can vary, a value of n=4 is generally used [20]. This relationship is mostly applicable to bond wire fatigue failure and may not hold for all temperature cycle failure mechanisms [12]. At Harris PEMs are qualified for 1000 cycles at either -65°C to +150°C (automotive) or -40°C to +125°C (industrial). Figure 4 plots the equivalent number of cycles for both these conditions at lower delta temperatures, using the model described.

Humidity:

Operation in humid environments relative to Al corrosion has been the main concern with PEMs over the years. PEM performance under accelerated biased humidity conditions has improved dramatically since the 1970's, as shown in reference [1] and figure 5. However, the perception of the 1970's still remains in many sectors, even though today's commercial use of PEMs registers in the billions per year, and field experience indicates that corrosion is rarely the cause of failure. Despite the significant improvement in moisture test and field performance, PEMs are still non-hermetic and are thus permeable to moisture. Therefore, they are susceptible to corrosion induced wear-out. Hermetic packages are not expected to exhibit this wear-out mechanism; i.e., if they are sealed in a dry ambient and the integrity of their seals are maintained over life. It is pointed out that a study comparing PDIPs and hermetic CERDIPs exposed to prolonged temperature cycle, followed by bias under 98%RH, showed a 4X higher failure rate for CERDIPs due to moisture induced corrosion [16]. The higher failure rate was attributed to the loss of hermeticity of the glass seals.

NUMBER OF TEMPERATURE CYCLES EQUIVALENT TO QUALIFICATION STRESS

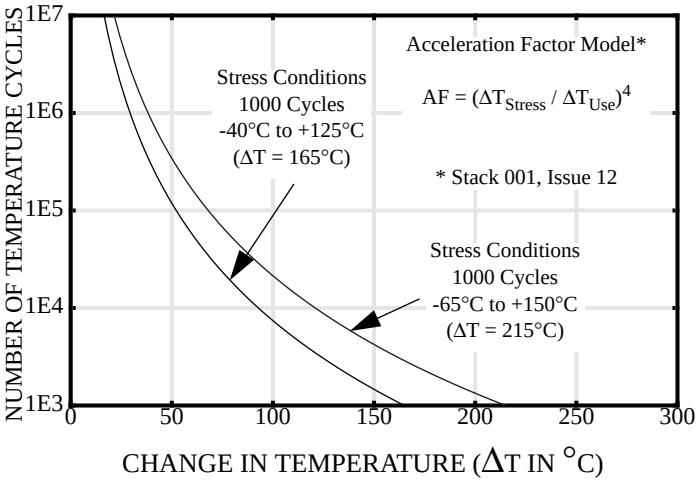

FIGURE 4

IMPROVEMENTS IN THB 85°C/85% RH PERFORMANCE IN PLASTIC-PACKAGED (PDIPs) CMOS LOGIC ICs

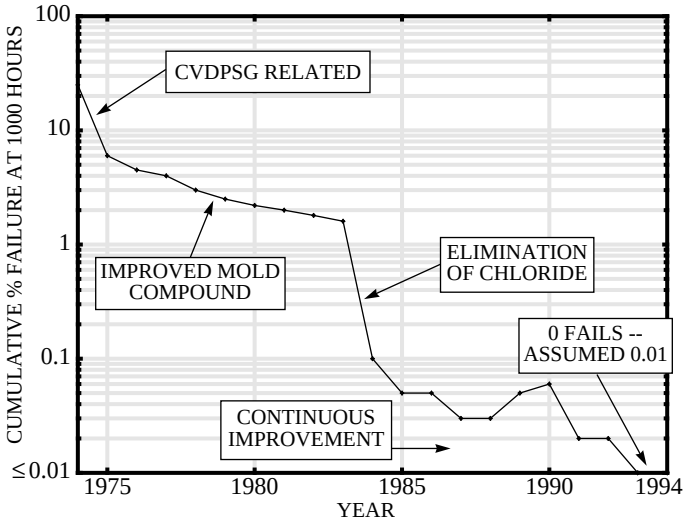

FIGURE 5

In the 1980's it became impractical to perform characterization studies of PEMs under standard 85/85 THB conditions, as their capability was in the thousands of hours (Table 4). Therefore, a more accelerated moisture test called HAST (Highly Accelerated Stress Test) was developed [21-23]. Typically, this test is conducted at 85% RH in the range of 110°C to 140°C (JEDEC 22-A110), although the humidity can be varied and higher temperatures have been evaluated. Wear-out characterization performed on PSG (phosphosilicate glass) passivated CMOS Logic ICs, using both HAST and 85/85 THB at 18 volts static bias is shown in Figure 6. This figure demonstrates the increase in median life gained through improvements in mold compound purity and lead frame construction, as well as from the reduction of Cl and other ionic contaminants incurred during the manufacturing process. The activation energy, empirically determined is in close agreement with Peck's 0.9eV [25]. Peck's model [24,25] was used to establish the acceleration factors relative to 85/85 in order to predict the set of curves shown in Figure 7. Extrapolation to 1% cumulative failure was based on an average log-normal $\sigma = 0.5$ and MTF of 18,000 hours. A voltage acceleration factor for the process [1] was used to extrapolate from 18 volts to 5 volts.

It is cautioned that not all PEMs yield equivalent results on moisture tests. Lifetimes may vary depending on the wafer process, package, and materials used. For example, HAST wear-out data generated at 145°C/85%RH/18V on silicon nitride/PSG sandwich passivation indicates a 10X longer lifetime than PSG (Figure 8). Thus, Figure 7 may provide a conservative estimate in many cases. Each supplier's data should be reviewed relative to moisture performance.

TABLE 4 - LONG TERM 85°C/85% RH TESTING (PDIP)

TEST	TECH.	HOURS	SAMPLE	FAILS
Storage	C	7,000	40	0
(No Bias)	A,B,C	10,000	120	0
	B	11,000	40	0
THB	A	3,000	180	0
(6V bias)	A	5,000	50	0
	A	7,000	40	0
	A	13,000	40	0
	A	14,000	40	0
	A	17,000	40	0
THB	B,C	5,000	40	0
(18V bias)	B,C	7,200	40	1@7.2k
	B,C	8,000	120	0
	B,C	9,000	160	1@6k
				1@9k
A=CMOS Silicon Gate (CD74HC/HCT), B=CMOS Metal Gate (CD4000), C=Bipolar, 14-20 lead PDIPs.				

Al CORROSION WEAR-OUT CHARACTERIZATION AT 85%RH DEMONSTRATES UP TO A 6X INCREASE IN MTF DUE TO IMPROVEMENTS IN MOLD COMPOUND, LEAD FRAME CONSTRUCTION, AND CLEANER PROCESSING

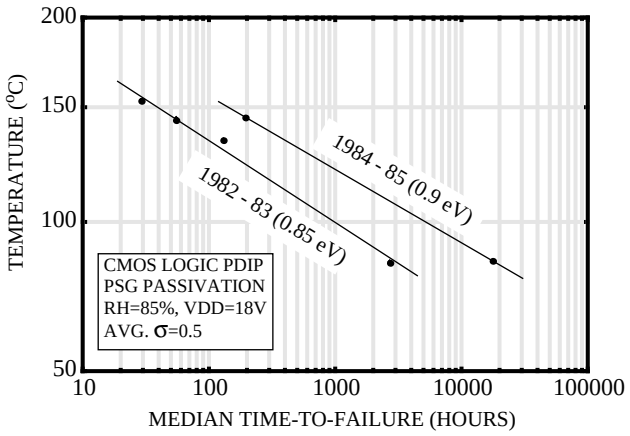

FIGURE 6

CMOS LOGIC PLASTIC DUAL-IN-LINE PACKAGE (PDIP) LIFE PREDICTION TO 1% FAILURE FOR ALUMINUM CORROSION AS A FUNCTION OF TEMPERATURE AND % RELATIVE HUMIDITY AT 5 VOLTS CONTINUOUS BIAS

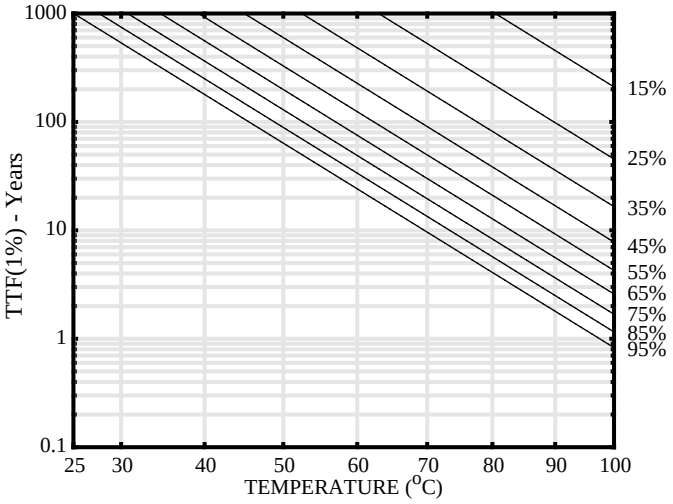

FIGURE 7

The characterization and prediction of long term humidity storage is made difficult by the fact that wear-out distributions can not easily be obtained over a practical period of time without the presence of a bias voltage. Available long term 85/85 storage and THB data are shown in Table 4. The unbiased saturated autoclave test (121°C, 100% RH, 15 psig) is routinely used to monitor PEMs. Although unbiased autoclave does not correlate well with 85/85 THB, it is a good accelerated test for monitoring lot-to-lot variability. PEMs generally do not have a problem passing the specified durations of 96 to 192 hours (Table 3). However, for

COMPARISON OF PLASMA ENHANCED NITRIDE (PEN) AND PHOSPHOSILICATE GLASS (PSG) PASSIVATION FOR Al CORROSION

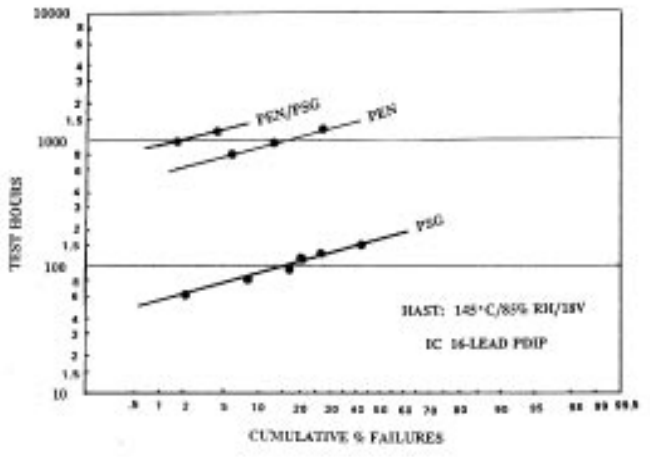

FIGURE 8

optimum results when storing parts prior to system use, it makes sense to keep the ambient humidity as low as possible. Recommended conditions are ≤55% RH at ≤30ºC, which is the upper limit of the typical PEM manufacturing environment.

A special case exists with the storage of certain Surface Mount Devices (SMDs) relative to "popcorn cracking", as described previously. Shipment in dry pack containers may be necessary on large, high pin count packages. Moisture sensitive devices are first subjected to a dehydration bake and then placed in a moisture resistant bag, along with a desiccant packet and moisture indicator card. The bag is then vacuum sealed. After opening the bag, the moisture indicator card should always be checked to ensure the seal was not impaired. The parts then should be board mounted within 48 hours, depending on ambient conditions, or stored in an environment which prevents the total absorbed moisture from exceeding 0.1% of the total package weight. Recently released industry standards, such as JEDEC A112 and A113 (moisture sensitivity classification and qualification preconditioning for SMDs), and the proposed JEP113 (Symbols and Labels for Moisture-Sensitive Devices) have established six categories of moisture sensitivity. These range from nonsensitive Level 1 packages (unlimited floor life at ≤30ºC/90%RH) to extremely moisture sensitive Level 6 (maximum floor life of 6 hours at conditions of ≤30ºC/60%RH)

Liquids, Gases, and Particles:

Environments which contain liquids, gases, and particles, as may apply in system assembly or use, should be guarded to obtain optimum use of PEMs. In the case of liquids used in processing, the concentration of halides and other anionic species and their residuals (Cl^-, F^-, Br, SO_4^{--}) in aqueous solutions should not exceed 50 ppm. Alkali ions, salts and residuals (Na^+, K^+, Li^+) in aqueous solutions should not exceed 10 ppm. Volatile gases, such as SO_2, NO_x, O_3, CO, etc., should be minimized, although, standards for plastic-encapsulated devices are not available. It must be pointed out that high humidity levels (>85%RH) greatly accelerate the activation of the deleterious effect of the presence of these volatiles. Also, the size and quantity of particles should be few enough and small enough so as not to collect between leads or bridge the lead spacing over the useful life of the PCB. Bias and humidity are accelerators which increase sensitivity to this mechanism. This applies to both PEMs and HSMs. Particle sensitivity becomes even more critical with fine pitch leads as found in SMDs. Best practices would ensure the elimination of conductive particles from the environment. Conformal coating of the PCB will also keep particles away from packages as well as provide extra protection against airborne contaminants and liquid moisture ingress.

Flammability:

Safe applications will use mold compounds that meet the following flammability ratings in conjunction with using adequate fusing and circuit breakers:

- ASTM D2863-91 oxygen index >28%
- UL 94 V1 Rating

Safest applications will use mold compounds that satisfy UL 94 V0 rating.

Radiation Hardness:

With regard to applications requiring radiation hardness, it is recommended that HSMs continue to be used, as insufficient data exists to merit the use of PEMs. However, preliminary data generated by Harris on silox passivated CMOS ICs in 16-lead PDIPs demonstrated no device degradation after an exposure level of 300k RADs. Additional work is needed to fully characterize plastic-packaged microcircuits.

In general, the use of HSMs should be continued in critical applications for which there is inadequate data to establish a comfortable margin of risk in the use of PEMs. Concurrent with this, industry assessments to stretch the PEM envelope relative to these applications should be ongoing.

BEST PRACTICES FOR DESIGNING IN QUALITY AND RELIABILITY

Over the years system manufacturers have continually placed requirements on suppliers of PEMs for demonstrating ever increasing high levels of quality and reliability, which in many ways exceed those imposed by the military (see Appendix Tables A2 and A3). Demands for AOQs (Average Outgoing Quality) of less than 20 ppm and failure rates of 10 FITs (Failure in Time) are not uncommon today, with these values expected to decrease an order of magnitude before the end of the decade. In order to meet these challenges, Total Quality Management (TQM) systems are employed by Harris throughout all phases of product development, manufacture, and service. Within the scope of TQM, new technologies are developed by the Technology (Process) Development System (TDS), which is overlapped by a system called Applying Concurrent Teams to the Product-to-

Market process (ACT-PTM). In brief, these systems are manifested in well defined, multidisciplinary project teams, which are given full responsibility for successful project execution from early product development to end customer service. This results in greater first pass success of new processes and products, reduced cycle time, enhanced quality and reliability, and continuous improvement. A full description of these systems is given in reference [26].

The principles for Building in Reliability (BIR) are used during the early stages of technology/product development to ensure wear-out and special cause mechanisms are eliminated from useful product life [27,28]. Figure 9 illustrates the paradigm shift made in the mid-1980's with respect to the BIR concept. The old paradigm (energy down stream) with Reliability involvement at the end of the development cycle led to qualification failures, recycle of design and three to four years to introduce a new technology. The BIR paradigm (energy up stream) with early Reliability involvement beginning at the concept facilitates the 'build-in' process, increases first pass success and has reduced cycle time by a factor of four. Two important benefits of BIR are reliability inputs into the design/layout groundrules and definition of reliability critical process node parameters. Appendix Table A4 gives a brief listing of some of the best practices employed.

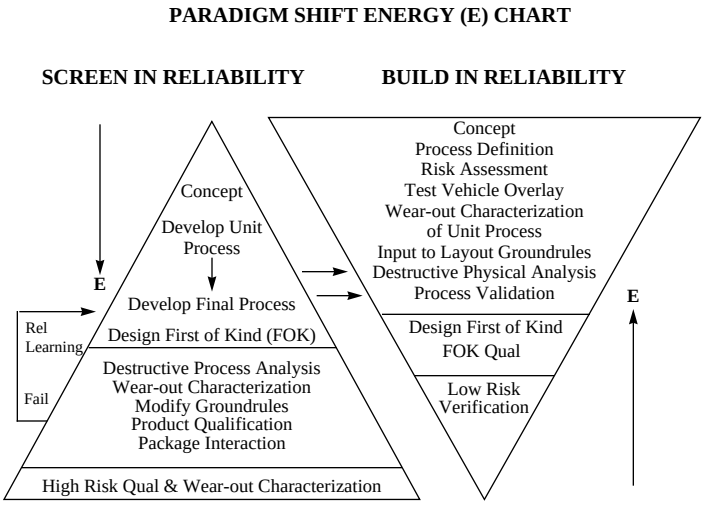

FIGURE 9

Verification of reliability is achieved through rigorous characterization/qualification testing at both the wafer and package level and then through the use of continuous production reliability monitoring (Appendix Table A3). SPC methods are employed throughout the manufacturing processes. Each manufacturing line (both wafer fab and package assembly) has a critical node list to assure quality and reliability are maintained and improved over time (examples are provided in Appendix Tables A5 and A6). These methodologies apply to the development of all product technologies, regardless of whether the end-use application is commercial, industrial, or military. Some of the tools/methods employed are listed below.

- Critical node list (wafer/assembly)
- SPC (Statistical Process Control)
- Statistical Design of Experiments
- TPM (Total Productive Maintenance)
- FMEA (Failure Mode & Effects Analysis)
- Reliability Characterization/Qualification
- Reliability Monitors
- Field Return Program
- 8-Discipline Problem Solving
- Self Audit
- Team Problem Solving
- Trend and Pareto Analysis
- Continuous Improvement Programs

BEST PRACTICES RECOMMENDED FOR PRODUCT HANDLING AND PROCESSING

The life expectancy of PEMs in an application is a strong function of the PEM manufacturing and the subsequent board/system handling and processing. These manufacturing steps set the stage for reliability of deployed systems. Appendix Table A7 provides a list of best practices recommended for PEM handling and processing that will help ensure reliable performance.

SUMMARY AND CONCLUSIONS

The thrust of this paper was to address the use of PEMs in military applications by reviewing their strengths and limitations relative to HSMs, comparing reliability data on the same microcircuit families manufactured in both package systems, describing the systematic approach for producing reliable PEMs, and outlining the conditions and best practices for achieving optimum use of PEMs in the system application. It was stated that within the reliable operating and storage envelope, PEMs are as reliable as HSMs, and therefore should be considered for the appropriate military applications. The key to successful use of PEMs is gained through matching the application conditions to the capability of PEMs. For some highly critical applications more characterization of PEM reliability is required to determine limitations and establish confidence, especially where radiation hardness and prolonged storage are requirements. However, PEMs have demonstrated acceptable reliability in a multitude of commercial/industrial applications for many years. Hence, there exists today a substantial amount of data and wealth of experience from which to support the use of PEMs by the military in similar applications. Finally, it is emphasized that procuring PEMs from a qualified supplier, one having extensive experience in both hermetic Military/Aerospace microcircuits and PEMs used in rugged environments, such as automotive, is as important as defining the envelope for reliable use.

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APPENDIX

TABLE A1 - PACKAGE RELATED FAILURE MECHANISMS IDENTIFIED WITH PLASTIC AND HERMETIC IC'S

DESCRIPTION	STRESS/ SOURCE	RESPONSE	ACCELERATING TEST	PLASTIC	HERMETIC
Cracked Die	Thermal	Electrical Short/Open	Temperature Cycle	X	X
	Mechanical	Electrical Short/Open	Impact Shock		X
Wire Breaks	Thermal	Electrical Open	Temperature Cycle	X	X
	Mechanical	Electrical Open	Vibration, Centrifuge		X
Wire Lifts	Thermal	Electrical Open	Temperature Cycle	X	X
	Mechanical	Electrical Open	Vibration, Centrifuge		X
Wire Lifts (intermetallic)	Thermal	Electrical Open	High Temperature Storage	X	X
Cracked Package Seals	Thermal	Loss of Hermeticity	Temperature Cycle		X
	Mechanical	Loss of Hermeticity	Impact Shock		X
Corroded Seals, external (Pin-to-Pin Shorts)	Moisture	Loss of Hermeticity	Humidity, Salt Atmosphere		X
Interface Delamination	Thermal	Reduced Moisture Resistance	Temperature Cycle	X	
Internal Water Vapor	Package Assembly	Al Corrosion	Low Temperature Bias Life		X
Moisture Ingress	Moisture	Al Corrosion	Temperature/Humidity/Bias Autoclave, HAST	X	
SMD Cracked Package (Popcorn Effect)	Thermal	Reduced Moisture Resistance/Elect. Opens	Humidity/Solder Shock Sequence	X	
Metal Deformation/ Cracked Passivation	Thermal	Electrical Shorts/Opens	Temperature Cycle	X	
Lifted Die	Thermal Mechanical	Electrical Shorts/Open Thermal Designation	Temperature Cycle Impact Shock, Centrifuge		X
Die Attach Voids	Package Assembly	Thermal Dissipation Low D/A Strength Cracked Die	Bias Life Temp Cycle, Centrifuge	X	X
Loose Die Attach, Sealing Materials, and Particles	Package Assembly	Electrical Shorts	Vibration/Shock PIND		X

APPENDIX

TABLE A2 - COMPARISON OF GENERAL INDUSTRY SAMPLING & QUALIFICATIONS FOR MILITARY HERMETIC VERSUS AUTOMOTIVE PLASTIC MICROCIRCUITS

DESCRIPTION OF TEST	MILITARY HERMETIC (Mil. Std. 883)			AUTOMOTIVE PLASTIC (Typical)		
	LTPD	#LOTS	DURATION	LTPD	#LOTS	DURATION
Burn-In 100%	(PDA = 5%)	All	168 Hours	(PDA = 0.5-2.0%*)	All	48-168 Hours
Operating Life Qualification	5	1	1k Hours	2 - 3	1 or 3	1k - 2k Hours
Biased Humidity Qualification	Not Specified	Not Specified	Not Specified	2 - 3	1 or 3	1k - 2k Hours
Temp Cycle Qualification	15	1	100 Cycles	1.5 - 3	1 or 3	1k Cycles
Mechanical Qualification	15	1	- - -	Not Specified	Not Specified	Not Specified
Group A Sampling	2	All	- - -	1	All	- - -

* Values are for when PDA is specified. Sample burn-in to LTPD of 2% typically performed when PDA not specified.
Note: This chart compares similar stress conditions with the exception of biased humidity and mechanical.

TABLE A3 - RELIABILITY MONITORS - COMPARISON OF MILITARY HERMETIC AND HARRIS PLASTIC

HERMETIC MILITARY (MIL-STD-883) QUALITY CONFORMANCE INSPECTION (QCI)			PLASTIC COMMERCIAL MATRIX MONITOR		
DESCRIPTION	SAMPLE/ ACC. NO.	FREQUENCY	DESCRIPTION	SAMPLE/ ACC. NO.	FREQUENCY
Group B			Matrix I		
Resistance to Solvents	3/0	Each Lot	HTOL (125˚C or 175˚C, 48 Hours)	45/0	2X/Month
Bond Strength	22/0	Each Lot	HAST (135˚C/85% R.H., 48 Hours)	45/0	2X/Month
Solderability(8 Hours Steam Age)	10/0	Each Lot	Autoclave (96 Hours)	45/0	2X/Month
			Thermal Shock (200 Cycles)	45/0	2X/Month
Group C			Matrix II		
HTOL (125˚C, 1k Hours)	45/0	1X/12 Months	HTOL (125˚C, 1k Hours)	45/0	1X/Month
			THB (85/85, 1k Hours)	45/0	1X/Month
			Autoclave (192 Hours)	45/0	1X/2 Months
			Storage Life (150˚C, 1k Hours)	45/0	1X/2 Months
			Temp Cycle (1k Cycles)	45/0	1X/2 Months
Group D			Matrix III		
1.Physical Dimensions	15/0	1X/6 Months	Solderability (8 Hrs. Steam Age)	22/0	2X/Month
2.Lead Integrity	15/0	1X/6 Months	Brand Adherence	15/0	1X/Month
3.Thermal Shock (15 Cycles)	15/0	1X/6 Months	Lead Integrity	15/0	1X/Month
Temp Cycle (100 Cycles)			Physical Dimensions	11/0	1X/Month
Moisture Resist (10 Cycles)			Flammability UL-94	5/0	1X/Quarter
4.Shock					
Vib. Var. Freq.	15/0	1X/6 Months			
Acceleration			SPC Monitored (Eqv. to Hermetic)		
5.Salt Atm. (24-240 HPS)			Bond Strength	SPC	1X/Shift
6.Internal Wafer Vapor	15/0	1X/6 Months	Die Shear	SPC - Z	1X/Oven/Cycle
7.Adhesion of Lead Finish	3/0	1X/6 Months		Chart	
8.Lid Torque	15/0	1X/6 Months	Solderability >4 Hours Steam Age	Recording	1X/Shift
	5/0	1X/6 Months	>8 Hours Steam Age	Recording	1X/Week

Note:Mil-Std-883 requires assembly locations to have an additional monitor program to Mil-Std-976 (i.e., Bond Strength/Die Shear, etc.) which has not been covered by this table.

APPENDIX

TABLE A4 - BEST INDUSTRY PRACTICES - DESIGN FOR RELIABILITY AND CONTINUOUS IMPROVEMENT

DIE RELATED	IMPACT ON RELIABILITY
• Electric (E) Field Plating	- Reduces mobile ion instability
• Particulate & Contaminant Control	- Lowers defects in oxides and ionic contamination
• Layout considerations for high stress areas.	- Reduces stress cracking of passivation at die corners.
• Denser passivation, sandwich layers of SiO_2/SiN_x	- Better integrity against fabrication defects. - Robust to thermomechanical stress. - Better moisture/ion barrier.
• Passivation overlap of die oxide edges.	- Provides moisture/ion barrier
• Advanced planarization for reduced stress.	- Reduced metal displacement and passivation damage.
• Wear-out failure mechanisms eliminated from useful life at the die level.	- Elimination from useful life the intrinsic wear-out failure mechanisms EM (Electromigration), TDDB (Time Dependant Dielectric Breakdown), Hot carrier injection, Corrosion, and Device Stability.
• Reliability critical process node list.	- SPC control of variables effecting quality and reliability
PACKAGE RELATED	**IMPACT ON RELIABILITY**
• Mold compounds: - Higher glass transition temperatures.	- Less thermomechanical stress at high temperatures - More robust to thermal cycling
- Low ionic (Low Halides, and Alkali) compounds	- Reduced corrosion and increased device stability
- Use of modified filler material.	- Reduced point stress damage on die surface.
- Low stress mold compounds for large die and complex geometries.	- Reduced passivation cracking and metal deformation
- Ion getters.	- Corrosion reduction and greater device stability.
- Reduced frame retardants	- High temperature stability and corrosion reduction
- Automated in-line mold machines	- Less wire sweep. - Less voids in plastic - Better control of molding process
• Die attach materials with low stress, low ionics.	- Less stress on die - Increased device stability
• Lead lock holes, moisture groves, locking bars on lead frame.	- Increased moisture resistance and corrosion reduction. - Increased mechanical integrity
• Optimum die to paddle spacing.	- Lower stress on die
• Automated assembly processes	- No human handling, less contamination, and less process variability
• SPC critical node list and process monitors.	- Variability reduction and Continuous Improvement.
EXPANDED MATERIALS CHARACTERIZATION	**IMPACT ON RELIABILITY**
• Acoustic Microscopy - CSAM - SLAM	- Non destructive analysis of Plastic products for voids, die cracks, and delamination isolation. DOX with CSAM yields Continuous Improvement.
• Thermal Characterization Methods: - Differential scanning calorimetry - Thermogravimetric analysis - Thermomechanical analysis	- Broader materials characterization and referencing enhances continuous improvement of raw materials.
• Moisture weight gain/loss measurements	- Determine sensitivity to delamination and popcorn cracking. - Material analysis - Determine dry pack requirements.
• Applications of dye penetrants	- Being further developed to enhance tracing moisture ingress on lead frame to Plastic interfaces.

TABLE A5 - ASIC WAFER FABRICATION, 6", CRITICAL NODE LIST EXAMPLE

MAJOR FLOW STEP	CRITICAL PARAMETER	TYPE OF CONTROL	CRITICAL NODE YES/NO
EPI Deposition	Sheet Resistance	XBAR-R	YES
	EPI Thickness	XBAR-R	YES
P-Diffusion	Oxide Thickness	XBAR-R	YES
Sink Deposition	Sheet Resistance	XBAR-R	YES
Nitride Dep & Etch	Post Etch Dimension	XBAR-R	YES
Local Oxidation	Oxide Thickness	XBAR-R	YES
BN Drive	Sheet Resistance	XBAR-R	YES
Gate Oxidation	Oxide Thickness	XBAR-R	YES
Poly Deposition	Poly Thickness	XBAR-R	YES
Poly Doping	Sheet Resistance	XBAR-R	YES
Poly Etch	Post Etch Dimension	Z-Chart	YES
DMOS Drive	Oxide Thickness	XBAR-R	YES
N+/P+ Ion Implant	Sheet Resistivity	XBAR-R	NO
Interlevel Dielectric	Oxide Thickness	XBAR-R	YES
First Metal Deposition	Deposition Rate	XBAR-R	YES
	Thickness	XBAR-R	YES
First Metal Etch	Post Etch Dimension	XBAR-R	YES
	Thickness	XBAR-R	YES
	Reflectivity	XBAR-R	YES
Intermetal Dielectric	Oxide Thickness	XBAR-R	YES
Sec. Metal Deposition	Deposition Rate	XBAR-R	YES
Second Metal Etch	Post Etch Dimension	Z-Chart	YES
Passivation Deposition	Passivation Thickness	XBAR-R	YES
In-Line Probe	Device Parameters	Test Site Sample	NO

Note: Other general or tool related critical controls such as Capacitance Voltage (CV) test for the cleanliness of furnaces and deposition tools are maintained in-line.

TABLE A6 - PLASTIC DIP ASSEMBLY CRITICAL NODE LIST EXAMPLE

MAJOR FLOW STEP	CRITICAL PARAMETER	TYPE OF CONTROL	CRITICAL NODE YES/NO
Wafer Mount			NO
Saw	Kerf width, DI	XBAR-R	YES
	Resistivity	Monitor	
Die Visual	Visual Quality	AQL	YES
QC Lot Acceptance	Visual Quality	AQL	NO
Die Attach	Visual Quality	NP-Chart	YES
Die Attach Cure	Oven Temp	XBAR-R	YES
	Die Shear	Z-Chart	
Wire Bond	Pull Strength	XBAR-R	YES
	Visual	NP-Chart	
	Temp	XBAR-R	
	Force	XBAR-R	
	Ball Shear	XBAR-R	
QC Lot Acceptance	Visual Quality	AQL	NO
Mold	Visual Quality	NP-Chart	YES
	X-Ray	AQL	
Chemical Deflash	Visual Quality	NP-Chart	YES
Mold Cure	Oven Temp	XBAR-R	YES
Trim/Form	Visual Quality	NP-Chart	YES
Solder DIP	Visual Quality	AQL	YES
	Solder Thickness	XBAR-R	
QA Lot Acceptance	Solderability	AQL	NO
Brand	Visual Quality	NP-Chart	YES
	Brand Perm	AQL	
QA Lot Acceptance To Test	Visual Quality	AQL	NO

APPENDIX

TABLE A7 - BEST PRACTICES RECOMMENDED FOR PEM HANDLING AND BOARD/SYSTEM PROCESSING

PROBLEM	PREVENTION
• Storage	
- Environmental vapors in ambient and moisture can be corrosive to the leads of packages and cause dendritic growth on insulating surfaces between leads.	- Control environmental ambient gases. Dry N_2 storage. - Eliminate Human handling of product.
- Storage environment if moist can lead to moisture uptake in plastic. With voids or delamination, accumulation of monolayers of moisture and contaminants can change pH or conductivity of moisture sufficiently to start galvanic corrosion of metallization.	- Dry N_2 purge storage, minimize storage time.
- Storage in moist environments may lead to “Popcorn Cracking” or delamination in certain surface mount device packages during solder reflow operations.	- Dry pack (sensitive package types) - Store surface mount devices at <30˚C and <55% R.H.
• Electrostatic Discharge (ESD) - applicable to hermetic and PEMs	
- Human handling without proper ESD prevention can lead to damaged products.	- Use monitored wrist straps at work station, with ionization if necessary. - Reduce sliding packages on insulated surfaces.
- Dropping parts out of tubes or in handlers onto a grounded surface can lead to triboelectric charge damage as well as non destructive oxide charging (surface leakage and reflected leakage).	- Reduce dropping distance or purge with ionization. - ESD gauge all handlers, pick and place machines, belt transports and transition points for charged surfaces. Improve grounding and charge dissipation
- Handlers that have ESD hot zones due to a lack of grounding or oxidized surface such as anodized surfaces, floating rails, etc., can cause ESD damage.	- Adjust coating and cleaning processes to minimize charging, i.e., use ionization, add CO_2 to DI water, etc. Low pressure applications.
- Conformal coating materials sprayed on PCB's can develop extreme ESD potential. Also sprayed DI water is an ESD source.	- Follow Mil-Handbook 263, - ESD Control Handbook Mil-Std 1686, JEDEC, Pub 108-A
• Handling to Prevent External Contamination	
- Human handling contaminants (body oils, salts, makeup, lotions) on the external surfaces of a package may diffuse through plastic with moisture, leading to ionic instability or corrosion.	- Use automated pick and place equipment. - If handled, use clean, ESD safe cots or gloves which have been shown not to transfer residuals or ionic contaminants to surfaces. - Thorough board cleaning.
• Processing Without Halides	
- Halides in flux or cleaning agents or residual halides on boards may diffuse through the plastic with moisture and lead to corrosion of bond pads, interconnect and lead frame.	- Use high purity electronic grade halide free flux and paste as well other high purity chemicals in board assembly or coat processes. - Thorough board cleaning.
• Alkali Metal Ion Free Processing	
- Alkali metal Ions (positive or cations) such as Na^+, Li^+, K^+ are mobile and can cause surface leakage and device drift.	- Use high purity electronic grade materials, gases, and liquids that certify as alkali free. - Control particle counts and analyze residue for alkali metals. Eliminate sources. - Eliminate human handling. - Thorough board cleaning.
• Surface Mount Device Solder Reflow	
- Thermal Shock due to temperature gradient and peak/temperature/time excursions in combination with sufficient absorbed moisture can lead to delamination of mold compound to die, paddle, and lead frame.	- Sensitive surface mount device packages not dry packed should be baked dry at 125˚C for 24 hours and used within 48 hours on board attach. - Use pre-heating in the solder attach process. - Monitor temperature profiles of the solder attach equipment - Pay special attention to the temp/time dwell of the peak solder temperature zone. - Standards - IPC, JEDEC A112
• Metallic Free Processing	
- Fine pitch packages, (<25 mils) are susceptible by their reduced lead pitch to residual solder and metallic fines which react with bias and moisture to cause leakage and shorts.	- Clean up residual solder paste and residual solder. - Eliminate sources of metallic fines in automated equipment. - Conformal coat PCB or selected surface mount devices. - Proper board packaging.