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Wafer bonding in silicon electronics

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Semiconductor wafer bonding offers a new degree of freedom in the design of material combinations without the common restrictions of the structure of the materials bonded. It is already an established method for the industrial production of advanced substrates (SOI) applied as basic material in high-performance device fabrication. SOI, i.e. a thin device layer on an insulator, is a promising concept for further device developments. The advantages of SOI can be combined with mobility enhancing materials such as strained silicon (SSOI) or germanium on insulator (GOI). The bonding process is not limited to a certain wafer diameter and is applicable to different material combinations which are important to integrate different functions on a chip (system on a chip, SoC).

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1 Introduction

The advances in silicon technology that have been the backbone of tremendous previous growth, was foreseen in 1965 when G. Moore published his famous prediction about the constant growth rate of chip complexity [1]. And, in fact, it has repeatedly been shown that the number of transistors integrated into silicon chips has indeed doubled every 18 months. Increases in packaging density, according to Moore´s law, are driven by two factors: reductions of production costs and increases in chip performance. The early concept of scaling for MOS transistors was to reduce all of the dimensions by the same amount α [2, 3]. Device and technology developments in recent years, however, have shown that scaling is more and more limited by material properties and power dissipation [4-6]. Especially improvements of the short-channel behaviour, current drive and switching behaviour are main issues to obtain the projected performance increase [5]. The application of advanced dielectrics (high-κ gate dielectrics) and multi-gate devices cause significant improvements of the short-channel behaviour, while scaling of the Silicon-on-Insulator (SOI) body thickness to reduce the capacitance affects the switching behaviour. Furthermore, mobility-enhancing measures through stress and substrate alternatives have been identified as most important material parameters to improve the current drive.

SOI substrates are widely used in today´s high-performance device processes. The advantages of SOI can be combined with mobility enhancing materials such as strained silicon, to form strained silicon on insulator (SSOI), or germanium on insulator (GOI). Especially the combination of the global strain of SSOI substrates with local stressors (process-induced strain) is required for the next device generation [7]. Also alternative substrates such as hybride orientation composites (HOT) [8] are under research. All these materials are engineered substrates realized by semiconductor wafer direct bonding techniques.

2 Physics and chemistry of semiconductor wafer direct bonding

Widespread interest in modern wafer bonding techniques was generated by reports on silicon-silicon wafer bonding about 20 years ago [9-11]. Semiconductor wafer direct bonding (SWDB) requires wafers with a high degree of flatness, parallelism and smoothness. Also clean surfaces are necessary which are free of particulate, organic, and metallic contaminations. This is important because the surface cleanliness has a direct effect on both the structural and electrical properties of the bonding interface as well as on the resulting electrical properties of the bonded material. After cleaning an activation of the surfaces is required prior to bonding. Then the two mating wafers are brought together face to face in air at room temperature. The top

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wafer is floating on the other due to the presence of a thin cushion of air between both wafers. When an external pressure is applied onto a small part of the pair to push out the intermediate air, a bond is allowed to be formed by surface attraction forces between the wafers at this location. For wafer bonding the interaction between two surfaces is important. The total energy of two planar surfaces at a distance D apart is given by [12] as

$$W = \frac{A}{12\pi}\left(\frac{1}{D_o^2} - \frac{1}{D^2}\right) = \frac{A}{12\pi D_o^2}\left(1 - \frac{D_o^2}{D^2}\right) \text{ per unit area,} \quad (1)$$

where W is the total energy, or adhesion energy, A the Hamaker constant, and D_o the interatomic distance. At D = D_o (both surfaces are in contact), W = 0, while for D = ∞ (two isolated surfaces),

$$W = A/12\pi D_o^2 = 2\gamma \quad (2)$$

or

$$\gamma = A/24\pi D_o^2 \quad (3)$$

in other words, the surface energy γ equals half the energy needed to separate two flat surfaces from contact to infinity, viz. it is half the adhesion energy. Adhesion is caused by different forces acting at an interface. Most important for wafer bonding are

a) capillary force,

b) electrostatic force initiated by Coulomb interaction between charged objects or from the contact potential between two surfaces caused by differences in the local energy states and electron work functions,

c) van der Waals force resulting from the interaction between instantaneous dipole moments of atoms,

d) solid bridging caused by impurites, and

e) hydrogen bonding between OH groups as the separation between the surfaces becomes small.

Measurements on silicon microstructures showed that capillary force dominates [13, 14]. It is about 2×10^2 µN per 1 µm^2 at a separation distance of two smooth silicon surfaces of 1 nm. Increasing the distance to 10 nm reduces the capillary force to about 5 µN. In addition, electrostatic forces, van der Waals forces, and hydrogen bonding are about one order of magnitude lower. For short distances between both surfaces (D ≅ 1 nm) hydrogen bridging and van der Waals forces are about 10 µN per 1 µm^2, while electrostatic forces reaches values of about 5 µN. All these forces act only over short ranges and the effect depends on the specific surface conditions. Most important is the surface roughness [15]. On the other hand, also the chemistry of species on the silicon surfaces affects the different forces.

2.1 Hydrophilic wafer bonding Silicon surfaces are covered with an oxide layer under room temperature conditions. If oxidized surfaces are bonded an oxide layer results in the interface (Fig. 1). XPS- and HREELS analyses [16] proved the existence of a large number of singular and associated OH groups causing the hydrophilicity of oxidized surfaces. A model for hydrophilic wafer bonding was first described by Stengl et al. [17] using the analogy of surface chemistry of silica and oxidized silicon. Based on

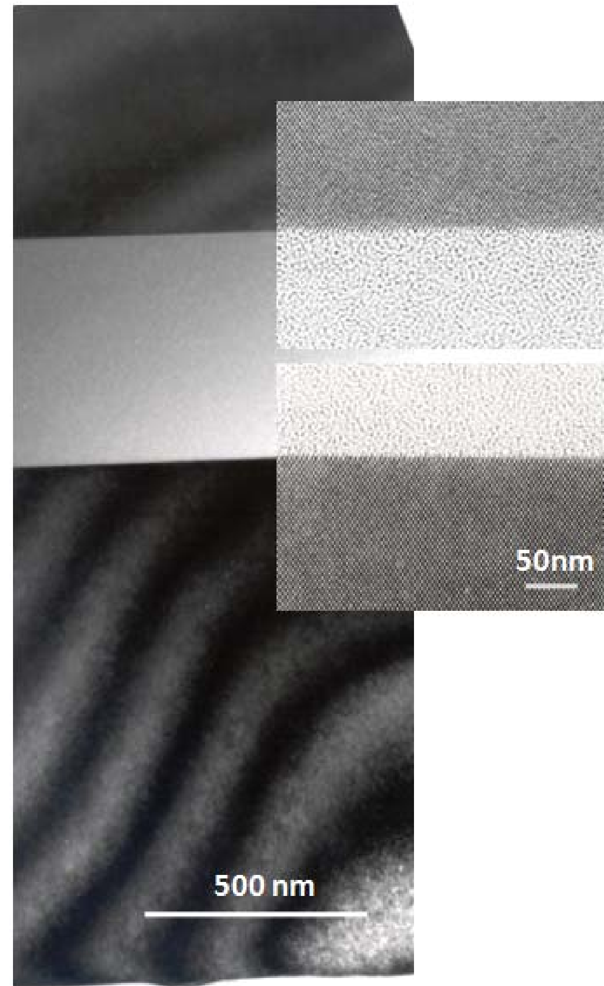

Figure 1 X-TEM image of the interface of bonded hydrophilic wafers. The inserts show high-resolution electron microscope images of both Si/SiO_2 interfaces.

results of infrared spectroscopy, a 3-dimensional hydrogen bonded network of water molecules was assumed. The water is primarily bonded via Si–OH groups on the silica surface. During heating above 180 °C the adsorbed water molecules desorb under atmospheric pressure leaving a hydroxylated silica surface, on which most of the SiO groups are linked via hydrogen atoms. OH groups are bonded more stable with increasing temperature.

The model was further developed by Tong and Goesele [18]. They proposed that for room temperature conditions, chains consisting of 3 or more hydrogen-bonded water molecules bridge the interface. This is based on the fact that hydrogen-bonded water triplets are more stable than single water molecules or dimers. They also pointed out that 2 main types of silanols are present on the oxide surface:

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singular silanols (Si–OH) and associated, or vicinal silanols (Si–OH–O–Si).

Another interpretation was given by Litton and Garofalini [19]. They discussed the presence of an additional type of silanol, the geminal silanol ($Si–(OH)_2$) found by NMR analysis on silica gel surfaces. It was also assumed that the mean siloxane (Si–O–Si) bond angle is lower (□130°) for thin oxides prepared by wet chemical cleaning than for bulk SiO_2 (□144°). This indicates that the oxide is strained due to the Si/SiO_2 interface.

Annealing after the initial bonding process at room temperature results in changes of the interface chemistry. Measurements of the interface energy of bonded hydrophilic wafers show a different behaviour for different temperature ranges [20]. Above 800 °C Si-O bonds are formed via the interface.

2.2 Hydrophobic wafer bonding When the oxide layer from a crystalline silicon substrate is removed with HF, a hydrophobic surface with unique properties is obtained, i.e., having a good resistance to chemical attacks and a low surface recombination velocity, which means a surface with a very low density of surface states.

Bonded hydrophobic wafers are characterized by completely different interfaces (Fig. 2). The removing of the oxide result, as in the case of bicrystals, that two silicon lattices are in contact. Crystal defects (dislocations) are generated forming a 2-dimensional network in order to match both crystal lattices. The dislocation structure depends on the misorientation. In general, the twist component causes a network of pure screw dislocations, while the tilt component is compensated by a periodic array of 60° dislocations.

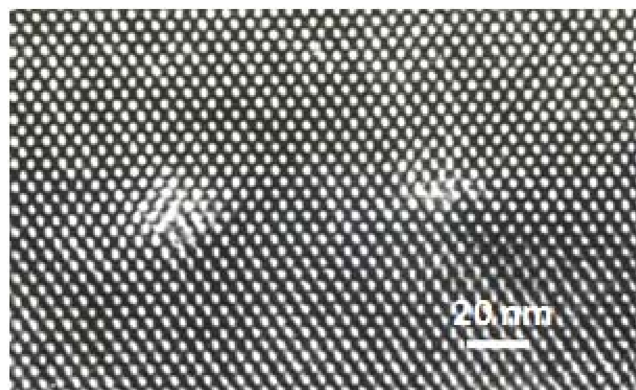

Figure 2 High-resolution electron microscope image (X-TEM) of the interface of bonded hydrophobic wafers. A 2-dimensional dislocation network is formed in the interface.

First detailed analyses of interfaces of bonded hydrophobic wafers were carried out by Bengtsson and Engström in 1989 [21]. A first concept for hydrophobic wafer bonding was presented by Bäcklund et al. [22, 23] suggesting van der Waals forces as the origin of the attraction forces. Further investigations assume the formation of hydrogen bonds via Si–F groups on the hydrophobic surface [20]. The surface energy was estimated by the equation

$$\gamma_s = \frac{1}{2}(2d_{Si-F} - d_{hHF}), \tag{4}$$

where $d_{Si–F}$ is the surface density of Si–F bonds and E_{hHF} is the lowest bond energy of the hydrogen bonded HF cluster across the two mating surfaces [18]. Using $d_{Si–F} = 1\times10^{14}$ cm^{-2} and E_{hHF} = 6.02 kcal/mol, the surface energy was calculated to be $\gamma \leq 42$ mJ/m^2, which is in accordance with experimentally measured data. Analyses of HF-treated surfaces and interfaces of bonded hydrophobic wafers proved the existence of fluorine, the main species, however, are hydrogen [16, 24-26]. This means that hydrogen bonds like Si–H · H–Si are probably more favoured. The contribution of the different hydrogen bonds depends on the pretreatment, i.e. if the hydrophobization is caused by diluted HF solutions, buffered HF solutions (HF/NH_4F, etc.), or by plasma etch techniques [27].

The behaviour of the interface energy on the annealing temperature is quite different for bonded hydrophobic wafers [20]. The interface energy is nearly constant for annealing temperatures up to 150 °C. At higher temperatures γ_s increases. But there are 2 different regimes. For 150 °C ≤ T ≤ 300 °C the increase of the interface energy is characterized by an activation energy of 0.21 eV, while an activation energy of 0.36 eV was determined for annealing at higher temperatures [18]. Both activation energies correlate to different interface processes. There is a relation to the existence of $Si–CH_x$ groups (stable up to about 400 °C) and Si–H groups detected up to about 600 °C on hydrophobic silicon surfaces [16].

3 Semiconductor wafer bonding techniques for advanced substrates

3.1 Silicon on insulator (SOI)

Besides others, ion implantation techniques such as SIMOX (Separation of Implanted OXygen) have been preferred in the SOI production over several years [28]. SIMOX requires the implantation of oxygen in the order of 1×10^{17} to 2×10^{18} cm^{-2}. The implantation of such a high dose needs special ion implanting tools and long implantation times. The implantation at high beam currents as well as additional high-temperature annealing steps cause the introduction of contaminants into the layers and the formation of lattice defects such as silicon islands in the buried oxide (Fig. 3). Different refinements of the SIMOX technique were introduced to improve the quality of the layers, such as ITOX – internal thermal oxidation, or SPIMOX – separation by plasma implantation of oxygen. Wafer bonding techniques based on layer splitting by the implantation of hydrogen, introduced by SOITEC and modified by Silicon Genesis, and the epitaxial layer transfer (ELTRAN) from Canon are alternative techniques of producing SOI wafers [28]. The quality of the single crystalline top layer,

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the reduced defect density and especially the reduction of the production costs drive the increase of the number of wafers produced by the wafer bonding approach.

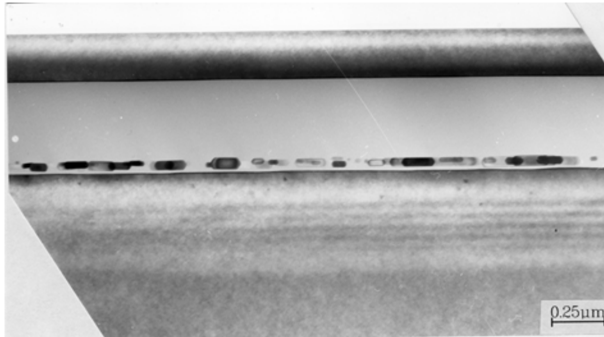

Figure 3 TEM cross-sectional image of a SIMOX wafer shows the presence of silicon islands in the burried oxide (BOX).

The combination of wafer bonding and layer transfer by hydrogen-induced splitting is the smartest and most effective method of producing SOI wafers. The behaviour of hydrogen (H) in silicon and other semiconductors have been studied for more than two decades. Hydrogen in single crystalline semiconductors has attracted growing interest because it was found that hydrogen passivates the electrical activity of many impurities including dopants, impurity atoms, defects and interfaces. If hydrogen ions are implanted at high doses (> 5×10^{16} cm^{-2}) platelet-like planar defects (microcavities) are generated on {100}- and {111}-planes near the implantation depth R_p. (Fig. 4). Some hydrogen ions bond to the dangling silicon bonds in the microcavities, while other fill these voids. If such an ion implanted wafer is heated up to 400-500 °C, more hydrogen segregates into the voids in the form of molecular hydrogen, the pressure builds up to a point of fracture, and blistering is obtained. The time required to generate optically detectable blisters on the surface depends on the temperature and annealing time. The so-called blistering time t_b is given by the relation [29]

$$1/t_b \propto \exp(-E_a/kT)\,, \tag{5}$$

where k is Boltzmann´s constant, T the absolute temperature, and E_a the activation energy of the process. The blistering phenomena caused by surface bombardement with hydrogen or inert gases (He) have been seen in the past, and all efforts were focused on preventing them. The invention of Bruel was to realize that the deleterious effect could be harnessed to accomplish a weakened plane or zone that makes it possible to attain a controlled cut through the crystalline lattice [30-32]. The key was to introduce a stiffener layer (another wafer bonded to the surface of the implanted wafer) that prevents blistering and redirects the pressure that builds up in microcavities in a lateral direction. The process is generally known as Smart Cut © [31, 32]. Analyses of the layer splitting kinetics showed 2 different activation energies indicating different processes in different temperature regimes [33]. At high

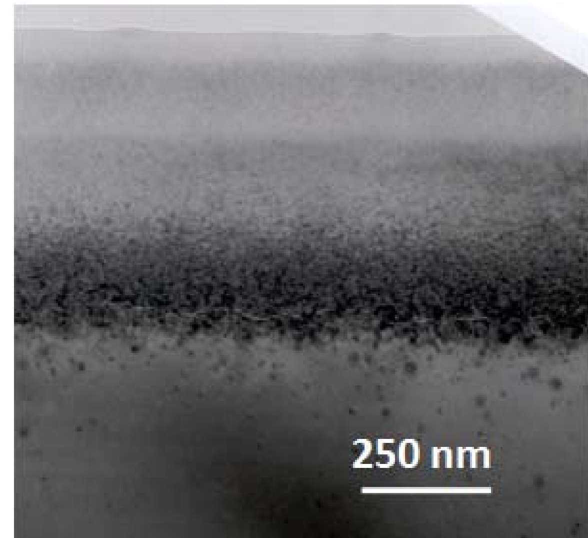

Figure 4 TEM cross-sectional image of hydrogen implanted Si wafer. A defect band (microcavities or platelets) is formed near the implantation depth R_p. Implantation conditions: H^+, 65 keV, dose 1×10^{17} cm^{-2}.

temperatures (T ≥ 400 °C), an activation energy of about 0.5 eV was found referring to the free atomic hydrogen diffusion (0.48 eV). At lower temperatures, the splitting activation energy is about 2.2 eV and refers to a trapping-detrapping phenomenon due to the trap efficiency in this temperature range.

The original approach of the hydrogen-induced layer splitting was modified in the past in several ways [28]. First, the implantation of H_2^+ instead of H^+ reduces the implantation dose and therefore also the risk of heating of the wafer during implantation. The temperature of the wafer during implantation is a critical issue. Furthermore, also the substitution of hydrogen by helium ions or the co-implantation of H^+ and He^+ were applied. Another approach uses a low dose boron implantation prior to hydrogen implantation which reduces the dose and/or annealing temperature required for layer splitting.

The main steps of the layer transfer approach combining hydrogen-induced layer splitting and wafer bonding are schematically drawn in Fig. 5. Hydrogen is implanted into the surface of an oxidized wafer (Fig. 5a). The thin oxide on the surface acts as a protection layer for contaminants during implantation and is applied as the buried oxide further on. The thickness of the thin silicon layer transferred is determined by the energy of the ions. After implantation and cleaning the wafer is bonded to another oxidized or bare silicon wafer (Fig. 5b) followed by an annealing (Fig. 5c). During the annealing the interface energy (bond energy) increases to a sufficiently high values and the layer

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splitting is initiated. To achieve both conditions, the annealing is usually carried out as a two step process combining a primary low-temperature step with a subsequent annealing step at a higher temperature. Finally a further annealing at high temperatures follows (Fig. 5d). The annealing is required to remove residual implanted hydrogen and related defects, to improve the electrical properties of the buried oxide and the bonded Si/SiO_2 interface as well as to reduce the surface roughness caused by the layer splitting.

Compared to conventional layer transfer methods which employ wafer bonding and polishing/etching thinning technique, e.g., bond-and-etched back SOI (BESOI),

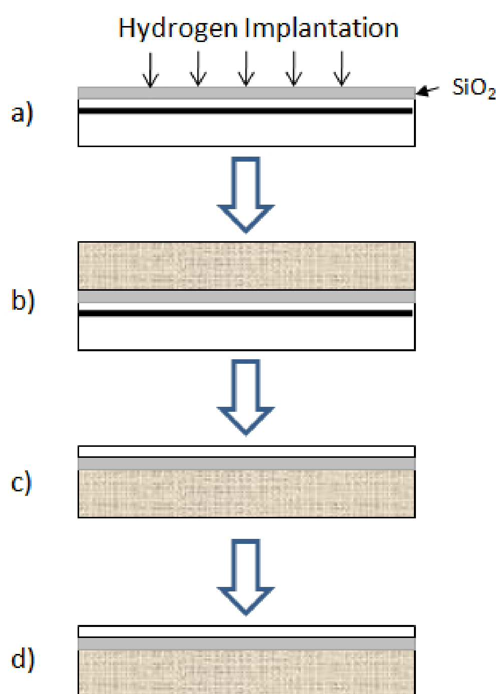

Figure 5 Schematic draw of the basic steps of the combined wafer bonding and layer transfer approach. The first step is a hydrogen implantation at a dose $\geq 5\times10^{16}$ cm^{-2} into a wafer covered with a thin oxide layer (a). The implanted wafer is bonded to another wafer (b) and subsequently annealed in order to introduce the layer splitting (c). Finally, the surface of the thin layer is smoothed by an additional high-temperature annealing and (if required) by CMP (d).

the ion implantation induced layer splitting has many advantages. First, a high thickness uniformity of the transferred layer is guaranteed by the ion implantation process which allows to control the implantation depth R_p (determining the thickness of the transferred layer) within a few percent over the whole wafer area. Furthermore, the implanted wafer can be reused for the next cycle after a short polishing step.

The thickness control and thickness uniformity are important issues for the application of SOI wafers in high-performance device fabrication. Today´s commercial SOI wafers for partially depleted CMOS applications are characterized by device layer thicknesses ranging from 90 nm down to 30 nm at a thickness uniformity of ± 3 nm. The wafer diameter is 300 mm. In addition, the thickness of the device layer for fully depleted CMOS is only 20-40 nm. The thickness uniformity here is ± 1 nm [34]. According to ITRS roadmap, however, further reduction of the device layer thickness is necessary for fully depleted CMOS [35]. One reason is that the combination of fully depleted SOI with high-κ dielectrics and metal gates minimizes the requirement for channel doping, thus strongly reducing the dopant dependence of the threshold voltage (V_T) and simplify the metal gate processing. Another significant advantage of a weakly doped channel is a much higher mobility. Moreover, due to its SOI nature and improved gate control, fully depleted devices exhibit a very low leakage even at higher temperatures, thus also significantly lowering static power consumption.

Besides reductions in the device layer thickness, SOI material with ultra-thin buried oxide layers (UT-BOX) is important for some applications. For very low power devices, for instance, UT-BOX offers the possibility to easily form buried n- and p-regions in the handle wafer, which can be used as back gates. By applying a back bias, the off current is reduced, while in the forward bias mode it lowers V_T resulting in a current drive increase [36]. Another advantage of UT-BOX SOI is the reduction of local MOSFET self-heating. An improvement by a factor of 3 in thermal conductance is obtained by reducing the BOX thickness from 150 nm to 20 nm [37].

3.2 Strained silicon on insulator (SSOI)

As device dimensions approach values below 100 nm, scaling becomes increasingly difficult. Strain engineering and material innovations have been identified as the main contributors to the continued performance improvement in CMOS devices. Besides SOI, significant improvements of the performance are obtained by an increased carrier mobility which has been reported for devices fabricated on strained silicon layers (for example [38-40]). Combining the advantages of SOI and strained silicon results in strained silicon on insulator (SSOI) substrates merging the properties of both materials.

For fabrication of SSOI wafers strained silicon (sSi) layers grow on a relaxed SiGe virtual substrate and were then transferred to oxidized Si handle wafers by direct wafer bonding. The strain in the silicon layer grown on a relaxed SiGe buffer is induced by the lattice mismatch between Si and SiGe. Because the lattice parameter of $Si_{1-x}Ge_x$ ($0 \leq x \leq 1$) alloys varies between 0.5431 nm for silicon (x = 0) and 0.5657 nm for germanium (x = 1) tensile strain is induced in a silicon layer. The strain is generally biaxial. There are different methods to realize sSi layers on SiGe virtual substrates [41, 42]. The growth of a re-

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laxed Si_{1-x} Ge_x buffer on a graded $Si_{1-x}Ge_x$ layer is mostly applied (Fig. 6a). Because the Ge concentration x increases continuously by about 10 % per µm, the thickness of the graded buffer is several micrometers. The sSi layer grows on top of the relaxed $Si_{1-x}Ge_x$ layer [43, 44]. An alternative is the relaxation of a thin pseudomorphic SiGe layer (< 500 nm) induced by hydrogen or helium implantation and subsequent annealing (Fig. 6b) [45, 46]. Thinner SiGe buffer makes the process costs effective. Variations of the basic structure (Fig. 6a) have been also published including dual channel structures incorporating an additional strained $Si_{1-y}Ge_y$ layer with y > x and heterostructures on bulk using a second strained silicon layer [41]. Layer stacks of the types a and b have been applied as virtual substrates for the preparation of SSOI and strained SiGe on insulator (SGOI) wafers. The realization of SSOI wafers from bulk materials is a complex process combining wafer bonding, hydrogen-induced layer transfer, and etch-back methods. Processes using thick SiGe buffer layers were described, for instance, in references [47-49], while a process using thin buffer layers was published in Ref. [50]. SSOI wafers up to 300 mm in diameter have been successfully realized.

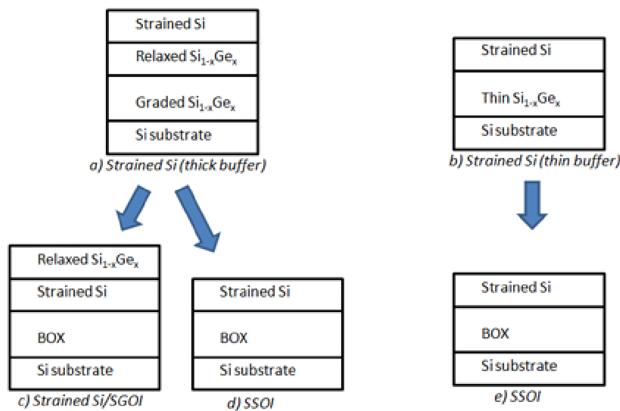

Figure 6 Schematic illustration of various heterostructure substrates produced by epitaxial growth on bulk substrates (a, b) and by transfer of the strained layers to oxidized substrates forming strained silicon on insulator (SSOI) (d, e) or strained Si/SiGe on insulator (SGOI) (c).

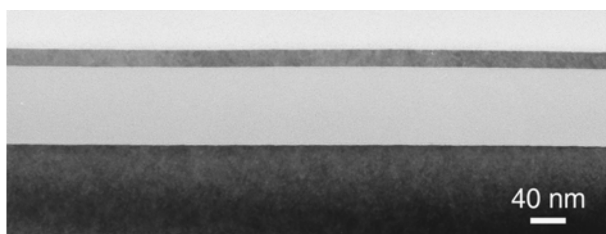

Figure 7 XTEM image of the final SSOI wafer prepared using virtual substrates with thin SiGe buffer layers (Fig. 6b). A 20 nm thick sSi layer was transferred on top of a 120 nm thick BOX layer.

Mobility enhancement in SSOI was reported in [41] and [50] for the different SSOI configurations. Furthermore, long channel devices (Lg ≥ 1µm) show clearly improvements of the device characteristics.

For instance, drive current (I_{DSAT}) improvements of 80% at the same source-to-drain leakage (I_{OFF}) have been measured compared to SOI material having the same device layer thickness. Improvements in the same order of magnitude were not obtained for short channel devices. Here, an I_{DAST} improvement of only 10-20% was proved up to now [50]. The main reason was the interaction with process-induced stressors reducing the effect of the biaxial strain [7]. This means that applications of SSOI wafers require modifications of existing CMOS processes. The combination of biaxially strained SSOI and optimized uniaxial stressors (dual-stress nitride capping layer and embedded SiGe) was already demonstrated resulting in I_{DSAT} improvements of 27% and 36% for n-channel MOSFETs and p-channel MOSFETs, respectively, in sub- 40 nm devices [51]. In addition, the gate leakage current was also reduced by 30%. All investigations suggest that the combination of biaxially strained SSOI and uniaxial strain by process-induced stressors is the optimum way for future requirements [41, 50, 51, 52].

3.3 Hydrophobic bonded wafers – hybrid orientation composites (HOT)

Wafer bonding techniques applied for SOI and SSOI fabrication uses hydrophilic surface conditions of the bonded wafers. As shown before (Section 2.2), bonding of hydrophobic wafers causes that both silicon lattices are in contact to each other without any interface (oxide) layer in between. But a 2-dimensional dislocation network is formed in the interface to adjust the lattice misfit. The advantage of the hydrophobic wafer bonding is the combination of wafers having different conduction type and resistivity (doping level). Using wafer bonding and thinning techniques wafers of the same conduction type but different resistivity are paired to produce stacks in analogy to epitaxial wafers. Combinations of n-type, medium doped substrates (corresponding to a resistivity value ρ = 10 20 Ωcm) with a low-doped (ρ = 500 Ωcm) wafer of the same conduction type (n-), acting as top layer after thinning, were used to fabricate low-capacity and high-speed photodiodes (pin-diodes) [53]. Properties of pin-diodes (dark current, photocurrent, CV- characteristics, rise time) were measured showing a comparable or improved behaviour to analogous devices prepared on conventional epitaxial material.

Hydrophobic wafer bonding also offers the possibility to combine wafers of different conduction type to form deep pn-junctions. Such materials are of interest for power device and automotive applications.

Another important application is the hydrophobic wafer bonding of wafers having different crystal orientations. The motivation was that hole mobility in silicon is more than doubled on {110}-oriented substrates with current

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flow direction along <110> compared to conventional {100}-substrates. However electron mobility is the highest on {100}- substrates. The combination of the transfer of a thin {110}-oriented layer on a {100}-oriented substrate, the patterning and etching of the thin layer, and a local epitaxial regrowth allow the fabrication of wafers having areas with different crystal orientation on the surface. The realization of such hybride substrates and the demonstration of the performance increase of p-FET devices were first published in 2003 by Yang et al. [54]. The approach of hybride substrates was modified over the last years either by applying hydrophobic wafer bonding or by hydrophilic wafer bonding using a thin oxide layer between both

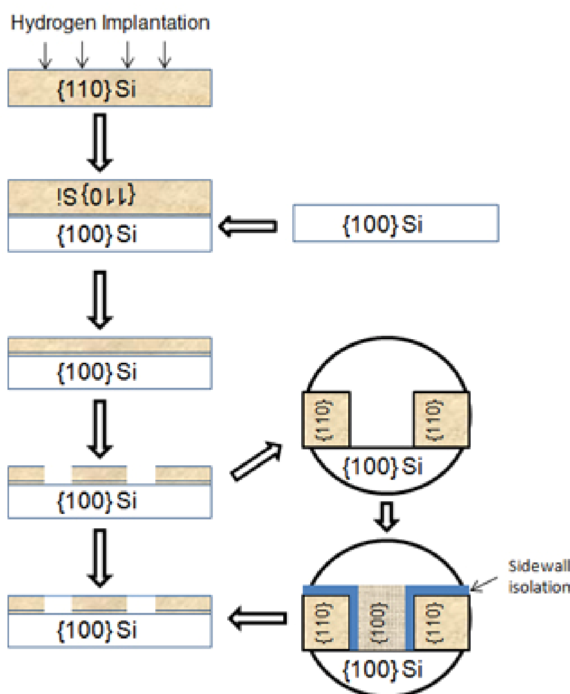

Figure 8 Schematic draw of main processes to realize hybride oriented wafers.

wafers (SOI) [55-57]. Substrates bonded under hydrophobic conditions were recently appointed as hybride orientation composites (HOT) [8]. The main process steps are schematically shown in Fig. 8. A {110}-oriented silicon wafer is implanted with hydrogen. Wafer bonding to a {100}-oriented substrate and a subsequent annealing causes that a thin layer of the {110}-oriented wafer is transferred to the {100}-oriented substrate. The transferred {110}-oriented layer is patterned by lithography followed by an etching up to the substrate. The sidewalls of the holes are isolated either by a thin oxide or nitride layer. The next step is a selective epitaxial deposition of silicon into the holes where the <100>- orientation of the islands is induced by the substrate. Finally, CMP is applied to planarize the surface. In addition, an amorphization by ion implantation followed by a recrystallization by solid phase epitaxy is an alternative approach to the etching and epitaxial regrowth [58]. An analogous process flow is applicable for {100}-oriented thin layers transferred to {110} substrates. This combination, however, is constrained by a more difficult epitaxial growth of Si on {110}.

The atomic contact of two silicon surfaces and their misfit are also the reason that defects (dislocations) generate in the interface of hydrophobic bonded wafer pairs. The dislocations produce a 2-dimensional network. The dislocation structure depends on the misorientation. In general, the twist component causes a network of pure screw dislocations, while the tilt component is compensated by a periodic array of 60° dislocations. The structure of both dislocation fractions were investigated for hydrophobic wafers bonded under environmental conditions [59-61] and under UHV conditions [62]. Detailed investigations of the dislocation networks in bonded interfaces showed numerous remarkable properties [63, 64]. Especially the luminescence properties of dislocations could be one of the most important applications in the future. The electroluminescence (EL) at about 1.5 µm of a p-n junction formed by direct bonding of p- and n-type wafers was already observed [65]. An efficient D1 emission at 1.5 µm from a MOS-LED based on the dislocation network in bonded wafers was also demonstrated [63]. When a dislocation network with appropriate structure is positioned near the Si/oxide interface, close to/within the accumulation layer, the radiative recombination is dominated by the D1 line at about 1.5 µm. The tunnelling current increases with increasing gate voltage, leading to an enhancement of the intensity of the electroluminescence (EL). The efficiency of the MOS-LED at 80 K is about 0.1% for the 1.5 µm radiation. Increasing of the temperature from 80 to 210 K causes a red-shift of the D1 line position in the spectra and a reduction of the EL intensity by a factor of about 2. Nevertheless, a sufficient 1.5 µm luminescence at 300 K is achievable with dislocation networks, since clearly detectable D1 emission at 300 K (efficiency $>$ 0.1%) was demonstrated already for a p-n LED containing a dislocation network. Using the amplification of the D-band luminescence caused by an external bias voltage across the dislocation network the efficiency might be considerably increased. The shift of the position of the D1 line in the spectra with the applied electric field refers to the Stark effect [66].

The carrier transport via dislocation networks is another remarkable property. The formation of 1-dimensional conductive channels by defects in silicon has already been demonstrated [67]. Analysis of dislocation networks in bonded interfaces revealed a similar feature. EBIC investigations on cross-sectional samples, for instance, proved bright contrasts along the bonded interface. This demonstrates transport of minority carriers along the dislocation network towards the collecting Schottky barrier. The transport of minority carriers over distances of more than 10 mm has been observed [67, 68]. The reason for the increases of the carrier transport is that dislocations represent channels of a reduced resistivity by dislocations. For demonstration a dislocation network was produced in the inter-

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face of 2 thin silicon layers by hydrophobic wafer bonding. The total thickness of the layer stack was 40 nm. Both layers make the device layer of a SOI wafer. Ohmic contacts were fabricated at a distance of 1 µm (Fig. 9a). The I-V characteristics measured at 300 K exhibits Ohmic character (Fig. 9b). The resistance of the structure yielded about $R_{disl} = 4\times10^2\ \Omega$, while a reference structure without a dislocation network in a 40 nm thick SOI layer result in a resistance of $R_{ref} = 2\times10^6\ \Omega$ [69]. Similar results about the reduced resistance by dislocation networks were also reported by Ishikawa et al. [70]. It is assumed that dislocations form "n-channels" in the surrounding p-type material and increase the electron concentration in the SOI layers. Because a very strong decrease of the resistance of 4 orders of magnitude was found, an increase of both, electron concentration and electron mobility was assumed [69].

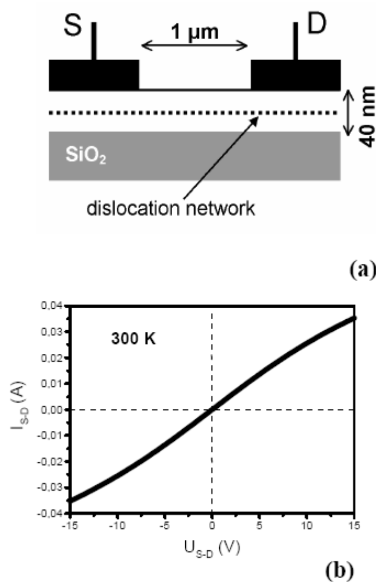

Figure 9 Schematic view of the sample containing a dislocation network within a 40 nm thick device layer (SOI) of p-type conductivity. The Ohmic contacts (S and D) are 5 µm wide and located at a distance of 1 µm. (b) I-V characteristics at 300 K revealing Ohmic character, yielding $R_{disl} = 4\times10^2\ \Omega$. For the reference sample without dislocations $R_{ref} = 2\times10^6\ \Omega$ was found [69].

This observation is consistent with the ballistic transport at dislocations in Si [71].

3.4 Germanium on insulator

The combination of different materials to form compliant substrates is another important application for semiconductor wafer bonding. For instance, the significantly larger bulk mobilities for both electrons (3900 vs. 1400 cm^2/Vs) and holes (1900 vs. 500 cm^2/Vs) for germanium over silicon lead to a resurgence of interest in Ge. Single crystalline Ge substrates are available up to 300 mm in diameter, but there are some significant disadvantages (extrem high material costs, higher density of Ge (5.32 g/cm^3) compared to silicon (2.33 g/cm^3) resulting in an about 2.3 times higher mass of a Ge wafer) making Ge wafers ineffective in mass production. Therefore Ge layers on silicon or Ge on insulator (GOI) are alternatives. Specific techniques have been applied to bond Ge wafers on Si or with an oxide layer in-between [72]. Figure 10 shows the acoustic microscope image of a bonded Ge/Si wafer pair after

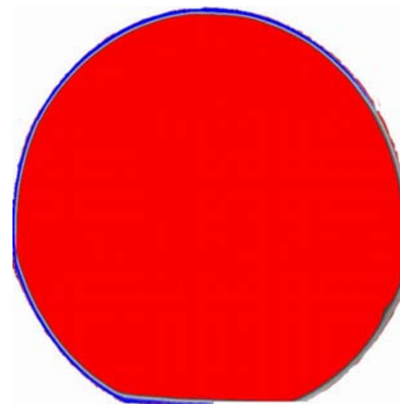

Figure 10 Acoustic microscope image of a bonded Si/Ge wafer pair after annealing at 250 °C for 8 hours. The wafer diameter is 150 mm. There are no defects in the interface detectable by this method (the lateral resolution is 20 µm).

annealing at 250 °C. A thin oxide layer (200 nm) is enclosed in the interface. There are no defects in the interface detectable by acoustic microscopy. The microscope operates at 100 MHz resulting in a lateral resolution of 20 µm. Using a pretreatment in an atmospheric plasma [72] the bond energy reaches values of about 1.5 J/m^2 even at low annealing temperatures.

The main problem for bonding wafers of different materials is the thermally induced stress during annealing. According to Hooke´s law the stress in a bonded Ge/Si wafer pair is given as

$$\sigma_{res}^{therm} = \frac{E}{1-\nu}\Delta\alpha \cdot \Delta T, \quad (6)$$

where E is the film elastic modulus (Ge), ν Poisson´s ration of the film, $\Delta\alpha = \alpha_{Ge} - \alpha_{Si}$ the difference of the thermal expanision coefficients, and ΔT the temperature change. Using

$$E_{Ge} = \frac{1}{s_{11}} = 103.73 GPa \text{ and } \nu = \frac{s_{12}}{s_{11}} = -0.2697\ , \quad (7)$$

with the compliance coefficients s_{ij} for Ge [73] and

$$\Delta\alpha = 3.668\times10^{-6} K^{-1} \quad (8)$$

one obtains

$$\sigma_{res}^{therm} = 0.2996\times10^{6} \cdot \Delta T\ \text{ Pa}\ . \quad (9)$$

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For bonded wafers a correction of Eq. (9) for thick layers is necessary

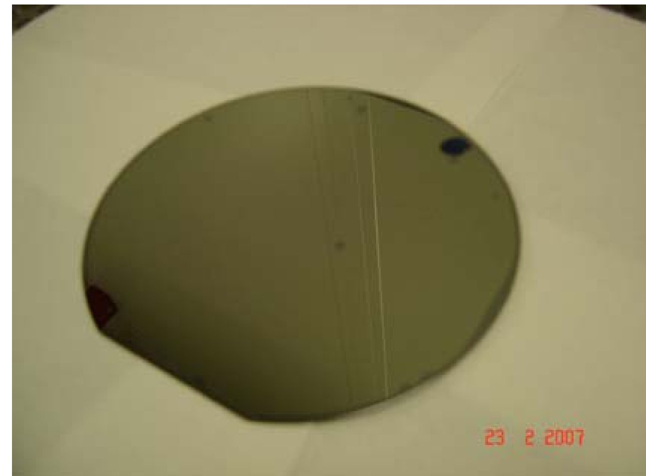
$$\sigma_0 = \sigma_{res}^{therm} \cdot \left[1 + (E_{Ge} / E_{Si}) \cdot (t/h)^3\right] / (1 + t/h) \quad . \qquad (10)$$

where h means the thickness of the substrate (Si) and t the thickness of the layer (Ge). Assuming a typical relation $t \approx h$ for bonded wafers, $\sigma_0 = 0.24\times10^6\cdot\Delta T$ (Pa). Changing the temperature by about 500 K (typical for annealing after bonding), a stress of about 100 MPa is induced. The stress causes bending of the wafers which can be calculated using the modified Stoney equation [74]:

$$R = \frac{E_{Si} \cdot h^2}{6 \cdot t \cdot \sigma_0} \qquad (11)$$

with R as the radius of curvature of the Si substrate and $E_{Si} = E/(1-\nu)$ as the biaxial elastic modulus of silicon. At room temperature R = 1.2 m follows from Eq. (11). Furthermore, increasing the wafer diameter causes that the relation t/h > 1 (typical thicknesses of Ge wafers (diameter 200 mm) are about 900 µm, while Si wafers of the same diameter are only 750 µm thick). This result in a further increase of the thermally induced stress yielding that debonding of the wafers is obtained even at low annealing temperatures if the bond energy (interface energy) is also low. Bonding Ge direct to a silicon wafer without an oxide layer in-between involves an additional type of stress induced by the lattice mismatch. Compared to the thermally induced stress the stress induced by the lattice mismatch is about a factor of 100 higher and is the reason that wafers break during annealing.

A more effective way to fabricate such compliant substrates is the transfer of thin layers (Ge) to a silicon substrate instead of the bonding of bulk wafers. Because the relation t/h in Eq. (10) is drastically reduced ($t/h \ll 1$) the transfer of a thin layer lowers the thermally induced stress significantly. Moreover, applying the Ge on insulator (GOI) approach stress induced by lattice mismatch is not observed. Wafer bonding techniques have recently been published using combinations of wafer bonding and hydrogen-induced layer splitting [75-77]. These techniques apply thin Ge layers produced either by hydrogen implantation into Ge wafers [75, 76] or, in a smarter and more competitive way, by transferring of Ge layers grown by CVD methods on silicon substrates [77]. The crucial problem of Ge layers grown epitaxially on Si is the high threading dislocation density. The dislocation density is reduced to about $6\cdot10^6$ cm^{-2} by applying graded buffer layers or by a 2-step growth process consisting of a low-temperature seed followed by the growth of a relaxed Ge layer at higher temperatures (600 °C-800 °C) [78, 79]. The thickness of the grown Ge layer is 1-2 µm [77]. An alternative is the formation of thin buffer layers grown at low-temperature by MBE [80, 81] allowing the growth and transfer of thin



a)

b)

Figure 11 Image of a GOI wafer (a). The wafer diameter is 150 mm. TEM cross-sectional image of a GOI wafer (b) shows the Ge layer on a buried oxide (thickness 200 nm). The dislocation density in the Ge layer is about 1×10^7 cm^{-2}.

Ge layers required to the production of high performance devices. Figure 11 shows a GOI wafer realized by the transfer of a thin MBE-grown Ge layer on an oxidized Si substrate. The threading dislocation (TD) density in this case is about 1×10^7 cm^{-2} but it was recently demonstrated that Ge layers with a lower TD density and thicknesses down to 30 nm have been realized and applied to fabricate GOI wafers up to 200 mm in diameter [82].

3.5 Other materials

Wafer bonding techniques are also applied to combine other dissimilar materials which could be of interest for future electronic applications. The research in this area is mainly driven by required combinations of electronic components with other functions to realize systems on a chip (SoC) integrating all components or other electronic systems into a single integrated circuit. Today's SoC's contain already digital, analog, mixed signal, and RF functions but future applications need also the integration of optoelectronic components (e.g. for optical data communication) or other functionalities. Large progress was obtained during

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the last years for wafer bonding of numerous materials including III/V- and II/VI-compounds, SiC, and complex oxides ($LiNbO_3$, $SrTiO_3$, etc.). Current reviews are presented for instance in [83, 84].

4 Conclusions

Semiconductor wafer direct bonding offers a new degree of freedom in the design of material combinations without the common restrictions of the structure (amorphous, polycrystalline, orientation, lattice constant) of the materials to be bonded. It is already established for industrial fabrication of advanced substrates (SOI) and is a key technology for further developments in this area (SSOI, GOI).

The basic processes of semiconductor wafer bonding are well understood for silicon. This includes the chemical and physical processes on silicon surfaces and bonded interfaces, the mechanical properties of bonded structures, the effect of thermal treatments after the bonding process, and the behaviour of bonded wafers during following device process steps. Further research, however, is required to realize SOI and other engineered substrates with ultrathin device layers (as for fully depleted devices) as well as the preparation of other dissimilar substrates.

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