

Performance Analysis of a Chaos-Based Multi-User Communication System Implemented in DSP Technology

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Abstract

This paper presents the implementation of a multi-user chaos-based communication system in DSP. The system is based on the chaotic phase shift keying (CPSK) digital modulation scheme, where chaotic signals are used as the spreading sequences of a CDMA system. Using chaotic signals offers the advantages of increased security and higher system capacity compared with conventional sequences. The aim of this hardware implementation was to enable a comparison against analytical performance results for CPSK. The transceiver prototype was implemented on a 32-bit floating-point TigerSHARC DSP. Its bit error rate (BER) characteristics were measured in the presence of additive white Gaussian noise. The prototype achieves excellent BER performance, matching that of theoretical CPSK. The effects of the limited number precision of the hardware platform are thus negligible. However, due to the limited concurrency of DSP, the multi-user system only supports low data rates.

1. Introduction

In the past fifteen years, there has been a tremendous growth in the demand for personal telecommunication services. Accordingly, wireless communication systems have become the most significant area of technological development in the field of telecommunications today [1].

In a wireless digital communication system multiple users require simultaneous access to the communication channel. The most widely used multiple access technique in digital cellular systems is Code Division Multiple Access (CDMA) [2]. This is due to its advantages of increased system capacity and higher security [3]. CDMA is a spread-spectrum system, allowing users' signals to overlap both in frequency and time by assigning each user a unique 'spreading code' [2].

Recently, chaotic signals have emerged as a promising alternative to the classical CDMA spreading codes (Walsh functions) [2]. Chaotic signals are random-like, aperiodic signals. They are produced by non-linear

dynamic systems characterised by a sensitive dependence on initial conditions [3]. The highly irregular and complex structure of chaotic signals provides increased security over Walsh functions [3]. Theoretically, an infinite number of uncorrelated chaotic signals may be generated, offering the further advantage of increased system capacity [2, 3].

This paper presents the results of the implementation of a chaos-based multi-user communication system in DSP (Digital Signal Processor) technology. The motivation for this hardware implementation was to enable comparison against the analytical performance results presented in [4]. To test the system's performance, its bit error rate (BER) characteristics were measured in the presence of additive white Gaussian noise (AWGN). A further aim of this project was to determine the maximum number of users and speed of operation that are achievable on the DSP hardware platform.

The paper is structured in the following way. Firstly, an overview of the theory behind multi-user digital communication systems and chaos-based communications is given. This is followed by a discussion of the issues that arise in a hardware implementation for the chaos-based system. The design of the implemented transceiver is then described, along with the details of the testing employed in the evaluation of the system. Finally, the results of the performance analysis undertaken are presented and discussed.

2. Theoretical background

A general multi-user digital communication system based on CDMA principles is shown in Figure 1. Each user's information, represented by a sequence of message symbols, m_n , is encoded with a unique 'pseudo-noise' basis signal, $\phi_n(t)$, corresponding to the spreading code of a CDMA system [5]. The spreading sequence bit rate is higher than the user data bit rate, so that several samples of the basis signal are modulated by each message symbol. The number of spreading sequence samples per message symbol is termed the spreading factor [3].

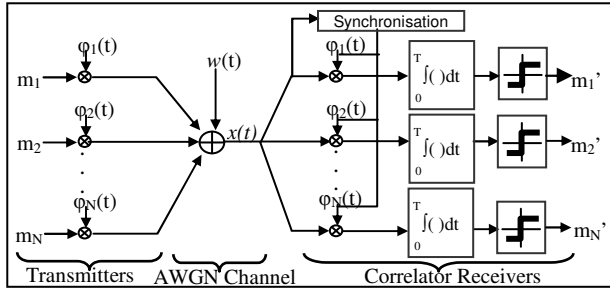


Figure 1. Multi-user CDMA digital communication system (Adaptation from [4])

The composite N-user signal passes through an analog communication channel where it is corrupted by background noise $w(t)$, which is additive, white and Gaussian. The individual signals are separated at the receiver using correlation, by exploiting the orthogonality property of the basis signals used. Namely, two orthogonal basis signals will have a cross-correlation product of zero. Thus with proper synchronisation, correlating the composite received signal, $x(t)$, with a user's unique basis signal will recover that user's original message, with minimal interference from the other users' signals. Based on the output of the correlator, the threshold decision circuit finally makes an estimate, m_n' , of each original transmitted message symbol.

The bit error rate (BER) measure is used to evaluate the performance of a digital communication system. It represents the probability of bit error and is given by the proportion of the original message bits which are erroneously decoded at the receiver. The BER is measured at different values of signal to noise ratio (SNR), denoted by E_b/N_o , representing the ratio of the energies of the transmitted message bit and the channel noise [5].

The system presented in this paper uses the digital modulation method of chaotic phase shift keying (CPSK), as proposed by Sandhu and Berber in [4]. In CPSK the chaotic basis signal, $\phi_n(t)$, is modulated by message symbols of Polar Non-Return to Zero (NRZ) encoding (+1 or -1). Thus, the resulting CPSK signal at the output of the transmitter for the n^{th} user alternates between $\phi_n(t)$, or the inverted version of $\phi_n(t)$, respectively.

Chaotic signals may be generated using a chaotic map, which is a recursive discrete-time representation of the chaotic system. An example is the Logistic map,

$$X_n = 1 - 2(X_{n-1})^2. \quad (1)$$

The property of sensitivity to initial conditions means that Equation (1) will produce entirely different signals by altering slightly the initial condition (X_0) used to start the chaotic sequence. It should also be noted that these signals are bounded between 1 and -1.

3. Hardware implementation of the chaotic communication system in DSP

The limited precision number representation inherent in a hardware platform such as DSP means that the chaotic samples will be rounded or truncated as they are generated. This loss of infinite precision means that any chaotic sequence generated will eventually have to repeat itself, becoming periodic, thus losing its favourable quasi-random property. Furthermore, the real-time hardware environment imposes bit rate and capacity limits on the multi-user CPSK system, since only a finite number of operations can be performed in a given time period.

The existing DSP implementations of chaotic communication systems to be found in the literature [6,7,8,9,10] concern themselves with rather basic issues, all being only single user systems, with no BER characteristics reported.

The DSP processor chosen for the implementation of the CPSK multi-user communication system is the ADSP-TS201S TigerSHARC 32-bit floating-point processor from Analog Devices. The word-length of 32 bits was chosen to provide sufficient precision for chaotic sample generation while accommodating multiple users. A floating-point processor was chosen because it can accommodate a wide dynamic range, as required in order to implement both a chaotic and noise generator in DSP. Additionally, although arithmetic operations are typically faster using a fixed-point number representation, extra scaling operations would be required, negating any anticipated speed gain.

Furthermore, maximising the capacity of the CPSK system requires as fast as possible a processor. TigerSHARC has the fastest execution speed among competing DSP processors, with a processor clock speed of 600MHz and being capable of performing 2400MIPS, 3600MFLOPS, and 1200MMACS.

This prototype was developed using the TS201S EZ-KIT Lite evaluation board for the TigerSHARC processor in conjunction with the VisualDSP++ development environment. The functionality of the CPSK system is specified in software written in the high-level C language and transferred to the processor's assembly language using VisualDSP++. Loading the executable code onto the DSP, debugging the software and running the required simulations was enabled by communication between VisualDSP++ on a PC and the evaluation board.

4. CPSK transceiver design

The multi-user CPSK system, as represented by Figure 1, was implemented in DSP as shown in the functional block diagram of Figure 2. It should be noted that while the synchronisation block of Figure 1 is crucial

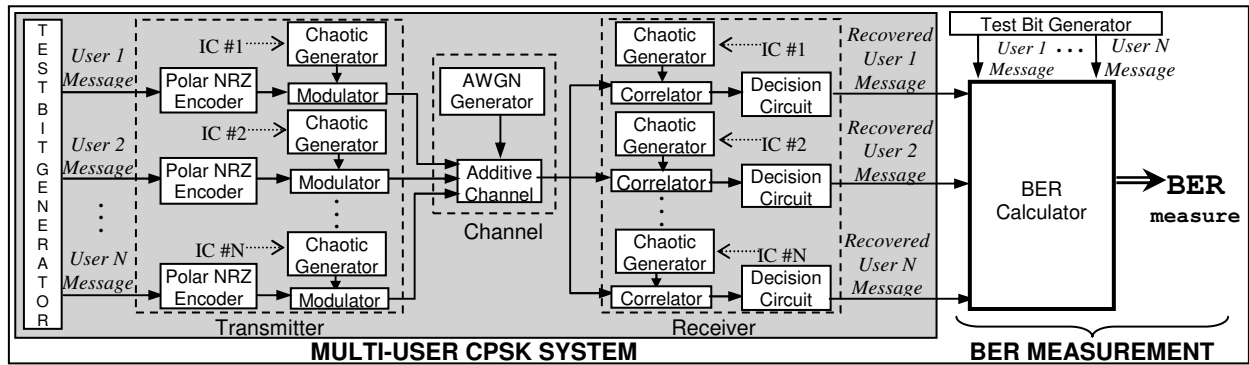


Figure 2. Functional block diagram of the multi-user CPSK system and BER measurement system

for a practical system, it was not a part of this implementation; proper synchronisation at the receiver was assumed (artificially arranged).

For the purpose of BER measurement, the analog communication channel is simulated inside the DSP using the AWGN generator. Therefore, the entire CPSK system of Figure 2 was implemented on a single DSP chip.

The functional blocks in the system diagram of Figure 2 are implemented modularly as separate functions in the C language description of the system. The Polar NRZ encoder converts the user message (1,0) into the required format (1, -1) for input to the modulator block, which is simply a multiplier. Similarly, the additive channel simply sums its input signals. Each individual user's message must modulate a different chaotic sequence produced from a unique initial condition (IC). The same IC must be used at the receiver to recover that message. The noise is added to the composite transmitted signal, while each correlator processes the composite received signal.

The chaotic generator block is based on the Logistic map of (1). Chaotic sequences generated on the DSP from 1000 different initial conditions were examined. A periodicity of 2240 samples was almost invariably observed. This is caused by each of these sequences eventually striking the particular value of 0.9996157. Following this, each chaotic sequence enters into the same 2240-sample long repeating pattern. The length of the unique sequence generated before this pattern is reached was also of interest. It was observed that over a quarter of the initial conditions investigated produce a unique sequence of over 5800 samples in length, with the longest of these containing 8275 samples.

To ensure good correlation properties, each chaotic sequence used must be unique. However due to the limited precision of the DSP, chaotic sequences generated from unique initial conditions eventually all turn into the identical repeating sequence. In order to prevent this, the

chaotic generator is periodically re-initialised with the initial condition. This occurs just before the repeating pattern would be entered into.

Thus, the chaotic generator operates by assigning each user a different IC and the accompanying unique sequence length. These are provided from a list available at both the transmitter and receiver. This list was compiled from the 256 initial conditions yielding the longest unique sequence lengths.

The operation of the correlator block consists of multiplying the received signal with the locally generated chaotic sequence, sample by sample, and computing a cumulative sum of these multiplication results for the number of samples equal to the spreading factor. As the original message symbols are either 1 or -1, the output of the correlator over a single transmitted symbol period will either be a large positive or a large negative value, respectively. Therefore to determine a best estimate of the transmitted message bit, the decision circuit block compares the output of the correlator with a zero threshold.

5. CPSK system testing

The transceiver prototype was tested by using a 511-bit pseudo-random test pattern implemented using a 9-stage shift register, as specified by the International Telecommunications Union (ITU) for error performance measurements of digital systems [11]. The test bit generator block (Fig. 2) generates each user's message by assigning one bit from this sequence to each user in turn. The identical test bit generator is available to the BER calculator, for comparison against the recovered messages.

The AWGN generator was implemented in DSP using a combination of the Box-Muller and CLT (central limit theorem) methods [12]. The Box-Muller method generates a random sample n of the Gaussian random variable $N(0,1)$ from two independent samples x_1 and x_2

of a random variable uniformly distributed over [0,1], as given by

$$n = (\sqrt{-\ln(x_1)})(\sqrt{2} \cos(2\pi x_2)). \quad (2)$$

Several values of n are then summed according to the CLT to produce a single Gaussian noise sample. The DSP implementation uses two accumulations of n , which is obtained by directly computing (2). The random samples x_1 and x_2 are generated by the *rand()* function in C.

The statistical characteristics of the noise generator have been confirmed to be satisfactory by generating 10^9 noise samples and examining the resulting distribution up to 4σ . The average relative error from the ideal Gaussian distribution is 0.2%, with a maximum relative error of 1.4% at 3.52σ .

The lengths of test sequences required for an accurate BER measurement of this system were determined using the technique proposed by Berber in [13], called the controlled accuracy (CA) technique based on the transformed Monte Carlo (TMC) method. The accuracy of the measurement is specified by

$$S = \text{Prob} \{ \hat{p} - k\hat{p} \leq p \leq \hat{p} + k\hat{p} \}, \quad (3)$$

where S gives the probability that the true BER value p will lie within the measured BER value \hat{p} , and k determines the width of the confidence interval. The number of samples in the test sequence, r , is then determined using

$$r = \left(\frac{\sqrt{2} \text{erf}^{-1} S}{k} \right)^2 \left(\frac{1}{\hat{p}} - 1 \right). \quad (4)$$

The BER measurements performed on the CPSK system are within 10% of the true probability of error, with 99% certainty ($S=0.99$, $k=0.1$). In the case of a BER measurement being made which fell outside the specified confidence interval, the length of the test sequence was recalculated with the measured BER serving as the new value of \hat{p} , and the measurement was repeated.

Measurements were also made to estimate the speed of the transmitter and receiver modules of the multi-user CPSK system. By counting the number of clock cycles needed to send or receive a 10^6 -bit long message consisting of all 1's, an estimate of the user data rate was obtained using

$$\text{Bit Rate} = \left(\frac{\text{Number of bits sent} * \text{Clock frequency}}{\text{Clock cycles} * \text{Number of users}} \right). \quad (5)$$

6. Results of performance analysis

6.1. BER measurement results

The BER of the CPSK system prototype was measured in the presence of AWGN at the E_b/N_0 levels of -3dB to 8dB. Simulations were carried out to investigate the

effect of varying the spreading factor and the number of users on the BER performance of the prototype. All of the BER results presented here are benchmarked against those of a BPSK (binary phase shift keying) system. It should be noted that the error bars in the following BER plots represent a measurement accuracy of $\pm 10\%$. The theoretical CPSK results [4] are also shown for comparison.

The results of the spreading factor investigation are presented in Figure 3. This is a BER plot for a four-user CPSK system using the spreading factors of 32, 64, 100 and 128. The BER reduces as the spreading factor is increased. However, a higher spreading factor means it takes longer to send a single message bit. A spreading factor of 100 achieves a significant improvement in BER compared with spreading factors of 32 and 64.

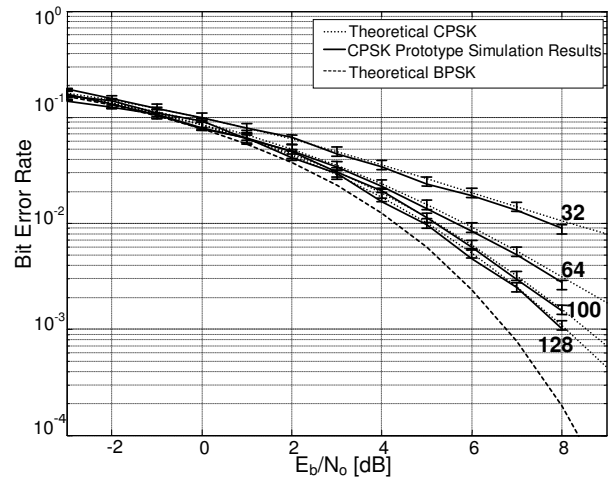


Figure 3. BER for a four-user CPSK system using spreading factors 32, 64, 100, 128

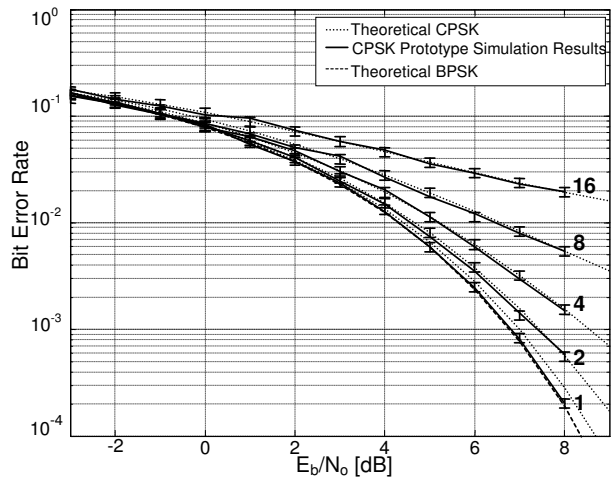


Figure 4. BER for a 1, 2, 4, 8 and 16 user CPSK system, spreading factor of 100

The continued improvement in BER with a spreading factor of 128 is considered to be insufficient to warrant the resulting 20% decrease in data rate. Thus, a spreading factor of 100 was found to achieve the best compromise between BER performance and speed.

The BER performance of the multi-user CPSK system for different numbers of users is shown in Figure 4. A spreading factor of 100 was used in these simulations, for the reasons outlined above. The effect of inter-user interference can be seen in the increasing BER for an increasing number of users in the system.

The BER measurement results for the prototype CPSK system match the theoretical CPSK results very well. Therefore, the hardware effects of the TigerSHARC DSP platform have a negligible impact on the BER performance of the CPSK system.

It should be noted that in some instances the BER results for the CPSK prototype appear to perform better than the theoretical CPSK results presented (Fig. 3, 4). This is due to the fact that the theoretical curves shown in these figures are based on analytical formulas which are Gaussian approximations [14]. The discrepancy between these Gaussian approximation curves and the true theoretical BER values is most pronounced for a low spreading factor (Fig. 3) and a low number of users (Fig. 4). A more rigorous technique [14] for deriving the theoretical BER of CPSK involves considering the exact probability distribution of the chaotic signal. This technique yields a more accurate prediction of the BER, which very closely agrees with the measurements obtained for the CPSK prototype.

6.2. Image transmission results

The results of image transmission shown in Figure 5 further illustrate the effects of AWGN and inter-user interference on the reliability of the CPSK system.

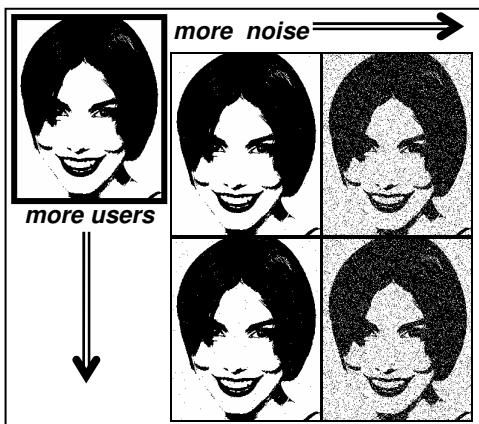


Figure 5. Image transmission results for a 1 and 4 user CPSK system at E_b/N_0 8dB, 0dB

The original image at the transmitter is shown in the top left corner. As predicted by the BER results, the quality of the recovered image degrades as both the level of the noise and the number of users in the system increase.

6.3 Speed estimation results

The maximum bit rates per user measured for the CPSK prototype at the transmitter and receiver are shown in Figure 6. The spreading factor of 64 was used to comply with the IS-95 CDMA standard [15]. Due to the limited parallelism implemented by the DSP platform, the bit rate per user decreases as more users are added to the system. Furthermore, the receiver achieves lower data rates compared with the transmitter. This is caused by the large amount of processing required to ‘simultaneously’ perform multiple correlations at the receiver. The prototype can support 1 user at a data rate of 19.2 kb/s required by the IS-95 cellular system [15].

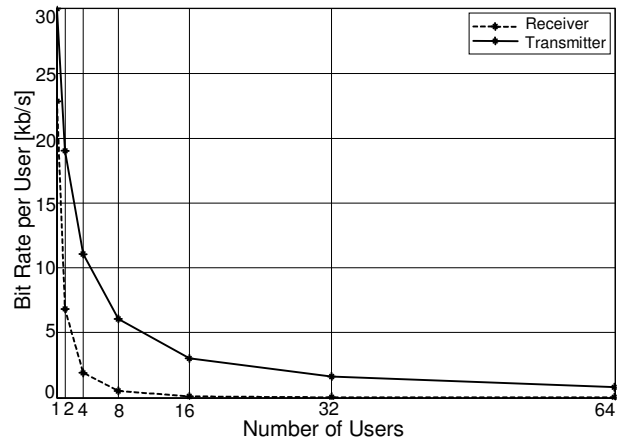


Figure 6. Speed estimation for the multi-user CPSK prototype on a TigerSHARC DSP

7. Conclusions

The design and testing of a multi-user CPSK system implemented on a 32-bit floating-point TigerSHARC DSP were presented in this paper. The prototype was developed using the high-level C language and tested on the target DSP using the TS201S EZ-KIT Lite evaluation board from Analog Devices.

The periodicity of the chaotic sequences generated by the prototype ranges from 5800 to 8275 samples. Currently 256 unique spreading sequences based on the Logistic map have been identified. For comparison, there are 64 spreading sequences in a Walsh function set. Potentially many more suitable initial conditions can be found. Including other chaotic maps would further increase the number of available spreading sequences.

The results of BER measurements on the prototype in the presence of AWGN match the theoretical results for CPSK very well. From this, we may conclude that the limited precision number representation of the DSP hardware platform has a negligible impact on the BER performance of the multi-user prototype system.

The speed of the DSP platform limits the capacity of the system to supporting one user at the data rates required by the cellular CDMA IS-95 standard. Therefore, the current implementation is not fast enough to be suitable for implementing a complete cellular CDMA system. However, the increased security and system capacity offered by chaotic spreading sequences remains an important advantage of CPSK. Therefore, given the fact that processor speed is continually improving, the CPSK scheme is a promising and viable CDMA option for the future.

Proposed future work in developing a practical CPSK system includes the implementation of a synchronisation block and the addition of the required RF elements to the transceiver to enable wireless transmission. This DSP implementation should also be compared with one on an FPGA platform. Ideally, there may be a way to combine the advantages of the two hardware platforms in a 'hybrid' implementation of the CPSK multi-user system.

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8. References

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