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Experimental study of depletion mode Si/SiGe MOSFETs for Low-Temperature Operation

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Abstract

N-channel enhancement mode Si/SiGe MOSFETs are characterised and studied over a wide temperature range of 10K<T<300K. It is shown that the sensitivity of quantum well based MODFETs to temperature changes results in an optimal operation temperature around 80K. The influence of LDD structures at sufficiently high drain voltages is analysed.

1. Introduction

Si/SiGe Modulation-Doped Field-Effect Transistors oxide-gated (called hereafter Si/SiGe MOSFET) have attracted much attention for their improved performance compared to conventional Si MOSFETs. This improvement is due to many factors: i) the use of Si:SiGe quantum wells to create a channel away from the SiO_2-semiconductor interface, ii) modulation doping which separates the doping atoms from the channel, and iii) strain which leads to reduced effective mass and lowered carrier scattering. These features have been shown to improve carrier mobility. Moreover, the use of SiGe allows for a Si compatible process, however with a reduced temperature budget [1].
Due to the limit imposed on the thermal load of the SiGe devices during processing, low temperature oxidation (800°C) has to be performed to avoid diffusion of doping atoms and Ge. The quality of this low T oxide however, is reduced compared to the full thermal process oxide (1000°C) resulting in higher gate leakage currents. Moreover, the use of relaxed SiGe virtual substrates (VS), where strain relaxation occurs through the formation of dislocations, increases the substrate leakage currents and thus the off-currents of the MODFETs.

Low-temperature operation of Si MOSFETs has shown promising improvements in their operation [2]. The decrease in temperature increases carrier mobility and decreases gate leakage currents. These features can also be employed to optimize the characteristics of SiGe MODFETs. Moreover, in the present (VS) devices, substrate leakage currents are governed by dislocations rather than impact ionisation, therefore substrate leakage currents decrease also with temperature. The reduction of leakage currents and enhancement of mobility makes low temperature operation of MOS-gated MODFETs on SiGe VS interesting as long as the operation enhancement occurs at temperatures above 77 K.
Improved HF performance of Si:SiGe Schottky-gated MODFETs has already been demonstrated at 50K [3] and a SiGe FATFET [4] was studied at 4.2K showing improved transconductance values. Although extensive research has been done on the low temperature operation of Si MOSFETs and CMOS [5], no consistent analysis of the device performance of Si:SiGe MODFETs has been done over a wide temperature range.
In this paper we present measurements of n-channel depletion mode (d-mode) Si/SiGe MOSFETs over a temperature range between 10K and 350K. Measurements were done for high and low bias conditions.

2. Device structure

Depletion mode devices were grown by UHV-CVD on p-type Si substrates. The schematic layer structure and processed structure are given in Fig. 1. The VS is a p-doped layer graded from 0% to 30% Ge covered with a 500 nm p-doped constant composition $Si_{0.7}Ge_{0.3}$ layer designed to reduce the number of threading dislocations in the active layers [6]. Doping is achieved with As in

the supply layer n=2 10^{18} cm^{-3} and B for p-doped regions p=5 10^{17} cm^{-3}. The thickness of the enhancement mode supply layer is 6nm. Device isolation is achieved by mesa etching into the p-type virtual substrate.
Gate oxides were grown by thermal oxidation at 750°C to a thickness of ~4nm. Source and drain contacts of Ti/Si were defined self-aligned to the poly silicon gate using LDD and HDD implantation techniques similar to CMOS processing, but without side wall spacers surrounding the gate. The gate length and width of the devices is 0.3µm and 100µm, respectively.

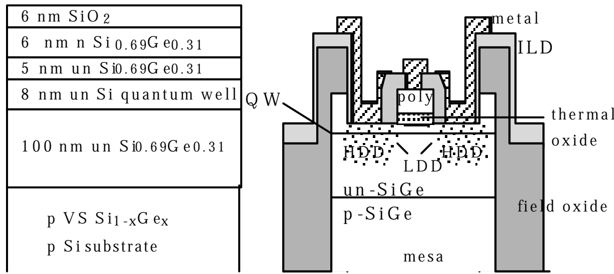

Figure 1: Left: layer structure. Right: schematic layout of the processed device.

3. Experimental results

The measurements were performed using a Janis CCS 350T closed cycle cryostat for temperature control down to 10K, and Keithley 236 source measurement units for voltage control and current measurement.

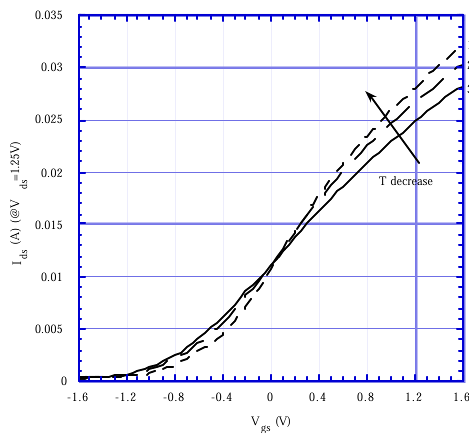

Figure 2: Source-drain current as a function of gate voltage for 3 temperature values: 300K, 200K and 140K.

Depletion mode quantum well channel (QWC) MODFETs function well down to very low temperatures because the amount of carriers in the QWC stay relatively abundant despite the freeze-out of the supply layer [3]. The freeze-out of the LDD doping [2] does not inhibit contacting the channel since the degenerately doped HDD layer is still in contact with the populated QWC. Moreover, at higher source-drain bias, impact ionisation overcomes partly the increased access resistance to the channel due to the freeze-out of carriers [7]. The situation for low bias conditions is different since the relative contribution of the leakage currents increases and the freeze-out of the LDD structure becomes more important.
Figure 2 gives the transfer characteristics of the d-mode device for three temperatures in the range 120K<T<300K. It should be noted that the sensitivity of the Si/SiGe device to temperature variations is similar to Si MOSFET characteristics [8] in this temperature range.
As temperature decreases from 300K to 120K, the absolute value of the threshold-voltage ($|V_T|$) decreases and the carrier mobility ($\mu(T)$) increases. From the measurements we notice that for 300K < T < 120K the increase in $\mu(T)$ is far more important than the shift in V_T, changes in $V_T(T)$ in this T-range being small for Si:SiGe MODFETs because the value of V_T is determined mainly by the doping density in the supply layer (SL) and freeze-out of carriers in this layer happens below 100K.

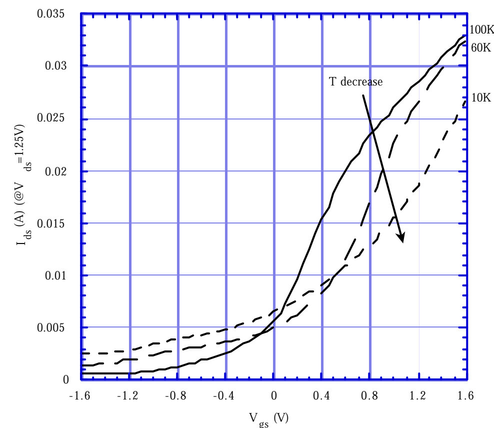

Figure 3: Source-drain current as a function of gate voltage for 3 temperatures: 100K, 60K and 10K.

As we reduce the temperature, we can notice a reversal of these characteristics within a lower temperature range 10K<T<120K (see Figure 3).
Due to carrier freeze-out in the supply layer at temperatures below 100K, V_T shifts more rapidly with T and becomes positive (as it will be shown below, Figure 6) implying a decrease in drain current.
The change of the mobility of the carriers is more complicated for lower temperatures. The temperature at which the mobility decreases due to impurity scattering is dependent on the doping concentration in the layers. In the highly doped supply layer the mobility of the carriers at lower temperatures is limited by impurity scattering, whereas in the quantum well channel of the MODFETs the carrier mobility increases further with decreasing temperatures since it is virtually undoped. Due to the residual impurities in the quantum well and neutral

impurities, the mobility increase in the QW as a function of T is limited. Moreover, the freeze-out of carriers in the supply reduces the carrier concentration in the supply more rapidly than the confined carriers concentration in the QWC, thus strongly modifying the relative carrier concentration in both layers as T decreases.

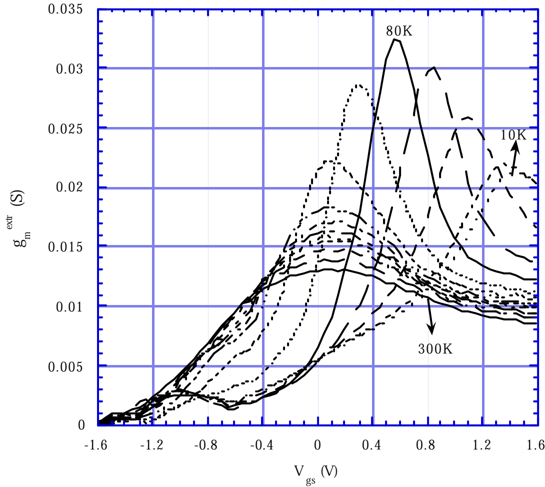

Figure 4: The extrinsic transconductance as a function of gate voltage over a wide temperature range going from 300 to 10K

All the above factors eventually lead to the existence of a temperature (above 77K) in the 10K<T<120K range at which we find optimal operation conditions of the Si/SiGe MOSFET. This is clearly illustrated in Figure 4.
Figure 4 gives the variation of the transconductance in the saturation regime of the MODFET as a function of gate voltage and temperature.
We can notice the shift in voltage position of the maximum transconductance which is related to the shift in V_T. The maximum transconductance in the MODFETs is determined by the weighted sum of the products n.μ in all parallel conducting layers (where n is the amount of carriers in the layer). Any leakage currents through gate and substrate can be neglected, since at high drain-source bias (V_{DS}=1.25V) those currents are measured to be negligible. At the point of maximum transconductance the product n.μ(T) is larger in the QWC than in the supply and setback layers, due to the larger mobility of the carriers in the QWC and the more rapid reduction of n in the SL than in the QWC as a function of temperature and gate voltage in agreement with Medici simulations.
Extra peaking of the transconductance at high negative gate voltages at low temperatures occurs and might be initially attributed to the existence of lower lying energy levels in the QWC as a result of the increased confinement at low temperatures.
The variation of the maximum transconductance of the device as a function of temperature is given in Figure 5.

The output resistance (R_{ds}) of the MODFET in strong gate overdrive and in saturation (V_{gs}=1.75V, V_{ds}=1.25V) is also plotted.

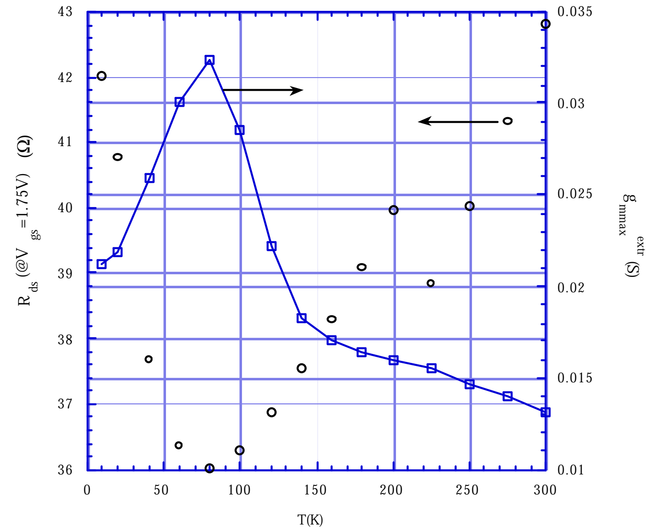

Figure 5: The maximum extrinsic transconductance (g_m^{max}) of the d-mode device and the output resistance as a function of temperature.

Fig.5 shows an optimal operation temperature of the MODFET of 80K where the maximum transconductance is 2.5 times larger than at 300K. The T dependency of g_m^{max} is different from Si MOSFET devices in the sense that for SiGe MODFETs a super-linear increase of the maximum transconductance with decreasing temperature occurs when the QWC becomes the main conduction path while g_m^{max} increases almost linearly for Si MOSFETs [9]. The peaking of the g_m^{max} characteristics is due to the existence of the QWC in Si:SiGe MODFETs. The rapid decrease of transconductance below 80K is caused by the freeze-out of carriers in the LDD structure, which increases the access resistance to the QWC. Improved performance as a function of T can be expected for Si:SiGe MODFETs with less impurities in the QWC and less parallel conduction.
The variation of the R_{ds} as a function of temperature demonstrates the influence of freeze-out of supply layer and LDD layers. The decrease of R_{ds} above 80K is due to the increase of the mobility in the conducting layer, while below 80K the mobility in the QW is still increasing but saturating, while the carrier density in the LDD is decreasing more rapidly, implying a faster increase in R_{ds} than the decrease due to g_m^{max}.
Since in a d-mode device there are sufficient carriers in the QWC at low temperatures to make a contact with the HDD structure, the transconductance remains higher at low temperature than at 300K because the increased carrier mobility in the quantum well more than equals out the increased access resistance. This can be clearly

seen by comparing these measurements to the measurements on the e-mode device of the same geometry [10].

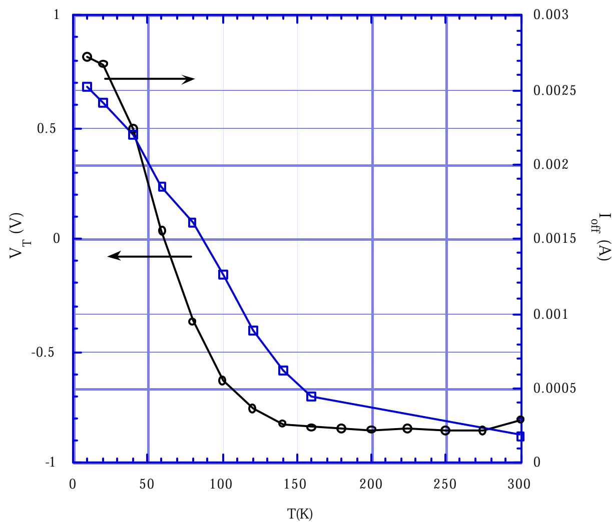

Figure 6: Variation of the threshold voltage and the off current as a function of temperature.

Off-currents in the devices are high due to the poor isolation characteristics of the pn junction to the substrate. This leakage current through the substrate is caused by the dislocations in the VS and the necessity of defining the pn junction in the SiGe close to the device layers to prevent parallel conduction in the background doped layer underneath the QWC. In Figure 6 we notice that the off-current of the device is constant over a wide temperature range (300K to 120K), while a rapid increase happens below 100K. Measurements show a decrease of the substrate leakage currents as a function of temperature, implying that the leakage current is not governed by impact ionisation like in Si MOSFETs but by conduction through the dislocations in the VS. The increase of the off-currents at low temperature can be attributed to punch-through problems similar to short channel effects. Optimisation of the layer structure can be done to reduce this punch-through effect. This, together with an increased quality of the VS and a decrease of impurity concentration in the QWC, would increase the transconductance improvement at low temperature with a factor larger than the reported in this work 2.5.

3. Conclusions

We have studied depletion mode Si/SiGe MOSFETs over a wide temperature range (10K to 300K) and demonstrated large improvements in the DC characteristics of the device at temperatures above 77K, making low T operation of these devices economically feasible. The maximum transconductance shows a peak at 80K which is associated with improved conduction happening mainly in the quantum well and the freeze-out of the LDD structure. D-mode devices show improved transconductance below the LDD freeze-out point because of the increased carrier mobility in the quantum well up to low temperatures. A large discrepancy between Si MOSFETs and Si/SiGe MOSFETs is noticed in the temperature dependence of the maximum transconductance which shows super-linear increasing rather than a monotonic increase as for the Si MOSFETs. This is due to the existence of a quantum well channel in the Si/SiGe MODFETs which allows for mobility improvements to much lower temperatures while retaining an adequate number of carriers in comparison to the parallel conducting layers.

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