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UNDER BUMP METALLURGY (UBM)-A TECHNOLOGY REVIEW FOR FLIP CHIP PACKAGING

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ABSTRACT
Flip chip packaging technology has been utilized more than 40 years ago and it still experiencing an explosives growth. This growth is driven by the need for high performance, high volume, better reliability, smaller size and lower cost of electronic consumer products. Wafer bumping is unavoidable process in flip chip packaging, thus, picking the correct bumping technology that is capable of bumping silicon wafer at high yield and a high reliability with lower cost is challenging. This paper discusses the available wafer bumping technologies for flip chip packaging. The discussion will be focused on process assembly, solder ball compatibility, design structure and lastly cost which translated to overall product costs.

Keywords: Flip chip Technology, Wafer Bumping, Flip chip packaging

INTRODUCTION

The goal of modern semiconductor packaging is to achieve shorter electron pathways for increased speed, lower power, better device functionality and lower cost. Flip chip is proving itself to meet these demands. Flip chip is not a new technology that has just recently come in the market. The first flip chip was introduced by IBM in the late 1960's is known as Controlled Collapse Chip Connection (C4) [1, 2]. This collapsible technology was limited to typical higher temperature solder utilizing high solder leads (97Pb/Sn and 95Pb/Sn) that were joined to ceramic package.

With the rapid growth in the flip chip market, the technology has gone through several revolutions, from the ceramic to plastic package, from the high leads to eutectic 63Sn/Pb and nowadays, leaded free [3]. However, the major driven factor is still cost reduction in electronic consumer product that directly related to flip chip package.

Flip chip fabrication process involved of several sequential steps: wafer bumping, attaching the bump die to the board or substrate and then completing the assembly with an adhesive underfill. In wafer bumping, it comprised of two functional steps. The first step is to create a solderable metal surface for each of the input/output (I/O) that serve as an interface between the I/O pad and the solder bump known as under bump metallurgy (UBM). The UBM is also known as multilayer thin film between aluminum bond (I/O) pad, passivation and solder bump as shown in Fig. 1. It can be deposited through evaporated, sputtered, electroplated or electroless techniques [4-6]. The second step is deposition of solder ball of which provides for both mechanical and electrical connection between the die and the substrate. Among of these techniques, electroless nickel immersion gold (ENiG) under bump metallurgy was rigorously studied because it can provide lower cost and Pb-Free solutions [4 - 11].

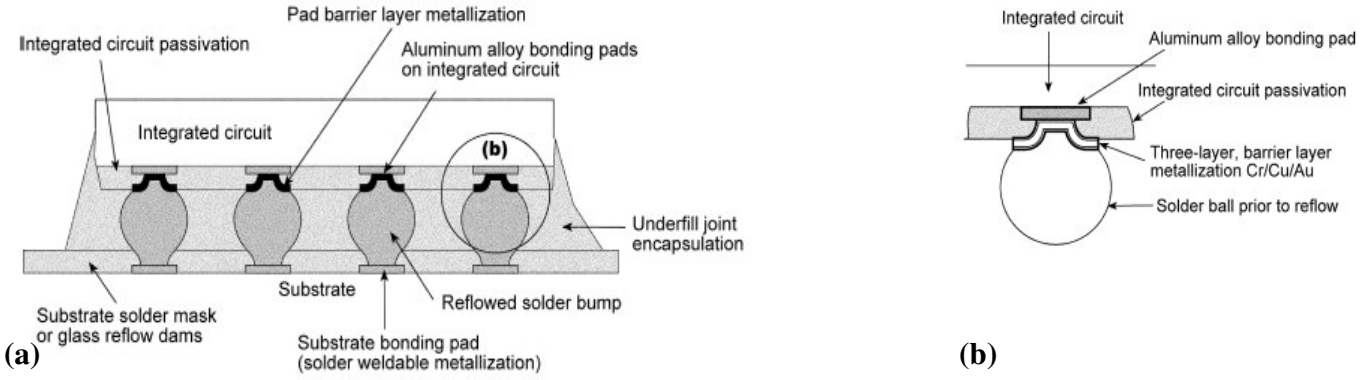

Fig. 1. Schematic diagram of (a) flip chip package (b) Under Bump Metallurgy (UBM)

In the flip chip package, under bump metallurgy (UBM) plays important factors in determine the solder ball compatibility and cost. This paper reviews each of the UBM deposition technologies in meeting the market demands.

Under Bump Metallurgy (UBM) Deposition

i. Evaporated UBM and Solder Bump

Evaporated UBM and solder bump were introduced by IBM for ceramic packages utilizing Cr/Cr-Cu/Cu/Au or TiW/Cu/Au as under bump metallurgy (UBM) [12, 13]. A schematic representation of an evaporated UBM and solder bump is shown in Fig. 2.

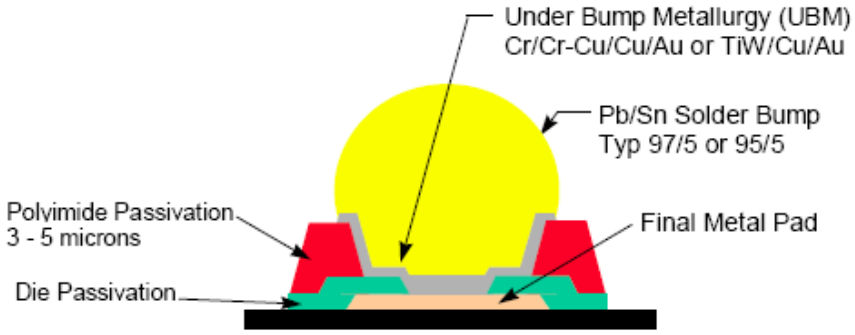

Fig. 2. Schematic cross-section of evaporated UBM and solder bump [12]

Evaporation deposition technology start with cleaning process is performed to remove oxides or photoresist prior to metal deposition. The cleaning also serves to roughen the wafer passivation and surface of the bond pad in order to promote better adhesion of the UBM. Then, the chromium, chrominum/copper, copper and Au layer are deposited through sequential evaporation process to form a multilayer thin film UBM. After that a high lead solder is then evaporated on top of the UBM to form a thick deposit of 97Pb/Sn or 95Pb/Sn. Both UBM and solder bump deposition involved of lithography and masking processes. Lithography is very expensive in term of capital expenditures [14], thus it not suitable for low cost solution. The explained process is illustrated in Fig. 3.

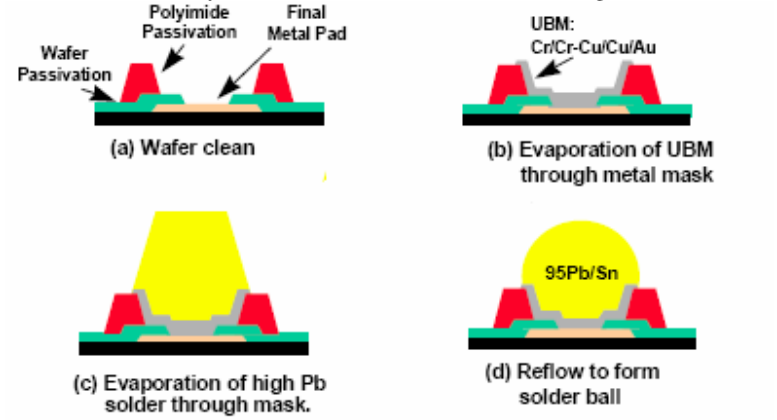

Fig. 3: Evaporation UBM and solder bumping process.

Due to low vapor pressure, the eutectic Pb/Sn solder cannot be evaporated and made this process only suitable for high lead. The high lead solder material is ductile and allows the solder bump 'collapsible' only upon exposure at high temperature (above 300° C) and makes it unsuitable for plastic or organic package. Then, the modification is made as 'Evaporated, Extended Eutectic' (E3) [12,14] whereby a layer of tin deposited separately prior to reflow process as illustrated in Fig. 4 (a) [12]. The tin layer allows the structure melt below the melting point of high lead solder. Alternatively, the eutectic solder is applied to the board as illustrate in Fig. 4 (b) [12]. This method is widely used in packaging of Intel Microprocessor dice [9]. Both methods incur additional cost because of additional process steps as compared to other method. It also leaves away the special feature of 'controlled

collapse' resulting planarization issue and the bump is not self-aligned [11, 14].

The process is expensive in terms of licensing fees, capital expenditures for equipment and materials. Throughput is limited with the process, averaging between 10-12 wafers per hour for 8 inch wafer and the not economically scaleable to larger wafer size [14].

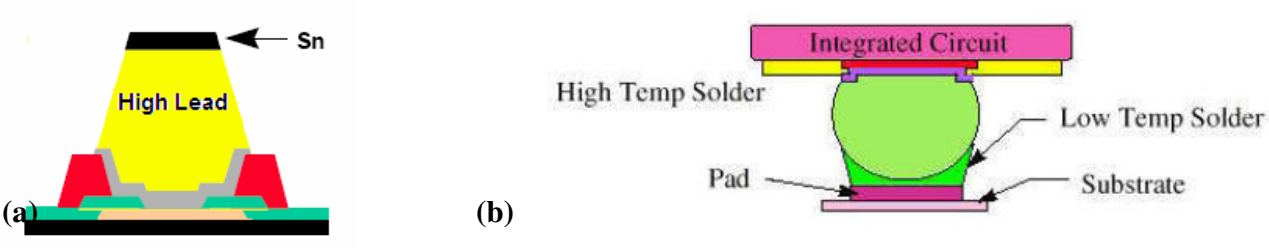

Fig. 4: (a) Deposition of Sn layer on top of high lead solder (b) High temperature solder joined to non-ceramic substrate [12, 15]

ii. Electroplated UBM and Solder Bump

Electroplating UBM process was developed is an alternative to the evaporation because of it lower equipment costs. It utilizes several materials plating process. The traditional plating processes for solder bump is adopted from the evaporated process and uses a Cr/Cr-Cu/Cu UBM with a high lead solder (3-5% Sn content). Another process, that is more accepted for eutectic 63Sn/Pb solder is involved of titanium/tungsten (TiW) layer followed by a thick solder wettable layer such as copper (Cu). This thick copper layer is sometimes called a 'minibump' or 'stud'. A schematic representation of this process is shown in Fig. 5.

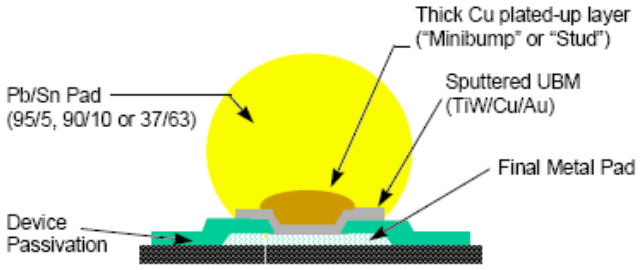

Fig. 5: (a) Electroplated thick Cu ('minibump' or 'stud') and solder bump [13]

In this technology, the process starts with cleaning the wafer to remove oxides or organic residue prior to metal deposition. As in evaporated approach, the cleaning roughens the wafer passivation and bond pad surface to promote better adhesion of the UBM. The multilayer UBM that consist of TiW, Cu and Au are then sequentially sputtered over the entire wafer. The UBM adheres to the wafer passivation layer as well as to the bond pads. For the creation of the minibump structure, the copper layer is plated over the bond pad to a height as determined by pattern photoresist. Fig. 6 illustrates the complete electroplated UBM and solders bump deposition process flow.

After the completion of UBM deposition, a second mask is used to form plated solder bump. The photoresist is stripped after the bump is formed, leaving the UBM exposed on the wafer as shown in Fig. 5(e). The UBM is removed in one of two ways. In the first approach, a wet etch is used and the UBM is removed from the wafer with some undercutting around the UBM. The solder is then reflowed into sphere. In the second approach, the solder bumps are first reflowed, with the aim that any intermetallics formed within the bump structure will protect the bump by minimizing undercutting during the subsequent etching process as shown in Fig. 6 (e) and (f).

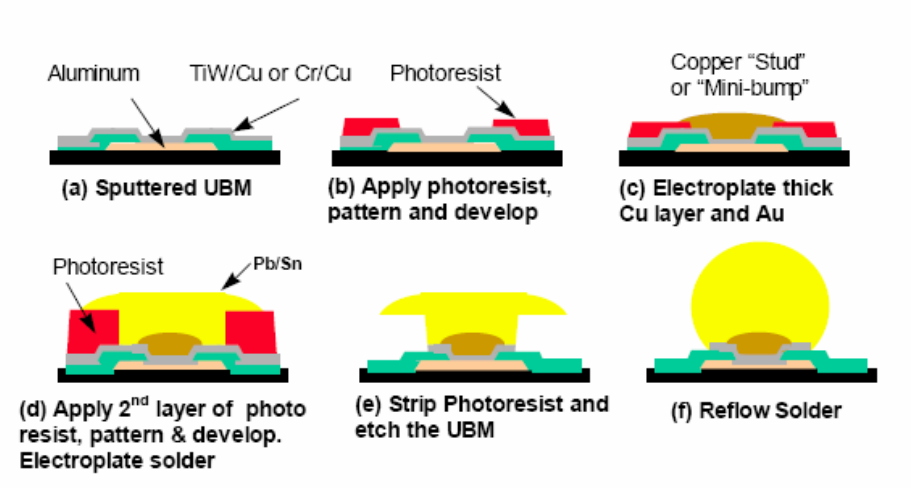

Fig. 6 : Electroplated UBM and solder bump process flow.

The use of the UBM/minibump structure enables the application of high leads and eutectic 63Sn/Pb solder bump [14]**.** However for eutectic solder bumps it has limited thermal cycle.

Electroplating is typically less expensive than evaporated wafer bumping. However, the major drawback is uneven bump uniformity that is due to non-uniform current density distribution, the electric field between the anode plate and the wafer, and the plating solution flow. The thick copper minibump that develops during electroplating induced unnecessary excessive stress to the silicon underneath that lead to cratering problem [14, 16]. The thick Cu creates the brittle Cu/Sn intermetallic after multiple reflow operations when the Cu consumed by the Sn. If the Sn were to consume the Cu minibump, it would fall back onto the non-wettable and de-wet from the UBM [14].

iii. Sputtered UBM and Printed Solder Paste Bumping

The formation of sputtered UBM and printed solder paste bumping was developed by Delco in 1970 [5]. In this technology, the process starts with cleaning to remove oxides or organic residue prior to metal deposition. As evaporated and electroplated, the cleaning serves to roughen the bond pad and wafer passivation to promote better adhesion of the UBM. Then, the Al is sputtered, followed by sputtered of Ni and Cu. The Al forms a strong adhesion to the wafer passivation as well as to the Al bond pads. The Cu is used to keep the Ni from oxidizing and unlike the plated minibump process; it not needed to allow the solder bump to adhere to the UBM. The Cu layer will be consumed into eutectic solder during the reflow. The Ni serves as dual-function, to provide solder diffusion layer and also solder wettable surface after the Cu layer consumed.

After that a layer of photoresist is applied, patterned and developed. The Al/Ni/Cu layers are then etched away except the bond pad opening. The resist is removed, leaving the multilayer UBM on the bond pad. Lastly, solder paste is printed onto the UBM and followed by reflow to form a sphere solder ball. Fig. 7 (a) to (e) illustrates the steps of these processes.

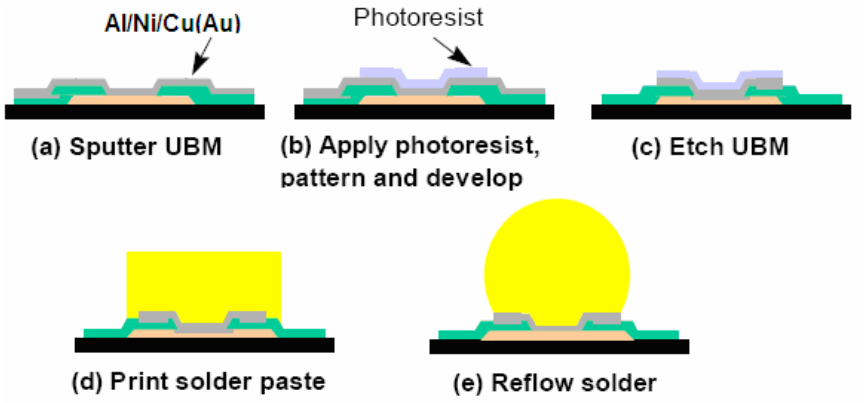

Fig. 7: Sputtered UBM and Printed Solder Paste Bumping [18]

The cost of bumping process is less expensive than evaporated and competitive with electroplated bumping technology. Unlike evaporated, no additional costs that are incurred at the board level because the UBM composition is compatible with eutectic 63Sn/Pb solder [12, 14]. The eutectic 63Sn/Pb solder bump is robust enough as compared to electroplated technology and be able to withstand more than 10 reflow cycles. It also reported compatible with lead free solder alloys Cu/Sb/Ag/Sn [13, 14]. The deposited solder bump can experience a 10-30% collapse upon assembly [14]. This feature provides robust assembly process with high yield.

iv. Electroless UBM

The previous wafer bumping technology does not fulfill the requirements for low cost products because it involved lithography process. The electroless deposition revealed as a promising technology to meet the low cost solution. Electroless bumping process is the selective autocatalytic metal deposition on activated Al pads without any costly equipment such as plating base and lithography. The nickel, cobalt, palladium, platinum copper, silver and variety of alloys involving one of more of these metals can be deposited with this technology [7]. Among these, electroless nickel and copper seem to be the most established deposition solution [7-9]. Fig. 8 shows the schematic diagram of electroless UBM.

Electroless nickel bump is unique, because it acts as UBM that can be used as a foundation for solder bump or with slight thickness increase it acts as a stand alone minibump that can be used with conductive adhesives. This can be achieved because electroless nickel is isotropic [10], the bumps grew evenly in all directions, and when above the passivation level, spread over it, sealing the bond pads

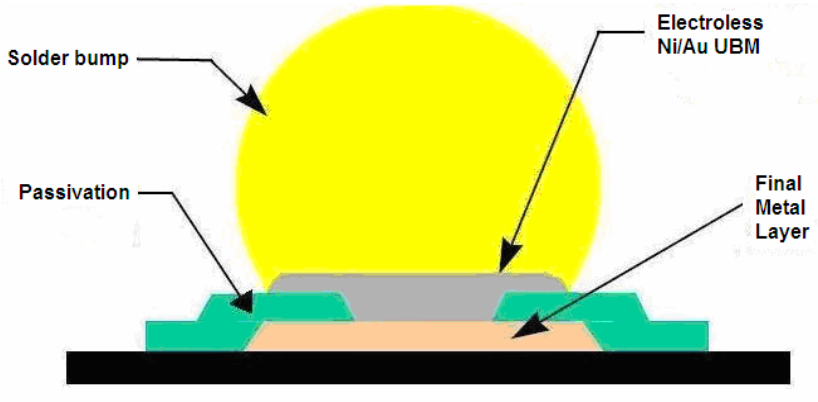

Fig. 8: Electroless UBM and solder bump [12, 17]

In electroless nickel bumping, the process starts with the wafer back side coating to prevent from nickel plated on the exposed silicon. The following next is cleaning process, used to remove contaminant on the passivation and Al bond pad. A second cleaning process is then applied to removes thick Al oxides and prepares the surface for metal deposition.

After that is the zincation process. It activates the Al bond pads surface for Ni deposition. A thin zinc layer is deposited on Al which is substitutes by Ni in the Ni bath. Finally, a thin gold layer is deposited on the Ni from an immersion gold bath to prevent the oxidation of Ni before soldering and also help to improve solderability with solder ball. Fig. 9 shows the sequence of the Ni bumping process of electroless nickel UBM. During the process the chemical baths must be well understood and controlled to avoid uneven or no plating

The major advantage of electroless Ni is, it compatible with a wide variety of solder ball, such as high lead (90Pb/10Sn), eutectic solder (63Sn/37Pb), leads free (95.5Sn/3.8Ag/0.7Cu) [11] and conductive adhesive [14]. The drawback is corrosion issues because the electroless UBM only adheres to bond pad and not at the passivation [14,17].

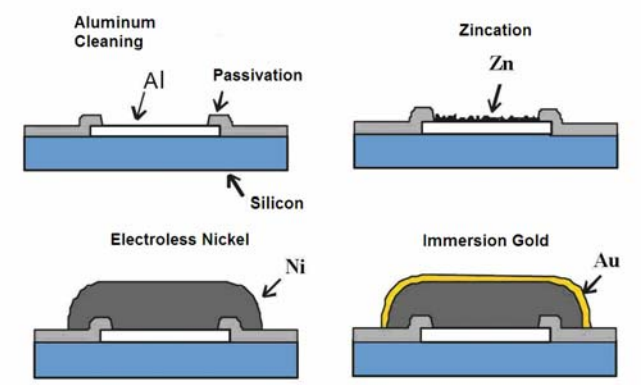

Fig. 9 : The schematic of electroless nickel bumping process [8, 11]

Summary

Table 1 shows the summary for each deposition technique as discussed previously. Each process has it own advantages and disadvantages; however costs, high throughput and flexibility would be a major driven factor in today industry, thus electroless deposition emerge as a viable process in the near future.

Table 1: Summary of the deposition techniques.

UBM Deposition Process Technology	**Solder ball compatibility**	**Process costs**	**Design Structure**
Evaporation	High lead 97Pb/Sn or 95Pb/Sn	Expensive – involved photolithography process	Fully 'collapsible' during reflow. Alignment accuracy is good.
Electroplated	High lead and eutectic SnPb (63Sn/Pb)	Typically less expensive than evaporated wafer bumping	Brittle Cu/Sn intermetallic and non-wettable surface of UBM
Sputtering	Compatible with eutectic 63Sn/Pb and leaf free Cu/Sb/Ag/Sn	Competitive with electroplated	Robust assembly, almost provide 'collapsible' bump during reflow.
Electroless	Compatible with high lead (90Pb/Sn), eutectic (63Sn/Pb) and lead free (95.5Sn/3.8Ag/0.7Cu)	Lower cost because eliminates photolithography process. The process is parallel and scaleable to larger wafer size.	The UBM only adheres to bond pad and not the passivation. Corrosion can be an issue.

CONCLUSION

Each of the wafer bumping has been discussed. The bumping of silicon wafer requires a bump technology that is extremely reliable and robust in it bumping yield and also a wide range of solder ball compatibility with cost will be the main driven factor. Thus electroless deposition technology will keep growing as the growth of flip chip packaging technology.

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