View metadata, citation and similar papers at core.ac.uk

brought to you by CORE

provided by CiteSeerX

Microelectronics Reliability 52 (2012) 628–634

Contents lists available at SciVerse ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel

Review

Emerging memory technologies: Trends, challenges, and modeling methods

A. Makarov *, V. Sverdlov, S. Selberherr

Institute for Microelectronics, TU Wien, Gußhausstraße 27-29, A-1040 Vienna, Austria

ARTICLE INFO

Article history:
Received 19 October 2011
Accepted 20 October 2011
Available online 16 November 2011

ABSTRACT

In this paper we analyze the possibility of creating a universal non-volatile memory in a near future. Unlike DRAM and flash memories a new universal memory should not require electric charge storing, but alternative principles of information storage. For the successful application a new universal memory must also exhibit low operating voltages, low power consumption, high operation speed, long retention time, high endurance, and a simple structure. Several alternative principles of information storage are reviewed. We discuss different memory technologies based on these principles, highlight the most promising candidates for future universal memory, make an overview of the current state-of-the-art of these technologies, and outline future trends and possible challenges by modeling the switching process.

© 2011 Elsevier Ltd. All rights reserved.

Contents

1. Introduction . . . 628
2. DRAM technology . . . 629
   2.1. ZRAM . . . 629
3. Resistive change based memory . . . 629
   3.1. CBRAM, PCRAM, and RRAM . . . 630
   3.2. Monte Carlo modeling of RRAM . . . 630
4. Magnetic memory technology . . . 631
   4.1. MRAM and STT-MRAM . . . 631
   4.2. Penta-layer STT-MRAM modeling . . . 631
5. Conclusions . . . 633
   Acknowledgement . . . 633
   References . . . 633

1. Introduction

In modern microelectronic devices the dominant memory types are DRAM, static RAM, and flash memory. These types of memory store data as a charge state. For many decades these memory technologies have been successfully scaled down to achieve higher speed and increased density of memory chips at lower bit cost [1]. However, memories based on charge storage are gradually approaching the physical limits of scalability and conceptually new types of memories based on a different storage principle are gaining momentum. Apart from good scalability a new type of memory must also exhibit low operating voltages, low power consumption, high operation speed, long retention time, high endurance, and a simple structure [2]. In addition, non-volatility is highly desirable to preserve the data when the power is off.

Alternative principles of information storage include the resistive switching phenomenon in insulators, the effect of changing the magnetoresistance, the domain wall motion along magnetic racetracks, the ferroelectric effect, and others. Some of the technologies based on these new storage principle are already available as product (such as phase change RAM (PCRAM), magnetoresistive RAM (MRAM), and ferroelectric RAM (FeRAM)), others only as prototype (such as carbon nanotube RAM (CNRAM), copper bridge RAM (CBRAM), spin-torque transfer RAM (STTRAM, STT-MRAM),

* Corresponding author.
E-mail address: makarov@iue.tuwien.ac.at (A. Makarov).

0026-2714/$ - see front matter © 2011 Elsevier Ltd. All rights reserved.
doi:10.1016/j.microrel.2011.10.020

and resistive RAM (RRAM)), while racetrack memory is available only as a memory concept.

From these technologies two of the most promising candidates for future universal memory are STTRAM and Redox Resistive RAM. Currently, STTRAM, RRAM and CBRAM have been demonstrated on 64 Mb [3], 4 Mb [4,5] test chips, respectively. These technologies would be manufacturable within 5–10 years [6].

First we briefly review the nearest future of DRAM technology, including ZRAM as a potential replacement of DRAM. Then we outline the possibility of creating a universal non-volatile memory based on resistance change and spin, the current state of these technologies, trends and challenges, and demonstrate modeling approaches.

2. DRAM technology

Although a new cell structure for DRAM has been developed by industry to overcome the scaling challenges at 30 nm, future size reduction below 20 nm is facing physical limitations and a process complexity resulting in high manufacturing cost. DRAM with vertical gate type transistors was introduced in order to resolve the critical scaling problems, but it is not easy to reduce the size of the cell capacitance for the 20 nm technology node [1]. A DRAM memory cell based on a transistor alone technology could solve this problem. The ultimate advantage of this new concept is that it does not require a capacitor, and, in contrast to traditional 1T/1C DRAM cells, it thus represents a 1T/0C cell name ZRAM (zero-capacitance RAM).

2.1. ZRAM

The concept of a DRAM memory cell based on a transistor alone was introduced already a decade ago [7–14]. The functionality of the first generation ZRAM is based on the possibility to store majority carriers in the floating body. The carriers are generated by impact ionization caused by the minority carriers close to the drain. The threshold voltage is modified because of the charge accumulated in the body thus guaranteeing the two states of a MOSFET channel, open and close, for a gate voltage chosen between the two thresholds.

The idea of the second generation ZRAM is to exploit the properties of the bipolar transistor [15], allowing to expand the ZRAM applicability to such advanced non-planar devices as FinFETs, multi-gate FETs and gate-all-around FETs. Contrary to the first generation, the current is flowing through the body of the structure. This increases the value of current by roughly the ratio of the fin radius to the surface layer thickness. The majority carriers are generated due to impact ionization. They are stored under the gate at the silicon/silicon dioxide interface. The stored charge provides good control over the bipolar current, in contrast to the first generation ZRAM, where the charge is stored in the area close to the buried oxide.

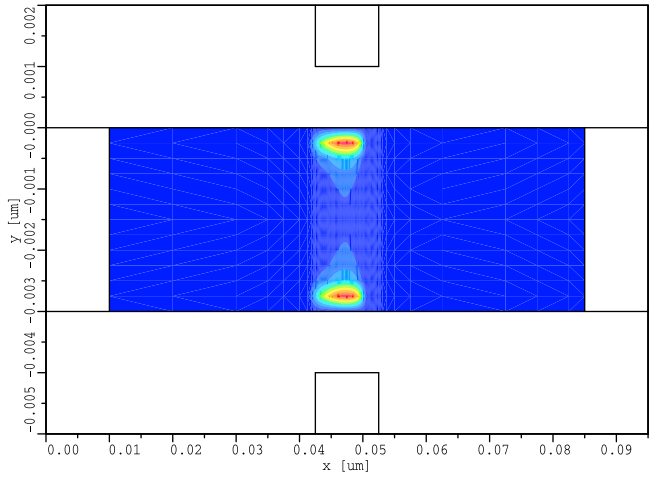

Fig. 1. Contour plot of the hole distribution in a 12.5 nm long MOSFET channel for the high current state. Close to the gates the hole concentration is high. Due to quantum effect, the centroid of the hole concentration is at a certain distance from the gates.

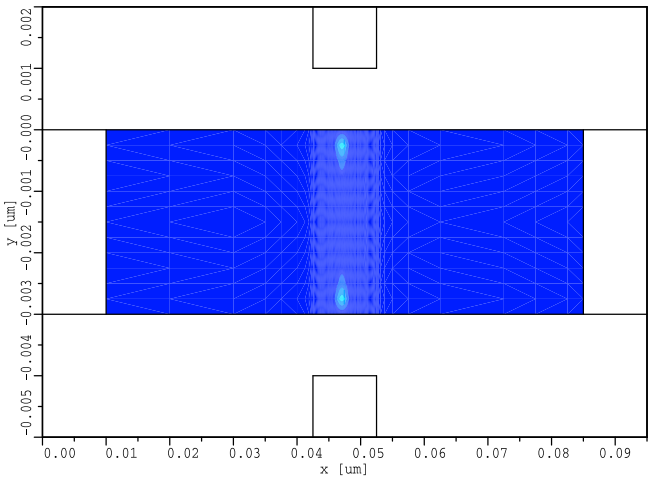

Fig. 2. Contour plot of the hole distribution in a 12.5 nm long MOSFET channel for the low current state. The concentration is appropriately small. Due to quantum effect, the centroid of the hole concentration is also in the low current state at a certain distance from the gates.

In [17] it is demonstrated that the programming window, which is formed by the two current values and the two gate voltage values when switching appears, is sufficiently large for stable ZRAM operation on 50 nm double-gate transistors. Simulations of a double-gate structure with the gate length as short as 12.5 nm gate were also performed. Excess hole concentrations in the open and close states corresponding to the large and low values of the current are shown in Figs. 1 and 2, respectively.

While keeping all advantages of the first ZRAM generation, the most recent generation of ZRAM cells [15] is characterized by a significantly enlarged programming window and much longer retention times. Recently, a 128 Mb floating body RAM was designed and developed [14].

The use of vertical gate-all around transistors extends the ZRAM roadmap to future generations. One disadvantage of the ZRAM cell is the relatively high operating voltage needed to ignite impact ionization. To reduce the operating voltage, a new concept of a 1T/0C cell was recently proposed [16].

3. Resistive change based memory

Resistive change memory possesses the simplest structure in the form of metal–insulator–metal (MIM). The electrical conductance of the insulator can be set at different levels by the application of an electric field and this phenomenon can be used in memory devices. The state with high resistance (HRS) can mean logical 1 and the state with low resistance (LRS) can mean logical 0, or vice versa depending on the technology. The resistive switching phenomenon is either bipolar or unipolar, based on the polarity of the SET and RESET processes. The switching operation is called bipolar, when the SET to LRS occurs at one voltage polarity and the RESET to the HRS on the reversed voltage polarity. The switching operation is called unipolar, when the switching procedure does not depend on the polarity of the write voltage.

Resistive switching phenomena is observed in different types of insulators, such as metal oxides, perovskite oxides, chalcogenide materials and others. Three technologies of memory, CBRAM, PCRAM, and RRAM, are based on the resistive switching.

3.1. CBRAM, PCRAM, and RRAM

CBRAM, also called in the literature as memory with an Electrochemical Metallization (ECM) cell or a Programmable Metallization Cell (PMC), is based on solid state electrolyte in which mobile metal ions can create a conductive bridge between the two electrodes under the influence of an electric field. The source of mobile metal ions is one of the electrodes, which is made from an electrochemically active metal, such as Ag, Cu, or Ni. Electrochemically inert metals, such as Pt, Ir, W, or Au are used for the second electrode [18].

PCRAM employs the difference in resistivity between crystalline and amorphous phases of a chalcogenide compound [19].

RRAM is based on metal oxides, such as NiO [20], Cu_xO [21], TiO_x [22–25], HfO_2 [26], ZnO [27], WO_x [28], on the heterostructure of metal oxides, such as AlO_x/TiO_x [29], and perovskite oxides, such as doped $SrTiO_3$ [30], $Pr_{1-x}Ca_xMnO_3$ [31], doped $SrZrO_3$ [32].

The concepts of RRAM shown by NDL [28] and Samsung [29] have already surpassed the scaling limit of charge-based storage memories [33]. Despite this, a proper fundamental understanding of the RRAM switching mechanism is still missing, hindering further development of this type of memory. First and foremost, one needs a better understanding and control of physical SET/RESET processes through development of accurate models [6].

In the literature several physical mechanisms/models based on either electron or ion switching have been suggested for the explanation of resistive switching in perovskite oxides [34–38], in metal oxides with bipolar [37,39–42] and unipolar behavior [43], and metal oxides with heterostructure [44]. Because bipolar switching shows a higher potential to implement a cost-effective multi-stacking cell as well as more stable cell operation [1], we briefly discuss modeling approaches to bipolar oxide based RRAM.

3.2. Monte Carlo modeling of RRAM

One of the first models of resistive switching proposed was a domain based model [39]. The insulating medium contains metallic domains, which inexplicitly correspond to charge traps in the real system such as dopants, vacancies, metallic clusters, and nanodomains. It is assumed in this model that there are just three types of domain. The top and bottom domains are taken to be smaller than the middle one. This differentiation might be justified by the different electronic states close to the interfaces of the metal electrodes. Electrons move around by hopping between domains as well as between a domain and an electrode only, when there an external voltage is applied. Resistive switching is explained on the basis of the filling and desolating these domains.

In [40] the resistive switching behavior is associated with the formation and rupture of a conductive filament (CF). The CF is formed by localized oxygen vacancies V_o. The conduction is due to electron hopping between these V_o. Rupture of a CF is due to a redox reaction in the oxide layer under a voltage bias (Fig. 3). In [40] the system in LRS is modeled: rupture of the CF is possible after a formation of a depleted region with low electron occupation.

In [41] the temperature dependence of the site occupations in the low occupation region was analyzed. The results indicate that the decrease in switching time with increasing temperature reported in [40] may stem from the increased mobility of oxide ions rather than from the reduction in occupations of V_o in the low occupation region. These results demonstrated the necessity to include the dynamics of oxygen ions. For modeling the resistive switching by Monte Carlo techniques the dynamics of oxygen ions (O^{2-}) and electrons in an oxide layer in this work was described as follows:

- formation of V_o by O^{2-} moving to an interstitial position;
- annihilation of V_o by moving O^{2-} to V_o;
- an electron hop into V_o from an electrode;
- an electron hop from V_o to an electrode;
- an electron hop between two V_o.

The hopping rates for electrons are modeled as [45]:

$$\Gamma_{nm} = A_e \cdot \frac{\Delta E}{h \cdot (1 - \exp(-\Delta E/k_b T))} \cdot \exp(-R_{nm}/a). \quad (1)$$

Here, h is the Planck constant, A_e is a dimensionless coefficient, ΔE is the difference between the energies of an electron positioned at sites n and m, R_{nm} is the hopping distance, a is the localization radius, T is the temperature, k_b is the Boltzmann constant.

To describe the motion of ions the ion rates are chosen similar to (1):

$$\Gamma'_n = A_i \cdot \frac{\Delta E}{h \cdot (1 - \exp(-\Delta E/K_b T))}. \quad (2)$$

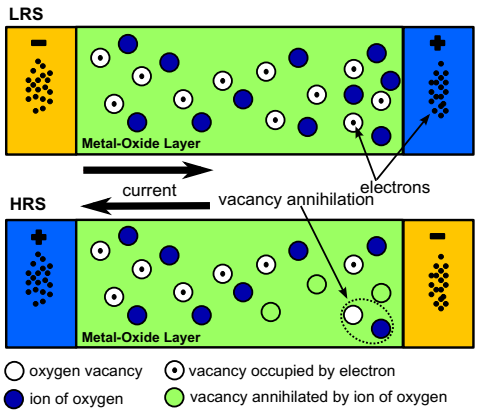

Fig. 3. Schematic illustration of the conducting filament in the low resistance state (top) and the high resistance state (bottom).

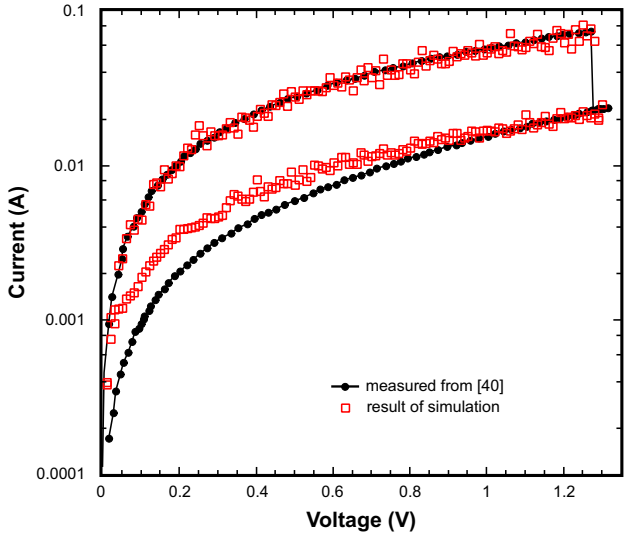

Fig. 4. Current–voltage curves during the reset process. The lines are measured result from [40]. The symbols are obtained from the model [41].

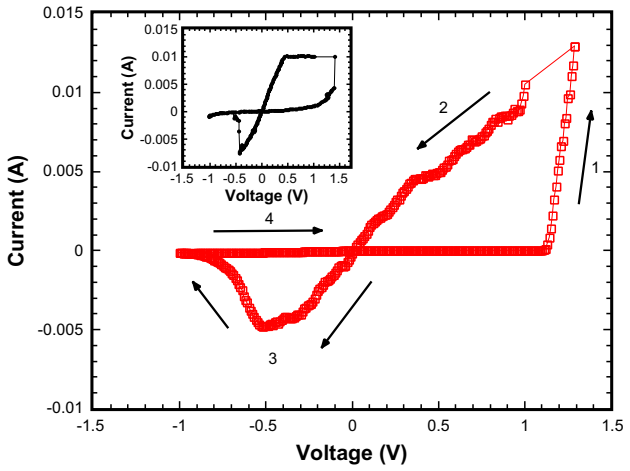

Fig. 5. I–V characteristics showing the hysteresis cycle obtained from the model [41]. The inset shows the hysteresis cycle for M–ZnO–M from [27].

Because moving of an ion is allowed only at the nearest sites, a distance-dependent term is incorporated in A_i. ΔE includes the formation energy for the mth V_o/annihilation energy of the mth V_o, when O^{2-} is moving to an interstitial or back to V_o, respectively.

Results of simulations obtained with the model [41] are shown in Figs. 4 and 5. Fig. 4 shows the RESET process for a single CF, which is in good agreement with the measurements from [40].

Fig. 5 shows the RRAM switching hysteresis cycle. The simulated cycle is in agreement with the experimental cycle from [27] shown in the inset of Fig. 5. The interpretation of the RRAM hysteresis cycle obtained from the stochastic model is as follows. If a positive voltage is applied, the formation of a CF begins, when the voltage reaches a critical value sufficient to create V_o by moving O^{2-} to an interstitial position. The formation of the CF leads to a sharp increase in the current (Fig. 5, Segment 1) signifying a transition to a state with low resistance. When a reverse negative voltage is then applied, the current increases linearly, until the applied voltage reaches the value at which an annihilation of V_o is triggered by means of moving O^{2-} to V_o. The CF is ruptured and the current decreases (Fig. 5, Segment 3). This is the transition to a state with high resistance.

4. Magnetic memory technology

Magnetic memory technologies include such types of memories as MRAM, STT-MRAM, and racetrack memory. Racetrack memory [46] is currently available only as a concept. We focus our attention on MRAM and STT-MRAM in the following.

4.1. MRAM and STT-MRAM

The basic element of an MRAM is a magnetic tunnel junction (MTJ), a sandwich of two magnetic layers separated by a thin nonmagnetic spacer (Fig. 6). While the magnetization of the pinned layer is fixed due to the fabrication process, the magnetization direction of the free layer can be switched between the two states parallel and anti-parallel to the fixed magnetization direction. Switching in MRAM is performed by applying a magnetic field. In contrast to field-driven MRAM, STT-MRAM does not require an external magnetic field. Switching between the two states occurs due to the spin-polarized current flowing through the MTJ. The spin-polarized current is only a fraction of the total charge current. Therefore, high current densities are required to switch the magnetization direction of the free layer. These densities are, however, one to two orders of magnitude lower than those needed for the current-induced domain wall motion in racetrack memory [46]. This makes the STT-MRAM technology attractive for applications, including recently proposed domain wall motion by the field-like component of the spin torque [47].

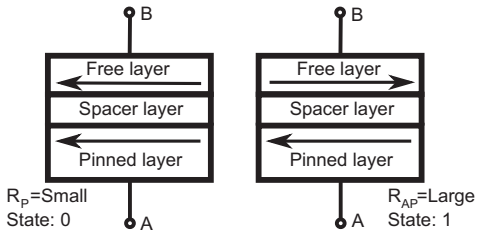

Fig. 6. Schematic illustration of the three-layer MTJ in low resistance state (left) and high resistance state (right).

Different options of MTJ are available: three-layer with in-plane magnetization of the free layer (in-plane MTJ) [48–51], in-plane penta-layer MTJ [52], three-layer MTJ with perpendicular magnetization [53]. Perpendicular MTJs with interface-induced anisotropy show good potential, but still require reducing damping and increasing thermal stability [54].

The reduction of the current density required for switching and the increase of the switching speed are the most important challenges in this area [55]. Several strategies have been proposed to decrease the switching time below a few nanoseconds: pre-charging with a bias current [56], by combining a spin-polarized current together with a small radio frequency field [57], and by applying a magnetic field perpendicular to the magnetization direction [58].

Measurements [52] showed a decrease in the critical current density for a penta-layer magnetic tunnel junction with the two pinned magnetic layers in anti-parallel configuration (Fig. 7, left) compared to the three-layer MTJ. Theoretical predictions showed a decrease of the switching time in penta-layer structures with an increase of the out-of-plane component of the magnetostatic field [59]. An even more pronounced decrease of the switching current density was recently reported in a penta-layer structure with a composite free layer (Fig. 7, right) [60].

4.2. Penta-layer STT-MRAM modeling

A penta-layer structure was investigated theoretically [61] by using the ballistic Green's Function formalism combined with the

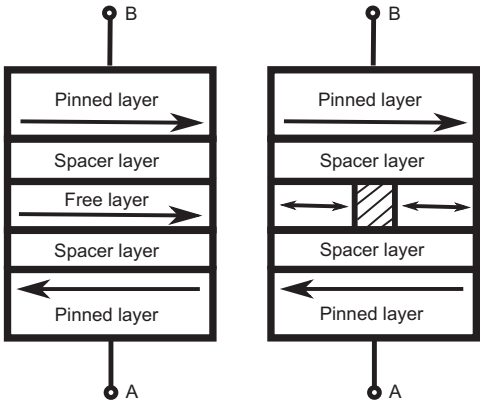

Fig. 7. Schematic illustration of the penta-layer MTJ with monolithic (left) and composite free layer (right).

soft magnetic layer dynamics based on the Landau–Lifshitz–Gilbert (LLG) equation. A spin torque enhancement was found in the anti-parallel penta-layers (the magnetizations of the two fixed layers are anti-parallel) as compared to the three-layer structure. This enhancement manifests itself only under dual barrier resonance tunneling conditions, when the current is high. At the same time, the aligned penta-layer configuration, when the magnetizations of the two fixed layers are parallel to each other, was found to have a fairly low spin torque efficiency and, as a consequence, it demands high switching currents [61]. Similar conclusions were obtained under the assumptions made in [62]. It follows that in the anti-parallel configuration of the fixed layers the spin currents from either of the pinned layers exert torques on the free magnetic layer in the same direction (full torque is the sum of the individual torques), while in the parallel configurations the torques are in opposite directions (full torque is the difference of the individual torques). The use of the model [62] is justified in structures with a free ferromagnetic layer thickness of a few nanometers. Indeed, the electron spins become aligned with the magnetization of the free layer at a distance approximately 1 nm away from the interface.

The micromagnetic simulations are based on the magnetization dynamics described by the LLG equation:

$$\frac{dm}{dt} = -\frac{\gamma}{1+\alpha^2}\cdot((m\times h_{eff}) + \alpha\cdot[m\times(m\times h_{eff})] + \frac{g\mu_B j}{e\gamma M_s d} \cdot (g_1(\Theta_1)\cdot(\alpha\cdot(m\times p_1) - [m\times(m\times p_1)]) - g_2(\Theta_2) \cdot(\alpha\cdot(m\times p_2) - [m\times(m\times p_2)]))).$$

Here γ is the gyromagnetic ratio, α is the Gilbert damping parameter, g is the gyromagnetic splitting factor, μ_B is Bohrs magneton, j is the current density, e is the electron charge, d is the thickness of the free layer, $m = M/M_s$ is the position dependent normalized vector of the magnetization in the free layer, $p_1 = M_{p1}/M_{sp1}$ and $p_2 = M_{p2}/M_{sp2}$ are the normalized magnetizations in the first and second pinned layers, respectively. M_s, M_{sp1}, and M_{sp2} are the saturation magnetizations of the free layer, the first pinned layer, and the second pinned layer, correspondingly. Slonczewski's expressions are used for the MTJ with a metal layer [63]

$$g_2(\Theta) = [-4 + (1+\eta)^3(3+cos(\Theta))/4\eta^{3/2}]^{-1}, \quad (4)$$

and with a dielectric layer [64]

$$g_1(\Theta) = 0.5\cdot\eta[1+\eta^2\cdot cos(\Theta)]^{-1} \quad (5)$$

between the ferromagnetic contacts, respectively. In the penta-layer structure the two spin torques are acting independently on the two opposite interfaces of the free ferromagnetic layer, provided its thickness is larger than the scale on which the electron spins entering into the ferromagnet become aligned to the ferromagnets' magnetization. The local effective field is calculated as:

$$h_{eff} = h_{ext} + h_{ani} + h_{exch} + h_{demag} + h_{th} + h_{amp} + h_{ms}. \quad (6)$$

Here, h_{ext} is external field, h_{ani} is anisotropic field, h_{exch} is a exchange field, h_{demag} is a demagnetizing field, h_{th} is a thermal field, h_{amp} is the Ampere field, and h_{ms} is the magnetostatic coupling between the pinned layers and the free layer.

In the uniaxial anisotropy case the anisotropic field is [65]:

$$h_{ani} = \frac{2K_1}{\mu_0 M_s}(m\cdot u)u, \quad (7)$$

while for the cubic anisotropy it is calculated as:

$$h_{ani} = -\frac{2D}{\mu_0 M_s}m. \quad (8)$$

Here, D is the diagonal matrix with entries

$$D_{11} = K_1\left(m_y^2 + m_z^2\right) + K_2 m_y^2 m_z^2, \quad (9)$$

$$D_{22} = K_1\left(m_x^2 + m_z^2\right) + K_2 m_x^2 m_z^2, \quad (10)$$

$$D_{33} = K_1\left(m_x^2 + m_y^2\right) + K_2 m_x^2 m_y^2, \quad (11)$$

K_1 and K_2 are the material-dependent anisotropy coefficients, u is the easy axis, μ_0 is the magnetic constant.

The exchange field is calculated as [65]:

$$h_{exch} = \frac{2A}{\mu_0 M_s}\sum_j((m_j - m)/|r_j|^2). \quad (12)$$

Here, A is the exchange constant.

For calculating the demagnetization field the method proposed in [66,67] is used.

The thermal field is calculated as [68]:

$$h_{th} = \sigma\cdot\sqrt{\frac{\alpha}{1+\alpha^2}\cdot\frac{2k_BT}{\gamma\Delta V\Delta t M_s}}. \quad (13)$$

Here, σ is a Gaussian random uncorrelated function, k_B is the Boltzmann constant, ΔV is the volume of cell, Δt is the time step.

The eddy currents field is [69]:

$$h_{amp,i} = \sum_{j=1\ldots N}\frac{J_j}{4\pi}\times\int_j\frac{r_i - r_j}{r^3}dv. \quad (14)$$

Here, J_j is the current induced on every cell (j:1...N).

In [60] the structure CoFe/spacer (1 nm)/Py (4 nm)/spacer (1 nm)/ CoFe (Py is $Ni_{81}Fe_{19}$) with an elliptical cross-section (major axes 90 nm and 35 nm, correspondingly) is investigated. The system with a composite ferromagnetic layer is obtained by removing a central stripe of 5 nm width from the monolithic free layer.

Fig. 8 shows a substantial decrease of the switching time in the penta-layer structure with the composite free layer for the same current density $j = 10$ MA/cm^2. The magnetostatic field h_{ms} causes the magnetization to tilt out of the x–y plane. The non-zero angle between the fixed magnetization and the magnetization in the free layer results in an enhanced spin transfer torque, when the current starts flowing. In the case of the monolithic structure, however, the torque remains marginal in the central region, where the magnetization is along the x axis. As the amplitude of the end domains precession increases, the central region experiences almost no spin

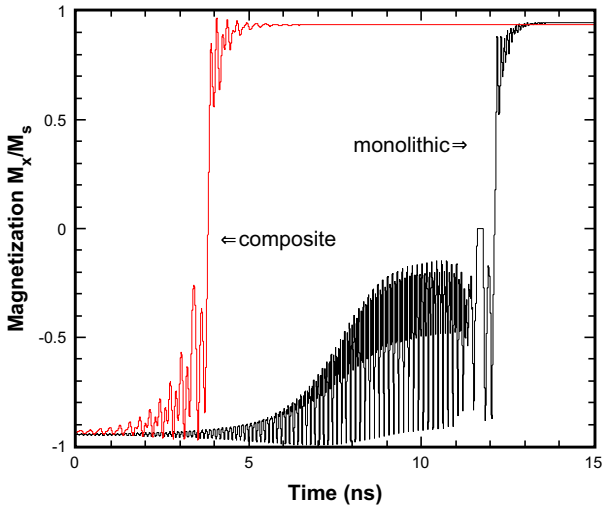

Fig. 8. The switching process for an MTJ with composite and monolithic free layer for a pinned layer thickness of 15 nm.

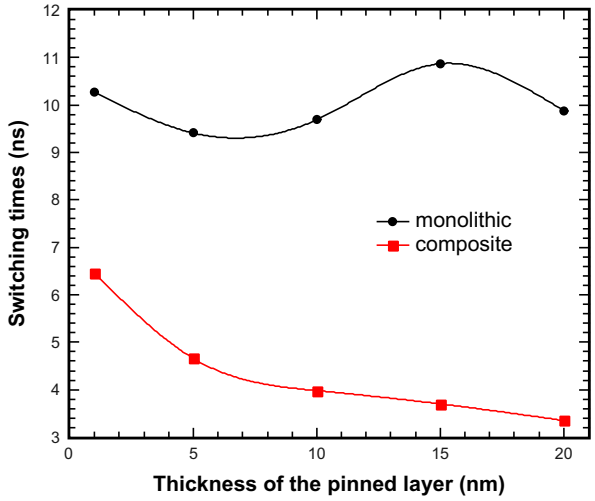

Fig. 9. The absolute values of the switching times for MTJs with monolithic and composite free layer as function of the pinned layer thickness.

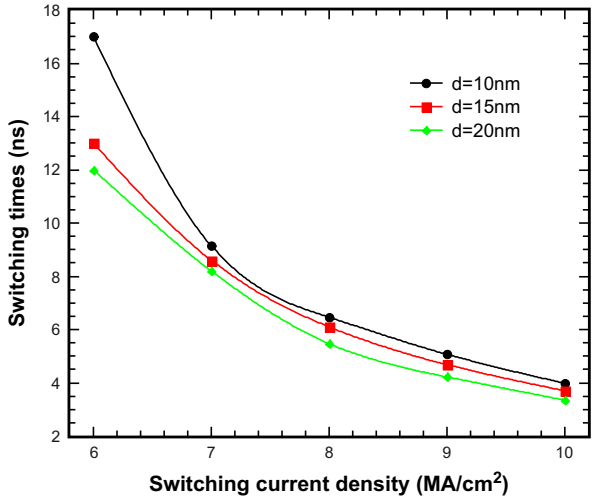

Fig. 10. The dependence of the switching times as function of the current density for the pinned layer thicknesses of 10 nm, 15 nm, and 20 nm.

torque and preserves its initial orientation along the *x* axis, thus preventing the whole layer from alternating its magnetization orientation. This is, however, not the case, when the central region is removed in the composite structure and the end domains become virtually independent. Fig. 9 demonstrates a substantial decrease of the switching time in the penta-layer structure with the composite free layer, for the same current density, as a function of the thickness of the pinned ferromagnetic layers. Due to the removal of the central region which represented the bottleneck for switching in the monolithic structure the shape anisotropy energy is decreased. However, its value is still sufficiently large for guaranteeing the thermal stability at operation conditions [52]. Larger torque allows to use a lower current density for switching as shown in Fig. 10.

5. Conclusions

Because charge-based memory scaling will be at risk as technology scales down to 20 nm, conceptually new types of memories based on a different storage principle are gaining momentum. A DRAM memory cell based on a transistor alone was introduced in order to resolve the critical scaling problems, but this technology is still volatile and can not be used for universal memory. We demonstrated that STT-MRAM and RRAM are the most promising candidates for future universal memory. In particular, RRAM cells have already surpassed the scaling limits of charge-based storage memories. Despite this, a proper fundamental understanding of the RRAM switching mechanism is still missing hindering further development of this type of memory. Therefore, a better understanding and control of physical SET/RESET processes through development of accurate models is urgently needed. The current challenge for the STT-MRAM technology is to reduce the switching current density. Perpendicular MTJs with interface-induced anisotropy show potential, but still require reducing damping and increasing thermal stability. Material and structure optimization through accurate modeling and simulations is a key ingredient in successful designing of future memory cells with low power consumption.

Acknowledgement

This research is supported by the European Research Council through the Grant #247056 MOSILSPIN.

References

[1] Hong S. Memory technology trend and future challenges. IEEE Int Electron Dev Meet 2010:292–5.
[2] Kryder MH, Kim CS. After hard drives – what comes next? IEEE Trans Magn 2009;45:3406.
[3] Tsuchida K, Inaba T, Fujita K, Ueda Y, Shimizu T, Asao Y, Kajiyama T, Iwayama M, Sugiura K, Ikegawa S, Kishi T, Kai T, Amano M, Shimomura N, Yoda H, Watanabe Y. A 64 Mb MRAM with clamped-reference and adequate-reference schemes. In: IEEE ISSCC; 2010. p. 258–60.
[4] Sheu S-S, Chang M-F, Lin K-F, Wu C-W, Chen Y-S, Chiu P-F, Kuo C-C, Yang Y-S, Chiang P-C, Lin W-P, Lin C-H, Lee H-Y, Gu P-Y, Wang S-M, Chen FT, Su K-L, Lien C-H, Cheng K-H, Wu H-T, Ku T-K, Kao M-J, Tsai M-J. A 4 Mb embedded SLC resistive-RAM macro with 7.2 ns read–write random-access time and 160 ns MLC-access capability, in: IEEE ISSCC; 2011. p. 200–2.
[5] Otsuka W, Miyata K, Kitagawa M, Tsutsui K, Tsushima T, Yoshihara H, Namise T, Terao Y, Ogata K. A 4 Mb Conductive-bridge resistive memory with 2.3 GB/s read-throughput and 216 MB/s program-throughput. In: IEEE ISSCC; 2011. p. 210–1.
[6] Roadmap of 2011 edition can be downloaded from the following URL. <http://www.itrs.net/Links/2011ITRS/Home2011.htm>.
[7] Okhonin S, Nagoga M, Sallese J, Fazan P. A SOI capacitor-less 1T-DRAM concept. SOI Int Conf Technol Dig 2001:153154.
[8] Youshida E, Tanaka T. A capacitor-less 1T-DRAM technology using gate-induced drain-leakage (GIDL) current for low-power high-speed embedded memory. IEEE Trans Electron Dev 2006;53:692697.
[9] Ban D, Avci UE, Shah U, Barns CE, Kencke DL, Chang P. Floating body cell with independently-controlled double gates for high density memory. IEEE Int Electron Dev Meet 2006:573576.
[10] Shino T, Kusunoki N, Higashi T, Ohsawa T, Fujita K, Hatsuda K, et al. Floating body RAM technology and its scalability to 32 nm node and beyond. IEEE Int Electron Dev Meet 2006:569572.
[11] Ban D, Avci UE, Kencke DL, Chang PLD. A scaled floating body cell (FBC) memory with high-K^+ metal gate on thin-silicon and thin-BOX for 16 nm technology node and beyond. Int Symp VLSI Technol 2008:9293.
[12] Ertosun MG, Cho H, Kapur P, Saraswat KC. A nanoscale vertical double-gate single-transistor capacitorless DRAM. IEEE Electron Dev Lett 2008;29:615617.
[13] Avci U, Ban I, Kencke D, Chang P. Floating body cell (FBC) memory for 16-nm technology with low variation on thin silicon and 10-nm BOX. SOI Int Conf Technol Dig 2008:2930.
[14] Hamamoto T, Ohsawa T. Overview and future challenges of floating body RAM (FBRAM) technology for 32 nm technology node and beyond. Solid-State Electron 2009;53:676683.
[15] Okhonin S, Nagoga M, Carman E, Beffa R, Faraoni E. New generation of Z-RAM. IEEE Int Electron Dev Meet 2007:925928.
[16] Rodriguez N, Cristoloveanu S, Gamiz F. Novel capacitorless 1T-DRAM cell for 22-nm node compatible with bulk and SOI substrates. IEEE Electron Dev Lett 2010;31:972–4.
[17] Sverdlov V, Selberherr S. Modeling floating body Z-RAM storage cells. Int Conf Microelectron 2010:45–50.
[18] Waser R, Dittmann R, Staikov G, Szot K. Redox-based resistive switching memories – nanoionic mechanisms, prospects, and challenges. Adv Mater 2009;21:2632–63.
[19] Lee BC, Zhou P, Yang J, Zhang YT, Zhao B, Ipek E, et al. Phase-change technology and the future of main memory. IEEE MICRO 2010;30:143.
[20] Seo S, Lee MJ, H Seo D, Choi SK, Suh DS, Joung YS, et al. Conductivity switching characteristics and reset currents in NiO films. Appl Phys Lett 2005;86:093509.

[21] Dong R, Lee DS, Xiang WF, Oh SJ, Seong DJ, Heo SH. Reproducible hysteresis and resistive switching in metal–Cu_xO–metal heterostructures. Appl Phys Lett 2007;90:042107.
[22] Kugeler C, Nauenheim C, Meier M, Rudiger A, Waser R. Fast resistance switching of TiO_2 and MSQ thin films for non-volatile memory applications (RRAM). Non-Volatile Memory Technol Symp 2008:6.
[23] Yu LE, Kim S, Ryu MK, Choi SY, Choi YK. Structure effects on resistive switching of Al/TiO_x/Al devices for RRAM applications. IEEE Electron Dev Lett 2008;29:331–3.
[24] Jeong DS, Schroeder H, Breuer U, Waser R. Characteristic electroforming behavior in Pt/TiO_2/Pt resistive switching cells depending on atmosphere. J Appl Phys 2008;104:123716.
[25] Shima H, Zhong N, Akinaga H. Switchable rectifier built with Pt/TiO_x/Pt trilayer. Appl Phys Lett 2009;94:082905.
[26] Chen YS, Wu TY, Tzeng PJ. Forming-free HfO_2 bipolar RRAM device with improved endurance and high speed operation. Intl Symp VLSI Technol 2009:37–8.
[27] Lee S, Kim H, Yun DJ, Rhee SW, Yong K. Resistive switching characteristics of ZnO thin film grown on stainless steel for flexible nonvolatile memory devices. Appl Phys Lett 2009;95:262113.
[28] Ho CH, Hsu C-L, Chen C-C, Liu J-T, Wu C-S, Huang C-C, et al. 9 nm half-pitch functional resistive memory cell with <1 μA programming current using thermally oxidized sub-stoichiometic WO_x film. IEEE Int Electron Dev Meet 2010:436–9.
[29] Kim MJ, Baek IG, Ha YH, Baik SJ, Kim JH, Seong DJ, et al. Low power operating bipolar TMO ReRAM for sub 10 nm era. IEEE Int Electron Dev Meet 2010:444–7.
[30] Watanabe Y, Bednorz JG, Bietsch A, Gerber Ch, Widmer D, Beck A, et al. Current-driven insulator conductor transition and nonvolatile memory in Chromium-doped $SrTiO_3$ single crystals. Appl Phys Lett 2001;78:3738.
[31] Sawa A, Fujii T, Kawasaki M, Tokura Y. Hysteretic currentvoltage characteristics and resistance switching at a rectifying Ti/$Pr_{0.7}Ca_{0.3}MnO_3$ interface. Appl Phys Lett 2004;85:4073.
[32] Lin CC, Lin CY, Lin MH. Voltage-polarity-independent and high-speed resistive switching properties of V-doped $SrZrO_3$ thin films. IEEE Trans Electron Dev 2007;54:3146.
[33] Chien WC, Lee FM, Lin YY, Chen YC, Lee MH, Lung HL, et al. Current status and future challenges of resistive switching memories. SSDM 2011:1003–4.
[34] Fujii T, Kawasaki M, Sawa A, Akoh H, Kawazoe Y, Tokura Y, et al. Appl Phys Lett 2005;86:012107.
[35] Szot K, Speier W, Bihlmayer G, Waser R. Switching the electrical resistance of individual dislocations in single-crystalline $SrTiO_3$. Nat Mater 2006;5:312.
[36] Nian YB, Strozier J, Wu NJ, Chen X, Ignatiev A. Evidence for an oxygen diffusion model for the electric pulse induced resistance change effect in transition-metal oxides. Phys Rev Lett 2007;98:146403.
[37] Nishi Y, Jameson JR, Recent progress in resistance change memory, in: Device research conference, 2008, p. 271274.
[38] Wu SX, Xu LM, Xing XJ. Reverse-bias-induced bipolar resistance switching in Pt/TiO_2/$SrTi_{0.99}Nb_{0.01}O_3$/Pt devices. Appl Phys Lett 2008;93:043502.
[39] Rozenberg MJ, Inoue IH, Sanchez MJ. Nonvolatile memory with multilevel switching: a basic model. Phys Rev Lett 2004;92:178302.
[40] Gao B, Sun B, Zhang H, Liu L, Liu X, Han R, et al. Unified physical model of bipolar oxide-based resistive switching memory. IEEE Electron Dev Lett 2009;30:1326.
[41] Makarov A, Sverdlov V, Selberherr S. Stochastic model of the resistive switching mechanism in bipolar resistive random access memory: Monte Carlo simulations. J Vac Sci Technol B 2011;29:01AD03.
[42] Yu S, Guan X, Wong H-SP. Conduction mechanism of TiN/HfO_x/Pt resistive switching memory: a trap-assisted-tunneling model. Appl Phys Lett 2011;93:063507.
[43] Russo U, Ielmini D, Cagli C, Lacaita AL, Spiga S, Wiemer C, et al. Conductive-filament switching analysis and self-accelerated thermal dissolution model for reset in NiO based RRAM. IEEE Int Electron Dev Meet 2007:775.
[44] Kim S, Choi YK. A comprehensive study of the resistive switching mechanism in Al/TiO_x/TiO_2/Al-structured RRAM. IEEE Trans Electron Dev 2009;56:3049.
[45] Sverdlov V, Korotkov AN, Likharev KK. Shot-noise suppression at two-dimensional hopping. Phys Rev B 2001;63:081302.
[46] Parkin SSP, Hayashi M, Thomas L. Magnetic domain-wall racetrack memory. Science 2008;320:190–4.
[47] Chanthbouala A, Matsumoto R, Grollier J, Cros V, Anane A, Fert A, et al. Vertical-current-induced domain-wall motion in MgO-based magnetic tunnel junctions with low current densities. Nat Phys 2011;7:626–30.
[48] Braganca PM, Krivorotov IN, Ozatay O, Garcia AGF, Emley NC, Sankey JC, et al. Reducing the critical current for short-pulse spin-transfer switching of nanomagnets. Appl Phys Lett 2005;87:112507.
[49] Meng H, Wang J, Wang J-P. Low critical current for spin transfer in magnetic tunnel junctions. Appl Phys Lett 2006;88:082504.
[50] Iwayama M, Kai T, Nakayama M, Alkawa H, Asao Y, Kajiama T, et al. Reduction of switching current distribution in spin transfer magnetic random access memories. J Appl Phys 2008;103:07A720.
[51] Zhao H, Lyle A, Zhang Y, Amiri PK, Rowlands G, Zeng Z, et al. Low writing energy and sub nanosecond spin torque transfer switching of in-plane magnetic tunnel junction for spin torque transfer random access memory. J Appl Phys 2011;109:07C720.
[52] Fuchs GD, Krivorotov IN, Braganca PM, Emley NC, Garcia AGF, Ralph DC, et al. Adjustable spin torque in magnetic tunnel junctions with two fixed layers. Appl Phys Lett 2005;86:152509.
[53] Ikeda S, Miura K, Yamamoto H, Mizunuma K, Gan HD, Endo M, et al. A perpendicular-anisotropy CoFeB–MgO magnetic tunnel junction. Nat Mater 2010;9:721–4.
[54] Ohno H. Magnetoresistive random access memory with spin transfer torque write (Spin RAM) – present and future. SSDM 2011:957–8.
[55] Sbiaa R, Lua SYH, Law R, Meng H, Lye R, Tan HK. Reduction of switching current by spin transfer torque effect in perpendicular anisotropy magnetoresistive devices. J Appl Phys 2011;109:07C707.
[56] Devolder T, Chappert C, Crozat P, Tulapurkar A, Suzuki Y, Miltat J, et al. Precharging strategy to accelerate spin-transfer switching below the nanosecond. Appl Phys Lett 2005;86:062505.
[57] Finocchio G, Krivorotov I, Carpentieri M, Consolo G, Azzerboni B, Torres L, et al. Magnetization dynamics driven by the combined action of AC magnetic field and DC spin-polarized current. J Appl Phys 2006;99:08G5007.
[58] Devolder T, Crozat P, Kim J-V, Chappert C, Ito K, Katine JA, et al. Magnetization switching by spin torque using subnanosecond current pulses assisted by hard axis magnetic fields. Appl Phys Lett 2006;88:152502.
[59] Makarov A, Sverdlov V, Osintsev D, Selberherr S. Fast switching in magnetic tunnel junctions with double barrier layer. SSDM 2011:456–7.
[60] Makarov A, Sverdlov V, Osintsev D, Selberherr S. Reduction of switching time in pentalayer magnetic tunnel junctions with a composite-free layer. Phys Status Solidi RRL 2011:1–3. doi:10.1002/pssr.201105376.
[61] Mojumdar NN, Augustine C, Nikonov DE, Roy K. Effect of quantum confinement on spin transport and magnetization dynamics in dual barrier spin transfer torque magnetic tunnel junctions. J Appl Phys 2010;108:104306.
[62] Finocchio G, Azzerboni B, Fuchs GD, Buhrman RA, Torres L. Micromagnetic modeling of magnetization switching driven by spin-polarized current in magnetic tunnel junctions. J Appl Phys 2007;101:063914.
[63] Slonczewski J. Current-driven excitation of magnetic multilayers. J Magn Magn Mater 1996;159:L1–7.
[64] Slonczewski J. Currents, torques, and polarization factors in magnetic tunnel junctions. Phys Rev B 2005;71:024411.
[65] Miltat JE, Donahue MJ. Numerical micromagnetics: finite difference methods. In: Kronmuller H, Parkin S, editors. Handbook of magnetism and advanced magnetic materials. John Wiley & Sons, Ltd.; 2007.
[66] Tomáš D. Modelling of micromagnetic structures. PhD Thesis. Paris-Sud University, Orsay and Charles University, Prague; 1999.
[67] Kákay A, Numerical investigations of micromagnetic structures. Ph.D. Thesis. Research Institute for Solid State Physics and Optics, Budapest; 2005.
[68] Ito K, Devolder T, Chappert C, Carey MJ, Katine JA. Probabilistic behavior in subnanosecond spin transfer torque switching. J Appl Phys 2006;99:08G519.
[69] Torres L, Lopez-Diaz L, Martinez E, Alejos O. Micromagnetic dynamic computations including Eddy currents. IEEE Trans Magn 2003;39:2498–500.