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Hardware Implementation of the Multirate Decimation Filter for Noise Thermometer based on FPGA

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ABSTRACT

This paper introduces an efficient Field Programmable Gate Array (FPGA) realization of a multirate decimation filter with narrow pass-band and narrow transition band for Noise thermometer application. The filter is composed of three stages; the first stage is a Cascaded Integrator Comb (CIC) decimation filter, the second stage is a two-coefficient half-band (HB) filter and the last stage is a sharper transition half-band filter. The frequency responses and implementation area of the proposed filter stages are compared. Using CIC-HB technique saves 18% of the design area, compared to the six stages half band filters.

Keywords: All-pass filters, CIC filter, half-band filter, multirate filter, polyphase filter, FPGA, Noise thermometer.

INTRODUCTION

Multirate filters have wide application in digital systems for data rate conversion as well as filtering. One of the applications that use multirate techniques is the noise thermometer for metrological and industrial temperature measurements. This noise thermometeris based on the Nyquist theorem [1], which describes the relation between the spectral density of the noise voltage (V) and the temperature (T) of a sensing resistor (Re (Z)).

$$V^2 = 4kTRe(Z) \qquad (1)$$

Where *k* is the Boltzmann's constant [3].

Because this thermal noise is independent of the sensor material, this principle is of interest. To eliminate the parasitic noise (e.g. amplifier noise), a configuration with two channels and cross correlation are used as shown in fig.1 [1]-[3]. The frequency dependent gain will be determined by measuring the noise voltage of a reference resistor at well-known temperature (e.g. triple point of water) [4].

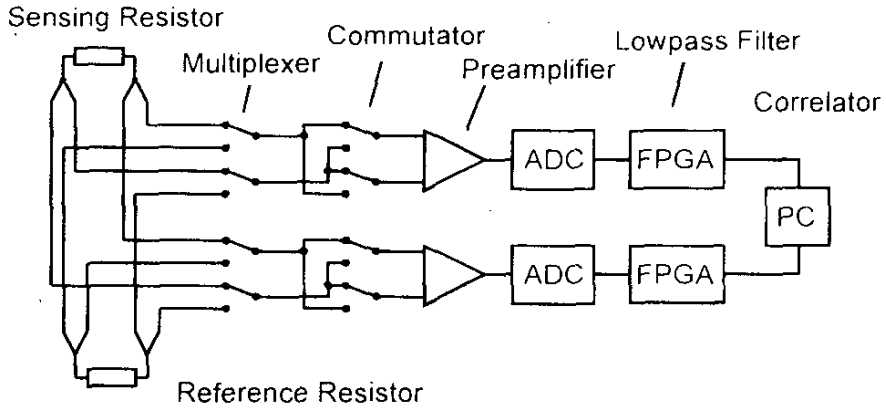

Fig. 1: Block diagram of the noise thermometer.

Traditionally, digital signal processing (DSP) algorithms are implemented using general purpose programmable DSP chips for low rate applications. For higher rates, special purpose fixed function DSP chips and Application Specific Integrated Circuits (ASICs) are used. The FPGA maintains the advantages of custom functionality like an ASIC while avoiding the high development costs and the inability to make design modifications after production. FPGA offer a better solution when a design requires the use of DSP algorithms, or time to market is critical, or design adaptability is crucial. Hence, the multirate filter is implemented using FPGA.

MULTIRATE FILTER ARCHITECTURE

To design a multirate digital filter, it is important to specify the overall filter requirements, determine the number of stages of decimation that will yield efficient filter implementation, and chose the appropriate decimation factors for each stage and design an appropriate filter for each stage.The multistage design offers significant savings in computation and storage requirements over a single stage design. Multipliers represent most of the hardware used to implement a multirate filter. As a result, multipliers contribute to most of the power consumption in a multirate filter. CIC filters do not need multipliers. Therefore, they have been cascaded in the beginning of the filter chain [5].

The proposed multistage multirate low-pass decimation filter with the following specifications: a pass-band frequency of 300 KHz, a stop-band frequency of 400 KHz, a maximum pass-band attenuation of 0.1dB and a minimum stop-band attenuation of 60dB.In this design , a F_s = 40MHz input sampling frequency is first reduced to 2.5MHz (F_s/16) with a third order CIC filter, Followed by further reduction to 625 KHz using two half-band (HB) filters as shown in fig. 2.

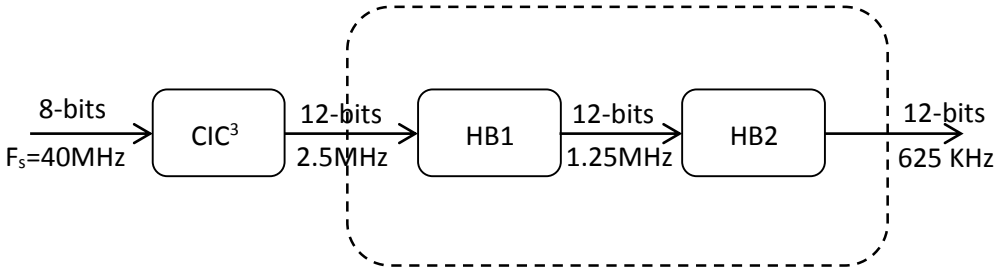

Fig.2 Building blocks of the proposed multirate filter

CASCADED INTEGRATORCOMB FILTER:

The Cascade Integrator Comb (CIC) filter introduced by Hogenauer [6] is commonly used in communications and signal processing systems as an efficient first stage in the process of sample rate conversion. These filters have a low-pass response and are multiplier-free. The attraction of these filters lies in their economical implementation: each structure uses limited storage and does not require multipliers. The decimating CIC filter consists of a cascade of *N* integrators followed by a section composed of *N* comb filters.Between these two sections, the signal is downsampled by afactor of *R*.

Fig.3 shows a three-stage CIC filter that consists of a three-stage integrator, a sampling rate reduction by R, and a three-stage comb. This arrangement saves a factor R of delay elements in the comb sections.

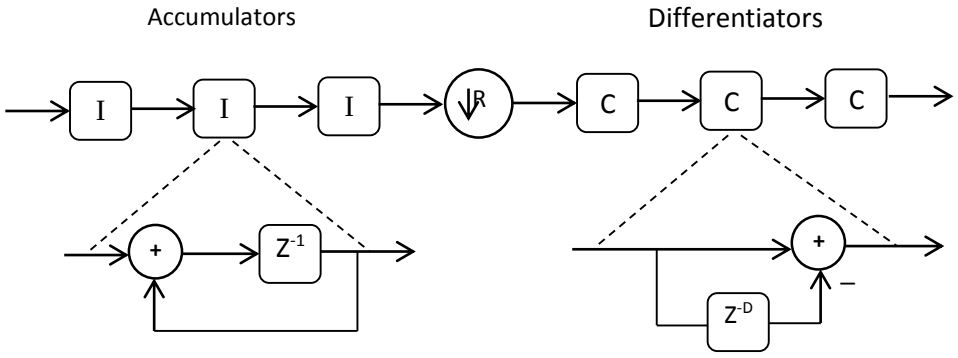

Fig. 3 CIC filter realization

The transfer function of the decimating CIC filter is

$$H(z) = \left(\frac{1-z^{-RM}}{1-z^{-1}}\right)^{N} \quad (2)$$

leading to the frequency response

$$H(\omega) = \left(\frac{\sin\left(\frac{\omega RM}{2}\right)}{\sin\left(\frac{\omega}{2}\right)}\right)^{N} \quad (3)$$

where R is the decimation factor of the filter, M is the differential delay (or the number of samples to delay the input signal in the comb stages), and N is the number of stages in the CIC. The number of delays M for a high-decimation rate filter is typically one or two [7]. The CIC filter output bit width follows

$$B_{out} = B_{in} + ceil[\log_2(RM)^N] \quad (4)$$

whereB_{out} is the bit width of the CIC filter output and *Bin* is the bit width of the input to the CIC filter, then the accumulators will not overflow and the filter will be stable.A three-stage CIC filter with B_{in}= 8 bits, M = 1, and$R$ = 16, would require an internal wordwidthof B_{out}= 20 bits to ensure that run-time overflow would notoccur [8]. The output word width would normally be a value significantly lessthan B_{out}, we used 12 bits.Fig. 4 shows the frequency response of CIC filter.

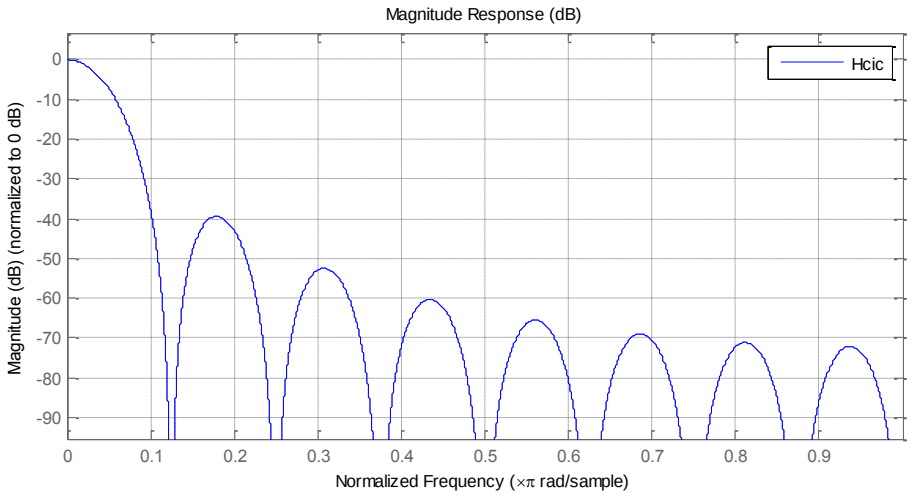

Fig. 4: Frequency response of the CIC decimation filter (R=16,M=1,N=3)

HALF-BAND FILTERS

Half-band filters are required as a filter as well as a decimator. The remaining 4x of decimation can be performed in two stages half-band filters. Decimation by two can be realized efficiently by using cascaded poly phase two path half-band Infinite Impulse Response (IIR) filters. The two coefficient fifth order filter is an attractive half-band IIR structure from the design as well as realization point of view. The first HB filter acts as a filter to improve the stop-band attenuation as well as reduce the sampling frequency from 2.5 MHz to 1.25 MHz. The transfer function of the two-coefficient filter employing the second-order all-pass section, having the structure shown in fig. 5, is givenby (5) and itsfrequency response is shown in fig. 6.

$$H_1(z) = 0.5 \cdot \left[\frac{a + z^{-2}}{1 + az^{-2}} + z^{-1} \frac{b + z^{-2}}{1 + bz^{-2}} \right] \qquad (5)$$

Where ‘a’ and ‘b’ are the branch coefficients.

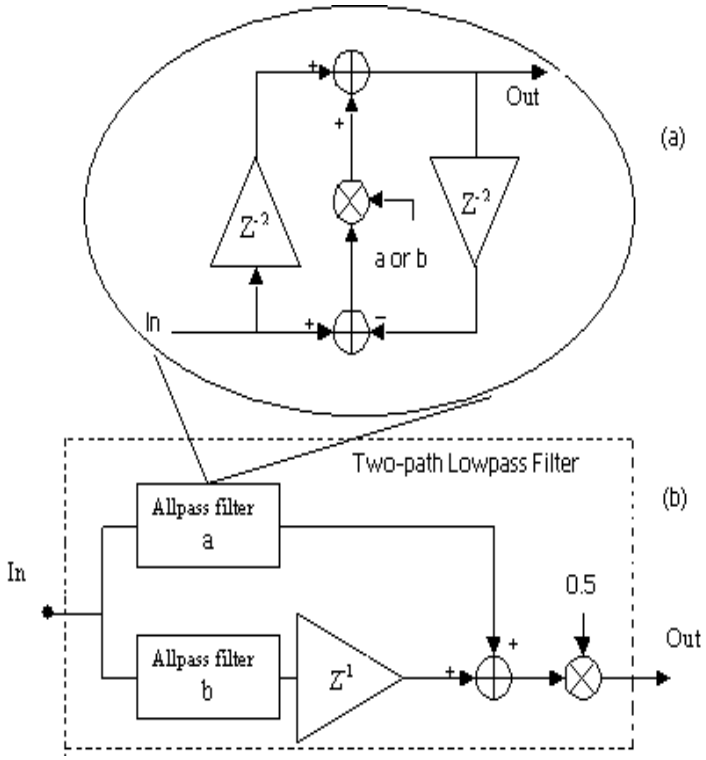

Fig.5: TheHB filter, (a) the basic second-order all-pass, and (b) the two-path half-band low-pass filter.

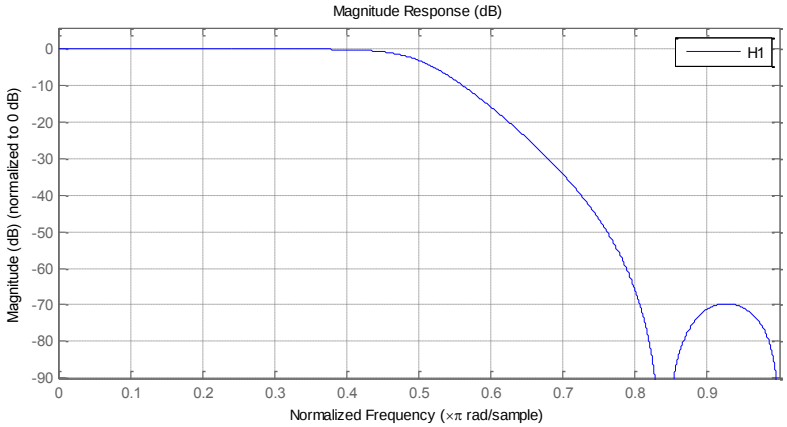

Fig.6: Frequency response of thefirst half-band filter

The second HB filter is a higher order filter to achieve sharper transition and simpler realization in the last stage of the multirate low pass filter (LPF). In this design, the second HB filter is a two cascaded two-coefficient filters with two different coefficient sets and it reduces the sampling frequency from 1.25 MHz to 625 KHz. The transfer function of the second HB filter is given by (6).

$$H2(z) = \left(0.5 \cdot \left[\frac{a_0 + z^{-2}}{1 + a_0 z^{-2}} + z^{-1} \frac{b_0 + z^{-2}}{1 + b_0 z^{-2}} \right] \right) \times \left(0.5 \cdot \left[\frac{a_1 + z^{-2}}{1 + a_1 z^{-2}} + z^{-1} \frac{b_1 + z^{-2}}{1 + b_1 z^{-2}} \right] \right) \qquad (6)$$

The frequency response of the two-cascaded two-coefficient filter (H2) is shown in fig. 7. The binary values of the coefficients of the half-band filters are summarized in Table I [10].

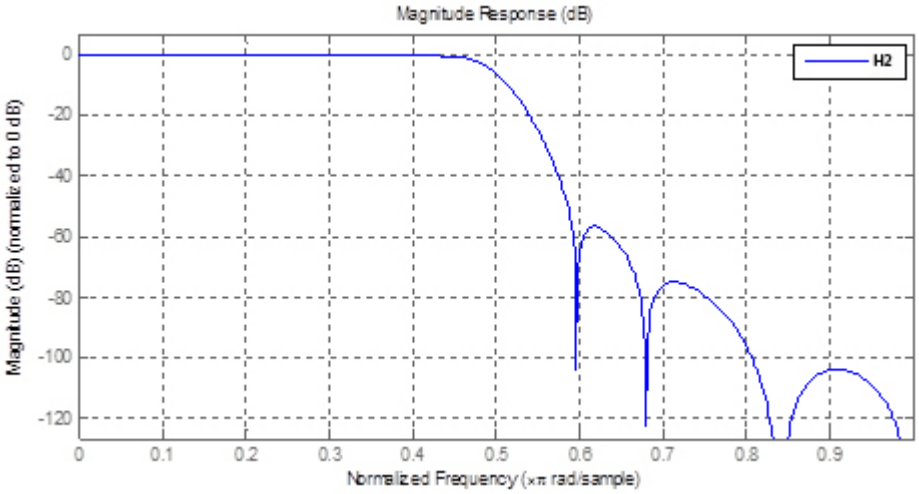

Fig. 7: Frequency response of the second half-band filter

Table I: Half-band filters coefficients in fixed-point binary representation

Half-band filter	Resp.	a_0	b_0	a_1	b_1
Two-coefficient	H1	0.001	0.1001	--	--
Two-cascaded two-coefficient	H2	0.001	0.1001	0.01001	0.11

From table I, the few one-bits in the coefficient indicate the simpler realization of the multiplication process.

FPGA REALIZATION

The FPGA chip (Xilinx Virtex800 "XCV800") is utilized to implement two filter channels, and interface to PCI card for the design case of the noise thermometer. The XCV800 has 9408 slices, where a slice is the unit of the Virtex architecture [11]. A custom PCI card was used where a Xilinx Virtex 800 FPGA "XCV800" is mounted as shown in fig.8.

Fig.8 Universal Digital signal processor Data Acquisition board (UNIDAQ)

Table II presents the XCV800 utilization for implementation of multirate decimation filter three stages. Note: In all listing of the device utilization summary, the number of CLB's can be calculated as half the number of slices.

Table II: XCV800-based implementation of multirate filter stages.

	CIC	HB1	HB2
No of Slices (Max 9408)	191	74	154
No. of Flip Flops (Max 18816)	326	100	203
No. of 4 input LUTs (Max 18816)	165	89	210
Max. Freq. (MHz)	94.742	72.228	60.064

The interface to the PC consumes 48 slices and the total design consumes 844 slices (9%). For comparison with other solutions, the implemented multirate filter using six stages half band filters introduced in [10], utilizes 1034 slices (11%) of a XCV800.

CONCLUSION

The realization of an efficient multistagemultirate decimation low-pass filter and its application in a noise thermometer system are introduced. The two filter channels are realized on an FPGA chip (Xilinx XCV800). The proposed filter is composed of three stages, where the CIC filter is used in the first stage followed by two stagesHB filter. Using CIC-HB technique instead of six stages half band filters saves 18% of the design area, while achieving the same performance.

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