AN IMPROVED ECG SIGNAL ACQUISITION SYSTEM THROUGH CMOS TECHNOLOGY

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Abstract:
This paper presents the design and realization of low power, high gain PC based system for ECG and data acquisition of a patient's heart condition. The advantage of this system is the use of standard CMOS process which will reduce the complexity and cost of the manufacturer. The system consists of three subsystems- Operational Amplifier based Pre-amplifier, ADC and USB interface device. High gain around 85 dB, low power dissipation of typically 0.683 mW and 61.5 degree phase-margin for stable closed loop operations were achieved. All design and simulation were done using Tanner Tool 0.5 µm technology.

Keywords: ECG, Opamp, ADC, Tanner Tool 0.5.

1. Introduction

The electrocardiogram (ECG) is an important diagnostic tool in the detection and treatment of heart disease. This is often done in a clinical environment under the care of physician. For at risk patients, an effective and potentially life saving approach to monitor the patient's heart throughout the day is necessary. This would provide the physician a long tern assessment of the patient's health for asymptomatic or intermittent heart problems. Our system could also be designed to allow the physician to remotely access the recorded data which would allow for a timely response to any potential warning signs. In order to achieve a smaller and cost effective ECG system, VLSI techniques need to be employed. This work is an effort to create a CMOS based ECG acquisition system consisting of operational amplifier based pre-amplifier, ADC and USB interface device as subsystems. CMOS technology provides an ideal platform for the implementation of all the electronic components.

The purpose of this paper is to explore various circuit techniques [1] in developing the ECG acquisition system through CMOS analog building blocks such as operational amplifier based pre-amplifier, ADC and USB interface device. We propose an ECG acquisition system based on CMOS technology applicable for ECG monitoring applications. A block diagram of the system is shown in Fig.1. A Preamplifier is designed using op-amp with suitable gain, phase-margin, slew rate, bandwidth and CMRR. The ECG signal is received by this op-amp based preamplifier and the amplified signal is passed to the 8 bit ADC section. A high speed 8 bit Flash Type ADC is used for this purpose. The analog signal is converted into 8 bit digital signal with proper resolution and is passed to the PC through USB section. The USB section act as an interface between computer and ADC section. The installed tool in the computer can read this binary bit and show its output.

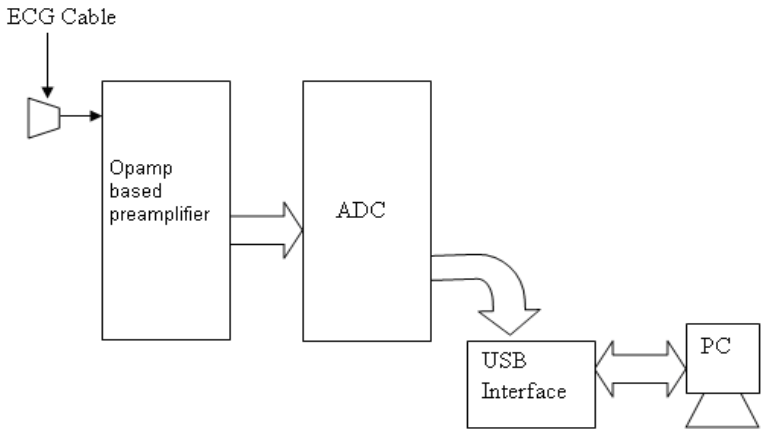


Fig.1 Block diagram of proposed system

2. System Design

Our system consists of three subsystems namely preamplifier, ADC and USB interface. Each subsystem is explained in the following sections.

2.1 *Operational Amplifier based Pre-amplifier*

An operational amplifier often referred as an '**op-amp**', is a direct coupled high gain differential voltage amplifier with one inverting and one non-inverting input. The single output voltage is the difference between the inverting and non-inverting inputs multiplied by the open-loop gain.

Op-Amps are among today's most widely used circuit building blocks. They can be used as summers, integrators, differentiators, comparators, attenuators and much more. Designers have been trying to integrate these versatile building blocks into the rest of their circuitry. In an effort to reduce cost and space and improve performance, designers are integrating more and more circuit blocks, both analog and digital, onto a single chip. This implementation of 'mixed signal' chips in a standard CMOS process reduces power dissipation to a great extent. In a further effort to reduce power dissipation in digital circuit blocks, it is advantageous to reduce the supply voltage $V_{dd.}$. For a standard CMOS inverter, power dissipation may be expressed as:

$$\mathbf{P_{avg} = C * V_{dd} * f}$$

In an effort to increase the intrinsic gain of CMOS devices, the trend in the MOSFET design industry is to shrink the gate oxide thickness, t_{ox}. Unfortunately, as t_{ox} is reduced, the MOSFET device's tolerance for high voltage levels at the gate is also reduced. This means that it is advantageous to reduce the maximum voltage supply V_{dd} for better reliability. This trend in reducing the supply voltage means that analog designers face challenges such as reduced input common mode range, output swing and linearity. Part of the problem is that V_{TO} does not scale in a linear fashion with the reduction in minimum device length. Unfortunately for the designer, V_{TO} does not tend to decrease at the same rate as V_{dd}. Some fabrications do offer low V_{TO} processes specially suited for analog blocks but they tend to cost more than standard CMOS processes. It is therefore desirable to use low voltage design techniques in order successfully implement analog circuit blocks using standard CMOS process.

The most commonly used configuration for CMOS operational amplifiers is the two stage amplifier [2] and [3]. There is a differential front end which converts a differential voltage into a current and a common source output stage that converts the signal current into an output voltage. An important criterion of performance for these op amps in many applications is the settling time of the amplifier.

In a never-ending effort to reduce power consumption and gate oxide thickness, the integrated circuit industry is constantly developing smaller power supplies. Today's analog circuit designer is faced with the challenge of making analog circuit blocks with 1V supplies with little or no reduction in performance. Furthermore, in an effort to reduce costs and integrate analog and digital circuits onto a single chip, the analog designer must often face the above challenges using plain CMOS processes.

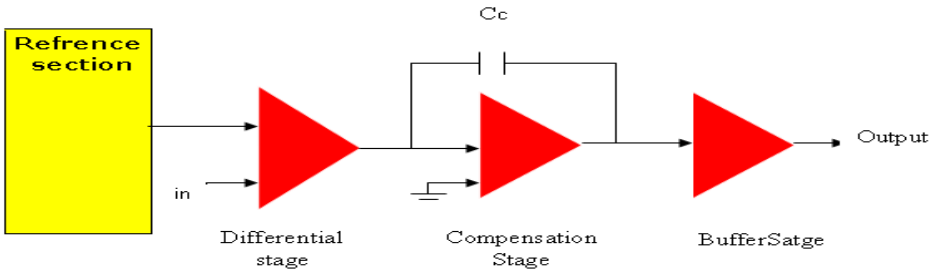
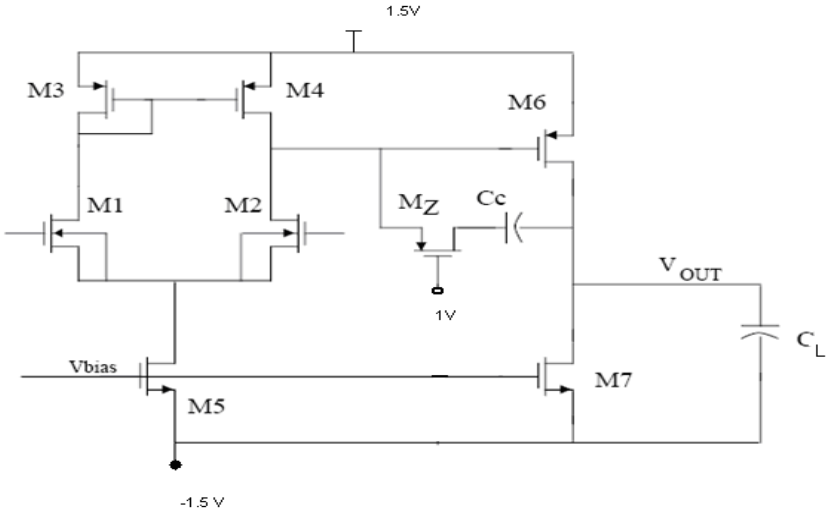


Fig.2 Block diagram of preamplifier

A block diagram of op-amp based pre-amplifier is shown in Fig.2. It consists of differential stage, compensation stage and buffer stage. Several DC imperfections in realizing a real op-amp such as finite gain, input bias current, input offset voltage, finite bandwidth, slew rate etc. are taken into account in compensation stage. Buffer stage is included for impedance matching purpose. Detail circuit diagram of two stage CMOS op-amp is shown in Fig.3.



. Fig.3 Schematic diagram of two stage op-amp

2.2 *Analog to Digital Converter*

Flash Type, Interpolation Type, Folding Type and Pipelined Type, Time Interleaved Type and Delta Sigma Type are few popular high speed ADCs [4]. In our design, we have used Flash type ADC. A Flash Type ADC usually referred as direct-conversion ADC has a bank of comparators sampling the input signal in parallel, each firing for their decoded voltage range [5] and [6]. The comparator bank feeds a logic circuit and generates a code for each voltage range. Direct conversion is very fast, capable of gigahertz sampling rates, but usually has only 8 bits of resolution or fewer, since the number of comparators needed, 2^N - 1, doubles with each additional bit, requiring a large, expensive circuit. ADCs of this type have a large die size, a high input capacitance, high power dissipation, and are prone to produce glitches at the output. This demerit can be overcome by using a novel approach of using clocked comparators. It is extremely important that all comparators are clocked simultaneously to avoid jitter, which reduces the resolution at high speeds.

Fig.4 shows 8 bit Flash type ADC. This ADC converts the analog ECG signal into a digital word in one clock cycle that has two phase periods.

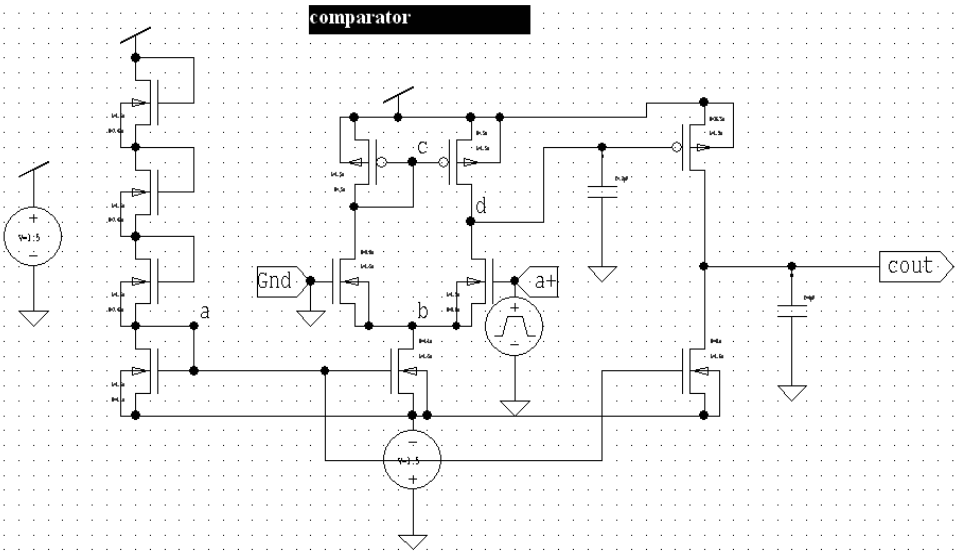


Fig.4 Schematic diagram of ADC

2.3 *USB Interface*

This section is used for interfacing the computer and ADC. Any high speed Analog to digital converter compatible USB interface can be used. USB 8451 is used in our work.

3. Equations for Preamplifier design

Step1 $$(\frac{W}{L})_{3,4} = (\frac{C_c + C_l}{C_c})(\frac{W}{L})_{5,8}$$

Setp2 $$(\frac{W}{L})_{3,4} = \frac{(\frac{W}{L})_6}{2(\frac{W}{L})_7}(\frac{W}{L})_{5,8}$$

Step 3 $$(W/L)_9 = \frac{2C_C SR}{\mu_p C_{ox} V_{HR}^{out+}(V_{DD} - V_{HR}^{out+} - 2|V_{tp}|)}$$

Step 4 $$(\frac{W}{L})_{5,8} = \frac{2SRC_c}{\mu_n C_{ox}(V_{HR}^{CM} - V_m - \frac{SR}{w_n})^2}$$

Step 5 $$W_b = \frac{2SR(C_c + C_l)}{\mu_p C_{ox}(V_{HR}^{out})^2} L_b$$

Step 6 $$I_{D5} = C_c SR$$

Step 7 $$(\frac{W}{L})_{1,2} = \frac{\omega_M^2 C_c}{\mu_n C_{ox} SR}$$

Step 8 $$L_6 = \sqrt{\frac{3\mu_p V_{HR}^{CR} C_c}{2w_n(C_c + C_l)\tan(\Phi_N)}}$$

Step9 $$C_c = \frac{16kT}{3w_n S_n(f)}[1 + \frac{SR}{w_n(V_{HR}^{CM} + V_{tn}}]$$

Step 10 $$I_{D7} = SR(C_c + C_L)$$

Step 11 Slew rate = $\frac{Is}{Cs}$

Step 12 First stage gain Av1 = $\frac{-g_{m1}}{g_{ds2}+g_{ds4}} = -2\frac{g_{m1}}{Is(\lambda_2+\lambda_4)}$

Step 13 Second-stage gain Av2= $\frac{-g_{m6}}{g_{ds6}+g_{ds7}} = \frac{-2g_{m6}}{I_6(\lambda_6+\lambda_7)}$

Step 14 Gain Bandwidth GB $= \frac{g_{m1}}{C_c}$

Step 15 Output Pole $p_2 = \frac{-g_{m6}}{C_L}$

Step 16 RHP zero $z_1 = \frac{g_{m6}}{C_C}$

Step 17 Positive CMR Vin (max) $= V_{DD} - \sqrt{\frac{I_5}{\beta_3}} - |V_{T03}|(\max) + V_{T1}(\min)$

Step 18 Negative CMR Vin (min) = $V_{SS} + \sqrt{\frac{I_5}{\beta_1}} + |V_{T1}|(\max) + V_{DS5}(\min)$

4. Simulation Results

Designing, simulation, schematics and comparison of various performance parameters were done for two different topologies. Simulation was carried out using T-spice TANNER Tool. All kinds of analysis including transients for these topologies were done. Frequency response of pre-amplifier for 6V/μs and 92 V/μs are shown in Fig.5 and Fig.6 and the transient response in Fig.7.

A comparison were done on the basis of various performance parameters such as open loop gain, phase-margin, and bandwidth, slew-rate, settling time, power and CMR (V) and is summarized in table-1. On the basis of table-1, it was found that as we increase the slew rate, power dissipation drops to a substantial level and settling time also reduces.

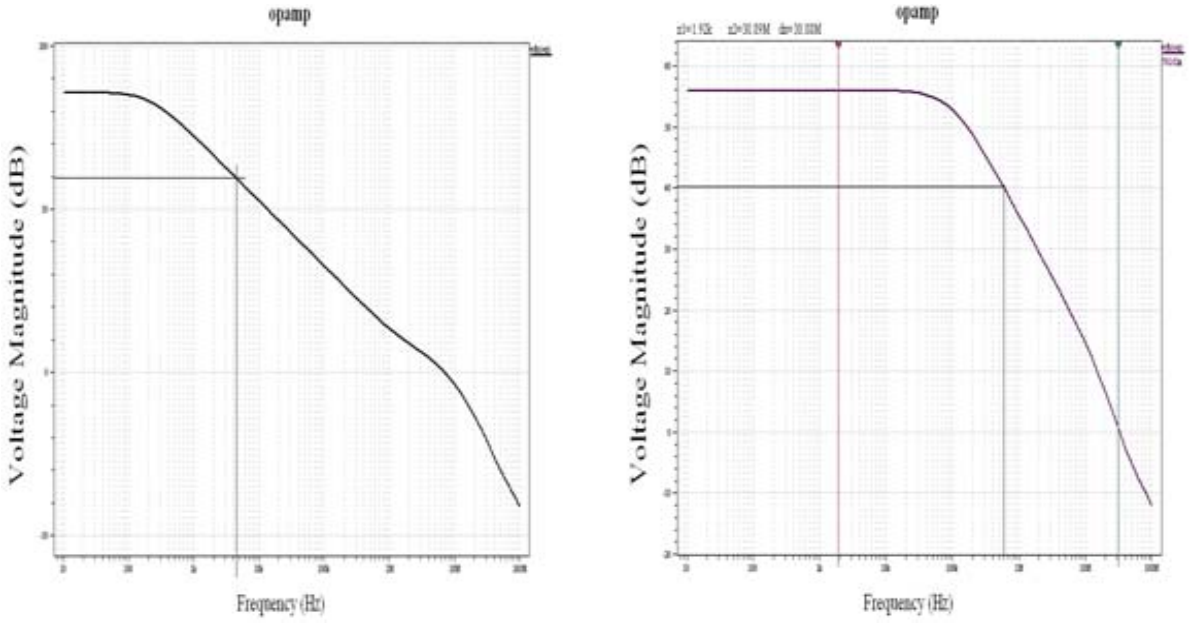


Fig.5 Gain Vs Frequency Plot

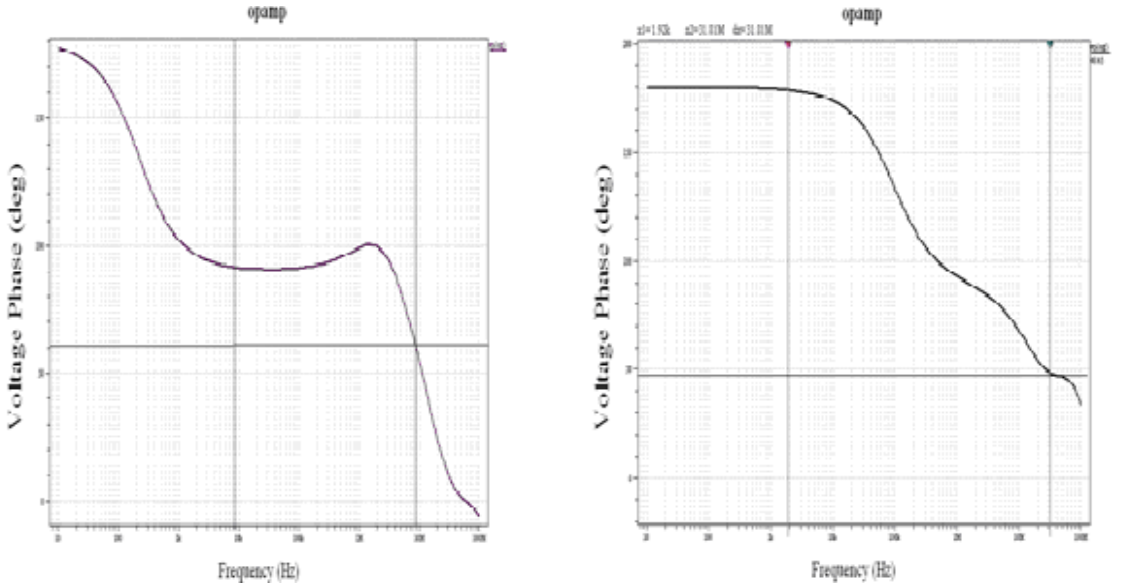


Fig.6 Voltage Phase Vs Frequency Plot

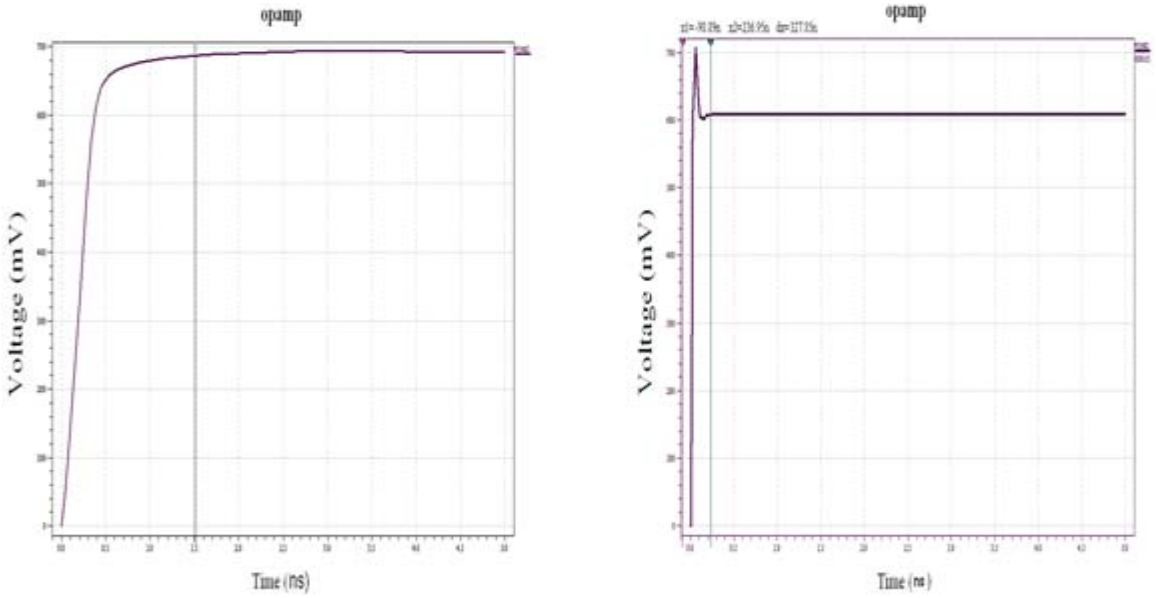


Fig.7 Transient response of preamplifier

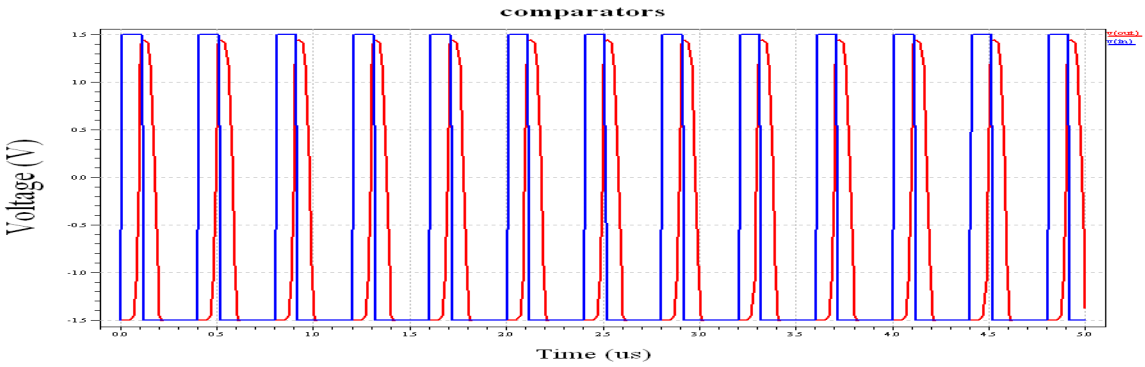


Fig.8 Input-Output waveforms of ADC

Table 1. Comparative analysis of the system for 6V/μs and 92 V/μs 6

Specification	Requirements	Results for 6uV/sec @ 1.5V RL=63k? CL=3.8 pF Cc=0.83pF	Results for 91uV/sec@1.5VRL=83k CL=0.22 pF Cc=0.055pF
Open Loop Gain	> 80 dB	85dB	56 dB
Phase Margin	> 60 degrees	61.5 degrees	50 degrees
Bandwidth	>100 KHz	4.5 KHz	500KHz
Slew Rate	>5 V/us	6.2 V/us	91 V/us
Settling Time	< 300 us	1.5 ns	0.25 ns
Power	< 1mW	0.693mW	0.105 mW
CMR(V)	+1/-1	1.32 / -0.852	1.32 / -0.852

5. Conclusion and Future work

This paper has detailed the design of a CMOS process based ECG acquisition system using high speed Flash Type ADC. The design has determined that the circuit gain is 85 dB and power dissipation is 0.693mW. The circuit has good immunity from noise; good frequency response, improved phase margin (61.5 degrees) and produces an ECG output voltage such that it can be easily read by the ADC and thus the users.

This schematic can be used for layout design. The preamplifier and ADCs can be designed using 0.18μm CMOS technology. The improved parameters from both the technologies can be optimized using soft computing algorithms such as fuzzy logic, neural network, BFO, genetic algorithm etc.

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