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Broadband Branch Line Balun using Meander line on Silicon Substrate

Harsimran Singh[1], Ayan Karmakar[2] and Kamaljeet Singh[2]
[1]*Student of Dept. of Electronics and Communication, Rayat and Bahra Institute of Engineering and Biotechnology, Mohali, Punjab, India)*
[2]*MEMS Development Division, Semi-Conductor Laboratory (SCL), Mohali, Punjab, India)*

Abstract : *This article presents the design of L-band branch line balun using microstrip configuration on high resistive silicon substrate (ρ>8KΩ-cm). In comparison to earlier designs better performance is achieved by meandering all the four branches and appending a quarter wavelength short circuited stub at the upper right corner of the structure. The circuit is designed using circuit simulator of Agilent's advanced design system (ADS) and further verified using Ansoft's FEM and ADS's MoM based electromagnetic solvers. Comparative study is carried out among various simulation techniques and analyzed. Fabrication methodology along with design steps are detailed in this article. Proposed design saves around 60% print area as compared to conventional topology. Further comparison with other reported topologies have also been discussed.*
Keywords - *Branch line balun, high resistive silicon, microstrip line, short circuited stub, via hole.*

I. INTRODUCTION

Baluns are generally used to convert unbalanced input to balanced output. Balun configurations are being used in various circuits such as balanced mixers, antenna, push pull amplifier, frequency multiplier and antenna feed networks [1-5]. Rapid development in digital wireless communication system demands wider bandwidth without compromising the size.

Conventional branch line balun [6] is composed of two quarter wavelength lines and two half wavelength lines. It has quite simple structure as compared to other types of baluns and can provide low insertion loss with promising return loss characteristics. Further viability of Si as a substrate has been established [7] by the author.

Present article proposed the branch line balun having meandered branches. It consists of two quarter wavelength lines, two half-wavelength lines and a quarter wavelength short circuited stub with via-hole. It is compact and around 60 % print area is less as compared to conventional topology [8]. Present design is carried out on Si substrate and optimized to cater for the desired specifications. The most critical part is the implementation of via topology for which fabrication aspects has been detailed.

II. BALUN DESIGN

The Proposed balun comprises of a pair of quarter wavelength transmission line(branch 1&3) and a pair of half wavelength transmission line(branch 2&4) and a quarter wavelength short circuited stub attached at the upper right corner, as shown in the Fig.1. Various branch line impedances are governed by the following equation [9]:

$$Z_1=Z_2/((\sqrt{2}\times Z_2)-Z_0 \quad \text{.....(1)}$$

Where Z_0 (50Ω) is the characteristic impedance of the input/output line and Z_1 & Z_2 are the impedances of the branch-1 and branch 2-4 respectively. One of them is chosen based on ease of fabrication and the other one can be determined from the Equation (1). In this study the branch line impedance are selected as Z_1= 86.10 Ω and Z_2= 60Ω.

The circuit is designed on the high-Resistive Si-substrate (ε_r=11.8 & tanδ = 0.001) of 675 μm thick considering metal (Al/Au) thickness as 1-2 μm. The effective permittivity (ε_{re}) of the substrate is calculated as:

$$\varepsilon_{re} = \frac{\varepsilon_{re}+1}{2} + \frac{\varepsilon_{re}-1}{2} * \left\{1+\frac{12h}{w}\right\}^{-\frac{1}{2}} \quad \text{..... (2)}$$

Where, ε_r is the dielectric constant of the substrate and 'w' and 'h' are the width of the microstrip and height of the substrate, respectively.

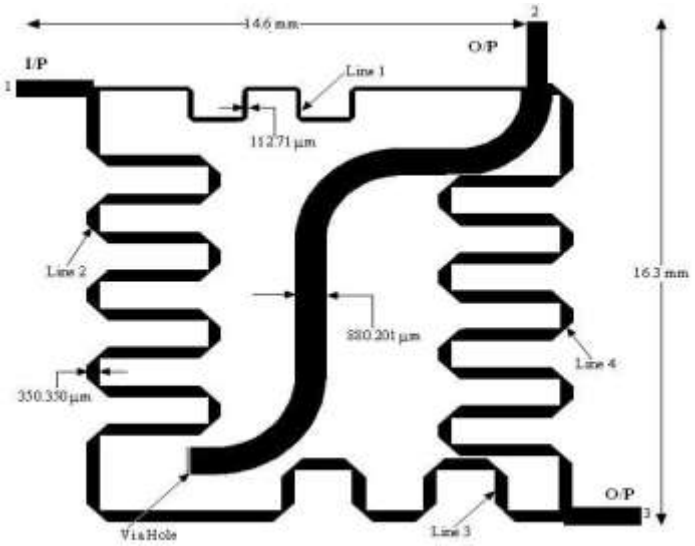

Figure 1: Layout of the designed Balun

Based upon above calculation balun has been designed at the centre frequency of 1.575GHz. Optimizing the design for the specified target, the physical parameters were found out to be as, the width of λ/4 line and λ/2 is 112.71 µm and 350.350 µm respectively with an overall area of 14.6 mm × 16.3 mm. The critical dimension of the structure is 18.87 µm. The width of the short circuited stub is 880.201 µm and with a via-hole cross-section of 880.2 µm ×100 µm. The conventional balun is of size 17.2 mm × 34.3 mm. Fig.2 shows the 3D structure of the design built in the FEM environment. Compared to conventional structure, a compact structure with 60 % less area is achieved by incorporating short circuited stub & meandering.

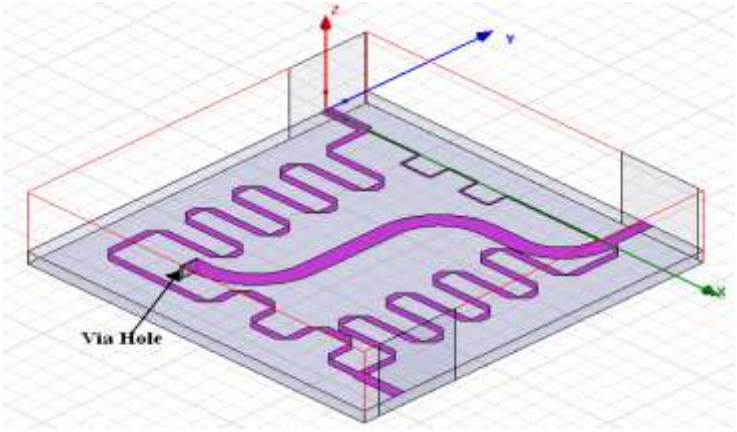

Figure 2: Isometric view of the designed balun

III. RESULTS

The simulation study and optimization is being carried out using circuit simulator, MoM and FEM based electromagnetic solvers [10] [11]. The main design challenge was to optimize the performance catering to undesired and cross-coupling phenomena between various branches.

Fig.3 shows the return loss (S_{11}) behavior of the designed structure. It shows better than 20 dB return loss over a wide band of frequencies (1.4 GHz to 1.9 GHz). There is a significant degradation of matching of around 6 dB in case of FEM in comparison to two other environments. It is basically due to Si substrate which is modeled for losses accurately in FEM based solvers. The losses are primarily due to undesired surface waves and leaky waves contributing in higher dielectric losses. FEM basically solves the problem using volumetric discretization method by evaluating the approximate solution of partial differential equations and integral equations for the given boundary conditions.

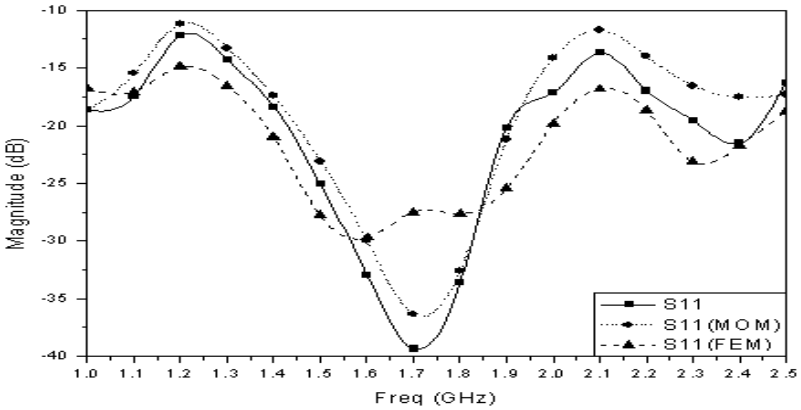

Figure 3: Input Return loss (S_{11}).

Fig 4 shows the insertion loss (S_{21}, S_{31}) at two balanced output ports. It's clear from the graph that a flat (almost constant) insertion loss nature is at the two output ports of the balun structure for wide band (1.4 GHz to 1.9 GHz). Here also FEM results show around 1 dB more loss because of the above said effects. And, in practice we used to always follow this result as a reference in many cases as it takes into consideration various practical situation during the simulation.

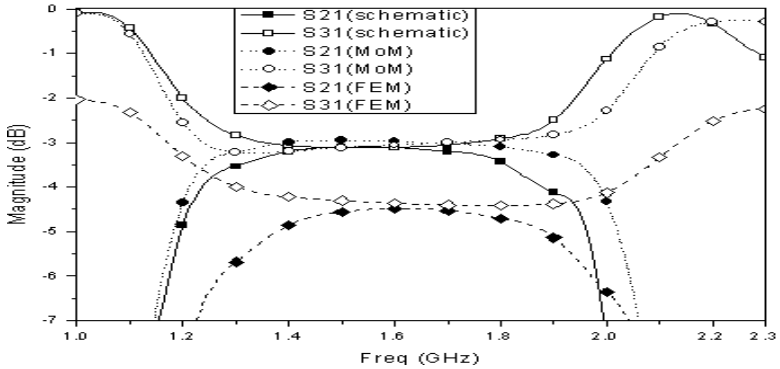

Figure 4: Insertion loss ($S_{21,}$ S_{31}) at two balanced output ports

Fig. 5 shows the phase difference between the two output ports which is -180.669° in case of schematic simulation, -176.194° and -176.089° in case of MoM based simulation and FEM based simulation respectively. The obtained 180±5° phase bandwidth of the designed balun is around 299 MHz (1.364 to 1.663 GHz) in case of schematic simulation, 355 MHz (1.488 to 1.843 GHz) in case of MoM simulation and 369 MHz (1.499 to 1.868 GHz) in case of FEM simulation. In case of FEM analysis, the effect of via-hole is very dominant for phase analysis. This is because of via-hole offers a parasitic inductance which in turn is a phase lagging component. The shape and size of the via-hole basically dictates the parasitic inductance for a given height of substrate, which can be accurately computed using only FEM

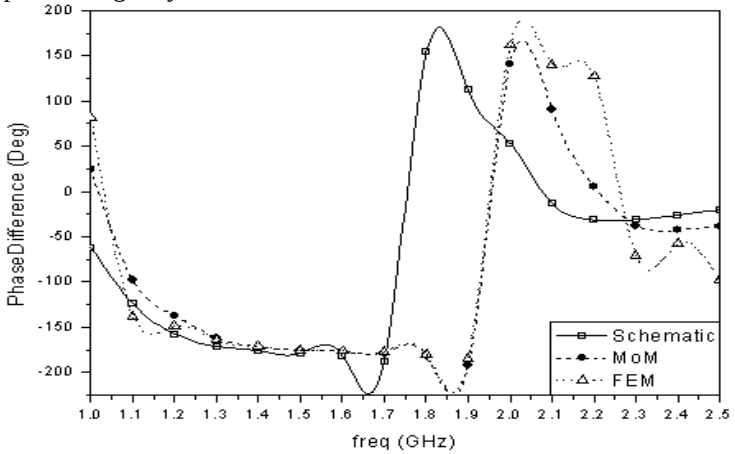

Figure 5: Output Phase Difference

A surface current density (J_{sur}) distribution plot is shown in Fig. 6. It depicts that there is a current crowding (densely populated current vectors) at the bending of the lines or at the corner of the line/stub. In case of meander line, there a clear indication of mutual coupling vectors (oppositely directed current vectors).

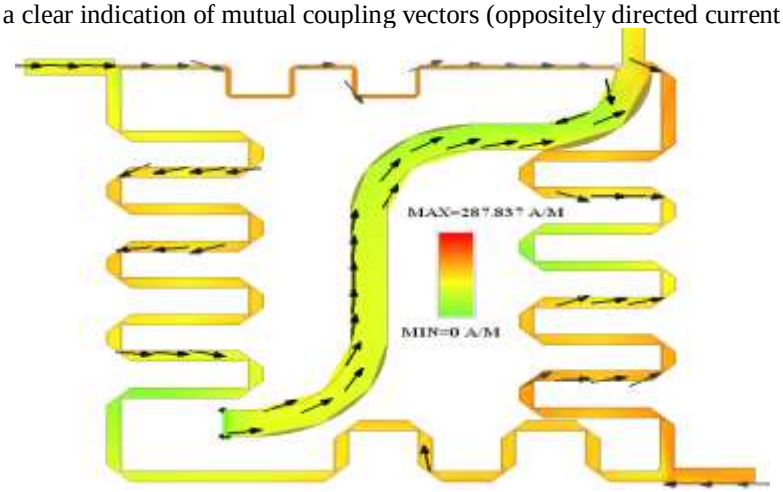

Figure 6: Surface current density distribution of the balun

Detailed simulation study on four different substrates other than Hi-Res Si is also performed to validate the versatility of the design. Table I shows the comparative study where all the parameter values are depicted. It has been observed that there is shift in centre frequency with variation of substrate characteristics keeping all the other parameters as fixed. For the lower dielectric constant substrate the tuning frequency shifts to a lower value.

TABLE I. COMPARITIVE STUDY OF BALUN'S PREFORMANCE ON DIFFERENT SUBSTRATES

Feature	**Alumina (25 mil)**	**5 □m Oxide on CMOS grade Si.**	**5 □m Polymide [PI 2525] on CMOS grade Si.**	**5 □m Nitride on CMOS grade Si.**
Centre Frequency(GHz)	1.9	1.8	1.8	1.8
Max Return loss(dB)	-25.627	-27.961	-28.611	-32.279
Max Insertion loss(dB)	-3.003	-3.026	-3.023	-3.012
Output phase difference (deg°)	-181.375	-179.169	-179.353	-180.337

Also the simulated parameter values obtained for the designed balun is compared with other designs incorporated on silicon substrate in Table II

TABLE II. COMPARISION OF DESIGNED BALUN WITH OTHER BALUN DESIGNS

Type of Balun design	**S_{11}(dB)**	**S_{21}(dB)**	**S_{31}(dB)**	**Phase difference (deg°)**
Conventional balun (on silicon substrate)[6]	-38.057	-3.471	-3.404	-179.595
Meandered balun (on silicon substrate)[6]	-33.679	-3.549	-3.394	-180.336
Proposed Balun	-23.08	-2.954	-3.113	-176.194

The comparison shows that the better results are obtained for the designed balun as compared to other balun design which are simulated on silicon substrate with a wide band nature and very compact size (60 % lower area than other baluns).

IV. FABRICATION PROCESS

Proposed fabrication steps are described as below in Fig.7 detailing required processes. At Step-5 the via-hole can be opened using the DRIE (**D**eep **R**eactive **I**on **E**tching) process and for the backside metallization evaporation technique can be utilized. In this way, we can use the simple CMOS technology to realize structure with desired design tolerances in respect of structural dimensions

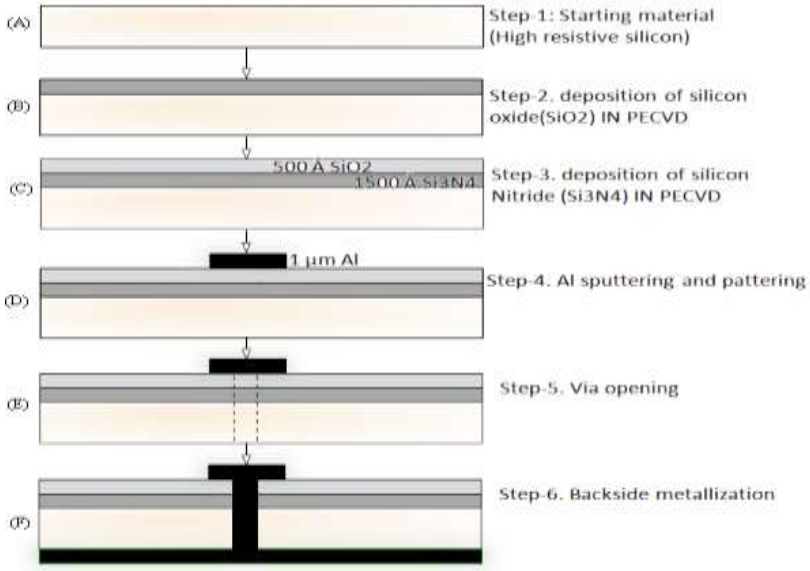

Figure 7: Steps for the proposed fabrication process

V. CONCLUSION

This article presents the design of a wideband balun structure of compact size, which can be realized using the MEMS technology and the proposed fabrication process is compatible with standard CMOS foundry. The designed three port circuit configuration has an added advantage of totally planar without any off-chip resistor as compared to conventional topologies. Better performance parameters are achieved by meandering all the four branches and attaching a short circuited stub at the top right corner of the balun. As the structure is targeted on Si-substrate, so integration of electronics (ASIC: **A**pplication **S**pecific **I**ntegrated **C**ircuits) will be easier to implement. As per author's knowledge, no other relevant circuit is designed on high permittivity substrates for wideband application. Three different analysis techniques are employed and comparative study is being carried out. This further establishes silicon as a viable MIC substrate for the development of system and sub-system. This design can be used for L1 band (1.575 GHz) GPS system and L-band long range surveillance radars for feeding network of mono-pulse antennas.

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