A Low Power MICS Band Transceiver Architecture for Implantable Devices

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Abstract

A sensor network system utilizing a low-power and miniature FSK transceiver for short-range biomedical applications is presented. The transceiver uses the new un-licensed band at 402-405 MHz recently allocated to Medical Implant Communication Systems (MICS) by FCC [1]. Although this band seems attractive providing low body absorption at these frequencies, it poses many challenges for RF designers to consider. Full-integration and low-power are the most important criteria for such an implantable transceiver. This paper mainly describes research work carried out on the design of a fully-integrated 402-MHz 0.18-µm low-power CMOS transceiver and discusses some of the challenges associated with full integration. System and circuit level issues are also addressed.

I. INTRODUCTION

The recent intensive effort in applications of transceiver chips for sensor networks has been accompanied by aggressive design goals such as low-cost, low-power, and very small size. The design of a trasceiver for transmitting biomedical signals over short ranges, on the other hand, requires special attention. The low bandwidth and low amplitude nature of the physiological signals imposes different design and optimization challenges to achieve low-power consumption and miniaturization.

The target application of the transceiver proposed here is to provide wireless communications for sensor based biomedical applications. One of the desired properties of the system is to provide communication with multiple sensor nodes for the purpose of monitoring/controlling more than one node. The transceiver acquires physiological data from sensor interface circuits and transfers this data to a remote system. The transceiver is supposed to be implanted together with sensor interface circuit and the sensors, as depicted in Fig.1.

The proposed system consists of a Main Control Unit (MCU) placed outside the body and implantable sensor nodes. The collection of data can be done one at a time from these nodes. Thus there is no time limitation and MCP initiated communication (polling) fits best for this application. Every sensor node can sleep most of the time and wake up for a very short time to see whether there is any communication session request from the MCU for that particular node. Only the ASIC processor, which can be designed to operate with a very low clock rate, stays awake. As a result, significant power saving is achieved and battery life is increased, which is very important for implantable devices.

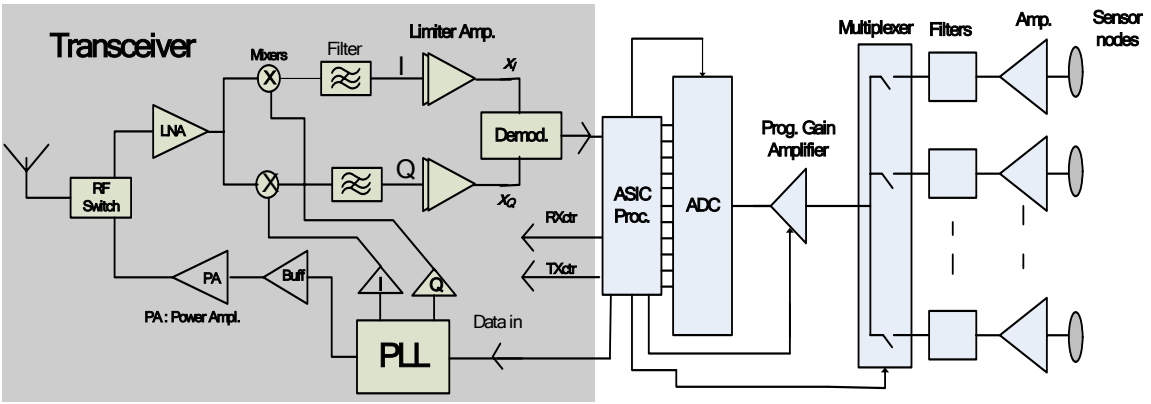

Figure 1. High-level block diagram of the proposed single sensor node.

Two main architectures that fit best for low power applications are direct conversion [2] and low-IF [4]. Complex image reject filter required in the case of low-IF requires high I-Q matching and high power consumption for a reasonable image rejection. Thus, direct conversion architecture is selected in the implementation due to its low-power and high-level integration advantages. Offset and flicker noise are serious issues in direct conversion. However, high modulation factor FSK is used to relieve these problems. Simplicity of FSK demodulation is another advantage. Because of the upper bound on the transmitter power (i.e. EIRP=-16dBm) [1],[5], integrated low-power power amplifier (PA) would not have an effect on the voltage-controlled oscillator (VCO)'s operation during the transmit mode, which is an important issue in the design of direct-conversion transceivers.

II. TRANSCEIVER ARCHITECTURE

The input data directly modulates the VCO frequency in the circuit design, eliminating the need to generate two separate frequencies necessary for FSK modulation. The data rate of 20 kb/s is enough for the application to accommodate a wide range of data coming from the interface circuit. The FSK tone frequency was selected to be $\pm\Delta f = 70kHz$ to fit into given maximum channel bandwidth of 300 kHz optimally. It relaxes the DC offset problem while keeping enough distance from the adjacent channel. A fractional-N PLL with 128/129 division ratio will correspond to a reference oscillator of ~3.14 MHz. With this selection, the whole 3-MHz MICS band (402-405 MHz) can be covered.

Sensitivity of the receiver can be determined by considering path loss in 2m and excess body loss. Thus, the minimum detectable signal level is MDS = -30 dB (free space loss in 2m [5]) –10 dB (excess body loss [6]) -35dBi (approximate antenna gain [5]) -16 dBm (maximum transmit power) = -91dBm. With a 50-KHz noise bandwidth (noise bandwidth is larger than the data bandwidth), for a 10-dB SNR value at the demodulator input, the noise figure requirement of the receiver is,

$$\begin{aligned} NF &= 174 - 10\log B - SNR + MDS \\ &= 174\text{-}47\text{-}10\text{-}91 = 26dB. \end{aligned} \quad (1)$$

This is a relaxed requirement and allows the design of a very low-power transceiver. The front-end components such as low-noise amplifier, mixers, and analog amplifiers can accommodate higher noise and therefore can be designed with less power than those of their counterparts.

The losses associated with an integrated matching network at 400 MHz would degrade the performance considerably. However, the relaxed noise figure requirement can be traded off for these drawbacks. At the transmit side, the PA can be designed to deliver around -5dBm power to a 50 ohm load to be consistent with max -16dBm EIRP [5] and also to save power (the sensitivity of the outside MCU unit can be high). Although the very low transmit-power requirement is advantageous in terms of integration of the PA without interfering the other blocks, the efficiency would degrade very much since the output device could not experience the full-swing at such a low output power level.

III. CIRCUIT REALIZATIONS

Some of the circuit implementation issues will be discussed in this section.

A. A Self Calibrating PLL with a Ring VCO

The fully integrated quadrature VCO is a great challenge for low power applications. It is difficult to have under-mW-oscillation with integrated lossy inductors at 400 MHz in case of an LC VCO. Quadrature signal generation is also serious issue, which requires additional power consumption. As a better choice, a four-stage differential ring oscillator is designed as shown in Fig. 2a. Although the phase noise performance of a ring VCO is worse than that of LC VCO, low power operation and small area requirement make it more attractive choice for this application. The required I and Q signals are already available in this case. The problem is to figure out that whether the phase noise requirement of the system can be satisfied by the ring option. Because of the fixed distance and upper bound on EIPR, the dynamic range is not too high (set by the path loss in 2m, ~30 dB). For this reason, the down conversion of the noise in the adjacent channel due to the phase noise of the oscillator is not very serious (except strong outside interferers; metrological aids service has primary allocation at 402-405 MHz band and the Earth exploration-satellite service together with metrological-satellite service have secondary allocation at 402-403 MHz [5]). Assuming 10-dB SNR due the next channel, the phase noise requirement of the VCO can be driven with the help of Fig. 2b as,

$$L(160KHz) = -30 - 10 - 10\log 20k = -83dBc/Hz. \quad (2)$$

Preliminary circuit simulations with 0.18-µm CMOS process have shown that this value can be achieved with a power consumption of 800-µW, including the buffers driving the mixers and the PA.

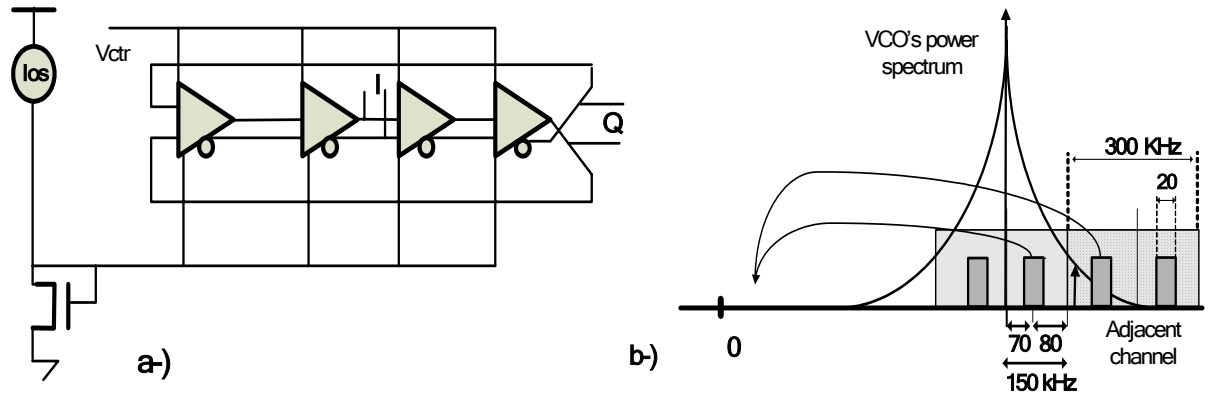

Figure 2. VCO design, a) Ring VCO schematic, b) down conversion of adjacent channel by the phase noise.

However, phase noise is not the only problem associated with the ring option. The excess dependence of oscillation frequency on process variations, and difficulty of having monotonic and linear tuning range are also serious issues. These problems can be addressed employing a second static calibration loop for the VCO as shown in Fig. 3a. By changing the source currents of the delay cells, the frequency can jump to the next clusters to search for the lock-frequency. This way the design can exploit low VCO gain, which means that the effect of the noise and charge-pump (CP) non-idealities on the oscillation frequency can be limited. This would also relax the integration of the loop filter (LF). Moreover, the VCO can be kept in the linear regions of the simulated tuning range show in Fig. 3b.

For the calibration loop, low frequency ASIC clock can be used to switch between the clusters during frequency search. The clusters are arranged to have approximately 3-MHz overlaps to assure continuous frequency search. Total frequency coverage is around 100 MHz with K_{VCO}=12 MHz/V in every cluster. The ring VCO has been implemented in 0.18-µm CMOS process including the buffers and a two stage power amplifier. Every component has been integrated including the 13.6 nH PA load inductor and two 9 pF MIM coupling capacitors in the RF signal path. The total die area is 550 µm X 600 µm including the bounding pads.

B. Digital Demodulator

It is important to note that the demodulator plays an important role in the system since it defines the receiver total sensitivity. The demodulator part of the proposed transceiver is given in Fig. 4. It takes the in-phase and quadrature signal components X_I, and X_Q as inputs as indicated in Fig.1 as well. In addition to the famous Vance's demodulator where the signal detection is simply done with a D-type flip-flop [7], we added digital counters/comparators before the detection flip-flop in order to increase the system performance. Because the signal might get distorted, the demodulator in [7] faces degradation in the signal detection.

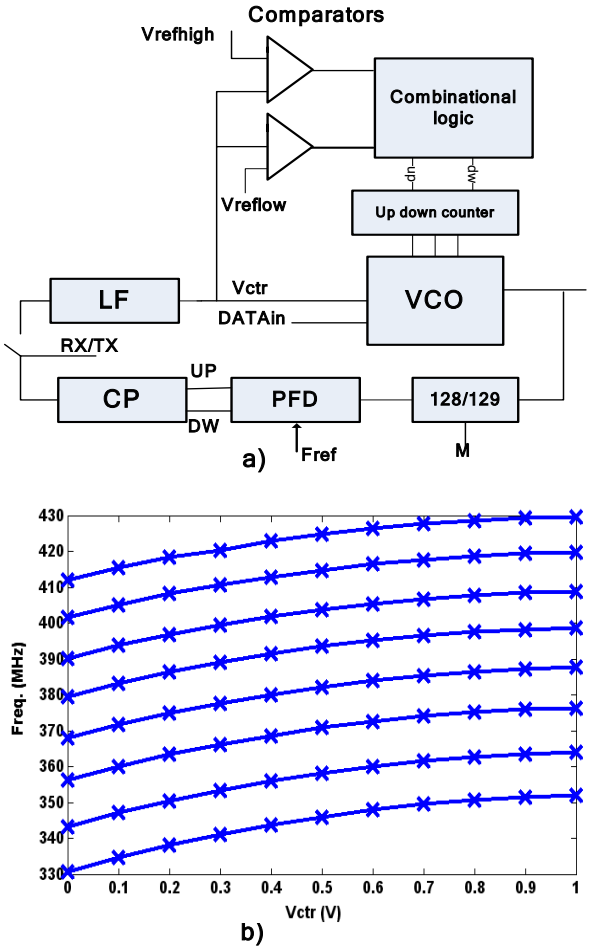

Figure 3. Self-calibrating PLL design, a) VCO with self-calibration loop, b) circuit simulated tuning characteristic in different clusters.

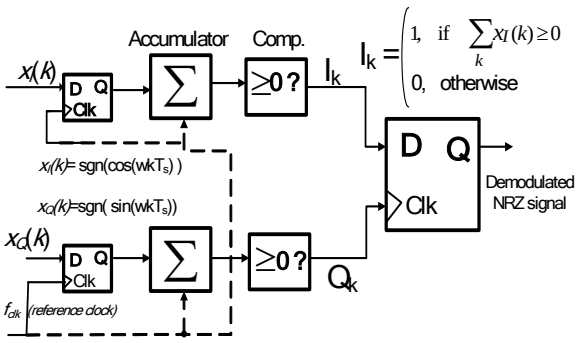

Figure 4. Enhancing performance of Vance's demodulator [7]. The digitized in-phase (X_I) and quadrature (X_Q) signals are obtained at the output of the limiter amplifiers shown in Fig.1.

The detailed waveforms of the digital demodulator are depicted in Fig. 5. The sinusoidal quadrature components I and Q are converted to the digital domain by two limiter amplifiers. These signals are, then, sampled by a reference clock, which is the PLL's reference clock already available in the system. Then, the digital comparator compares the total number of samples and decides whether it is less or bigger than zero. Thus, the errors in the X_I and X_Q are eliminated. The output of the comparator is either "1" or "0" within pulse duration T_I, as indicated in Fig. 5.

IV. CONCLUSION

A transceiver architecture targeting the new un-licensed medical band at 402-405 MHz has been described. System and circuit level trade-offs, some of which have been discussed, should carefully be studied to achieve a fully-integrated, low-power implantable transceiver operating at this new MICS band. The circuit blocks of the direct conversion FSK transceiver described in this paper are being implemented. The proposed self calibrating Ring VCO with direct modulation, buffers and power amplifier (Fig.6.) have been submitted for fabrication for characterization before integrating with the other loop components.

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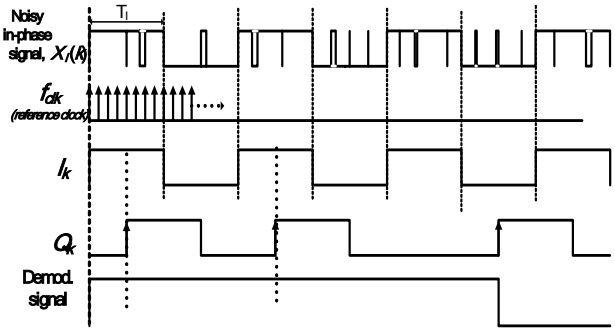

Figure 5. Signal waveforms of the digital demodulator.

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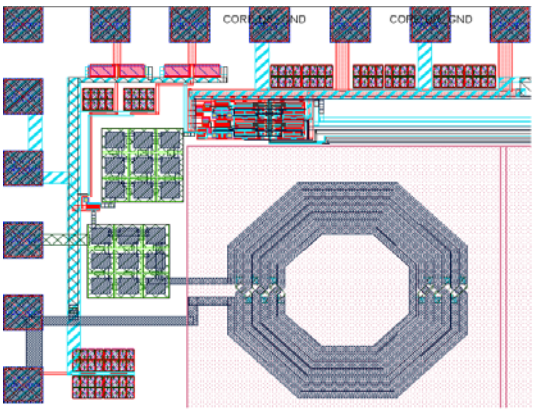

Figure 6. Layout of the designed transmitter (power amplifier, VCO, buffers).